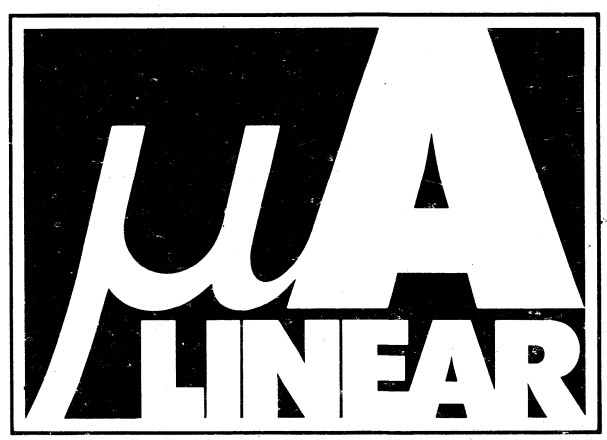
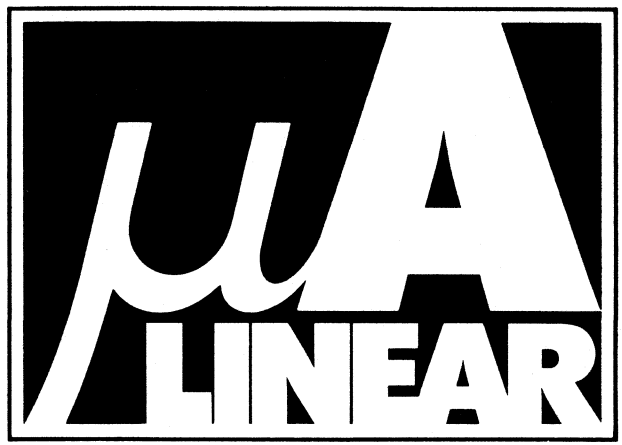
FAIRCHILD SEMICONDUCTOR



LINEAR INTEGRATED CIRCUITS DATA BOOK



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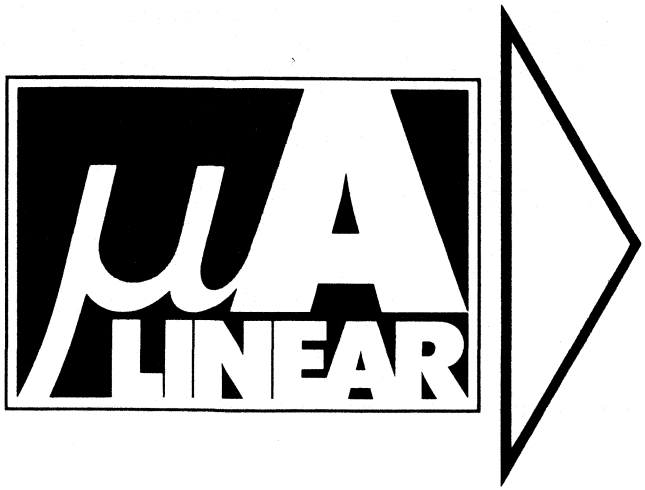
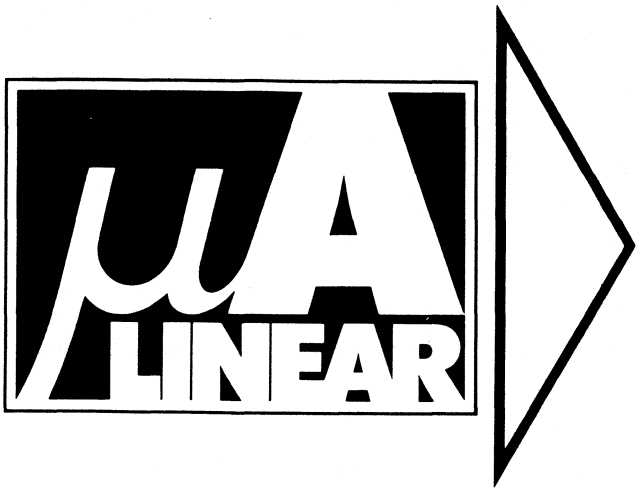


INTRODUCTION

The increase in linear IC complexity over the past decade has reflected industry demands for more compact subsystems promising higher efficiency and reliability at lower costs. Where only a few years ago, linear ICs were confined primarily to simple building blocks, – op amps, comparators, line drivers and receivers, etc. – today, complex subsystems such as the μA720 AM radio and the μA3089 FM IF detector are available on single chips. The dramatic influx of new devices, particularly in the interface, voltage regulator and consumer product areas has contributed significantly to the improved design and performance of linear systems.

This data book presents complete technical data on Fairchild's full line of linear integrated circuits. To expedite the designer's search for the right devices to meet various system requirements, several helpful aids are provided – selection guides by function, an LIC cross reference with 1000 devices and their Fairchild direct replacements or nearest equivalents, and a package cross reference for determining equivalent packaging within the industry. For the Hi Rel customer, descriptions of Fairchild's Hi Rel processing and Matrix VI are given in a separate section. To enhance the usefulness of this data book as an important member of the Fairchild data/application library, a comprehensive glossary and a list of available applications notes are included.



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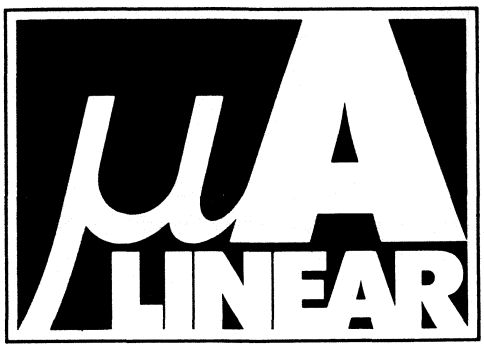


SELECTION GUIDE INDEX

CONSUMER CIRCUIT SELECTION GUIDE BY FUNCTION

TV

Function	Circuits
AFT	μA3064
Sound IF Amp. Lim. Detector	μA3065
Video Amplifier	TBA970
Chroma Processing NTSC	μA746, μA780, μA781, μA787, μA788
Chroma Processing PAL	TAA630S, TBA510, TBA520, TBA540, TBA560C, TBA990
Chroma Matrix	TBA530
Sync Separator Hor. Oscillator	μA1391, μA1394, TBA920
Audio Output	TBA800, TBA810S
Video Tape Recorders	μA796

AUDIO

Function	Circuits
AM Radio	μA720
AM-FM IF	μA721
IF Amplifiers	μA703, μA753
IF Amp. Lim. Detectors	μA2136, μA3075, μA3089
Stereo Demodulators	μA732, μA758, μA767
Audio Preamplifiers	μA739, μA749, μA7305
Four-Channel Sound	μA1312, μA1314, μA1315
Dolby Noise Reduction	μA7300
Audio Amplifiers	μA706, TBA641, TBA800, TBA810S, TBA810DS
Tape Motor Speed Control	μA7391

COMPARATOR SELECTION GUIDE
BY DEVICE NUMBER

(Note 7)

DEVICE NO.	Function	Input Offset Voltage (mV Max)	Temperature Coefficient of Input Offset Voltage (mV/°C)	Input Bias Current (μA) (Max)	Input Offset Current (μA) (Max)	Supply Voltage (V)	Response Time (ns)	Input Voltage Range (V)
	Notes	(2)	(4)	(2)	(2)	(2)	(1)	(2)
μA311	Voltage Comp	10	6.0	0.3	.07	0, +5.0 to ±15	200	±14
μAF311	FET Input Comp	10	6.0	150	.075	0, +5 to ±15	200	±14
μA710	High Speed Comp	5.0	5.0	40	7.5	+12, −6.0	40	±5.0(3)
μA711	Dual Comp	5.0	5.0	150	25	+12, −6.0	40	±5.0(3)
μA734	Precision Comp	7.5	3.5	0.15	.045	±5.0 to ±15	200	±5.0
μA760	High Speed Diff Comp	6.0	3.0	60	7.5	±4.5 to ±6.5	16	±4.0
μA775	Quad Comp	9	10	0.3	0.7	+2 to +36	1300	$\pm V_S$
μA3302	Quad Comp	40(6)	12	1.0(6)	.03(1)	+2 to +28(6)	2000	$\pm V_S$(6)

NOTES:
1. Typical values at 25°C unless otherwise specified.
2. Minimum or maximum value for $0°C \leq T_A \leq 70°C$ unless otherwise specified.
3. $V- = -7.0$ V
4. Typical
5. $T_A = +125°C$
6. Automotive temp. range −40°C to +85°C.
7. For temperature ranges and order information refer to specific data sheets and the Order Information Section.

COMPARATOR SELECTION GUIDE BY DEVICE NUMBER

(Note 7)

Output Voltage Swing (V)	Voltage Gain (V/mV) (Min)	Power Consumption (mW) (Max)	TTL Fanout	Diff. Input Voltage Range (V)	Package(s)	Military, Full Temp. Availability	Data Sheet Page No.
(2)	(5)	(5)	(1)	(2)			
0.4 to V_S	200(4)	205	5.0(Min)	±16	TO-99,9T	Yes	9-8
0.4 to V_S	200(4)	205	6	±16	TO-99,9T	Yes	9-3
−0.5 to +3.2	0.8	150	1	±5.0	TO-99,TO-91,6A,9A	Yes	9-10
−0.5 to +3.2	0.5	230(5)	1	±5.0	TO-91,TO-100,6A,9A	Yes	9-17
0 to +8.0	25	145	2	±10	TO-100,6A	Yes	9-21
0 to ±3.0	5.0(4)	325	2	±5.0	TO-99,6A	Yes	9-28
0.4 to V_S	25	12.5	4	$\pm V_S$	6A,9A	Yes	9-33
N.A.	2	22.5	1	$\pm V_S$	9A	(Note 6)	9-39

INTERFACE SELECTION GUIDE
BY DEVICE NUMBER

Line Drivers – Differential and Single-Ended Output

DEVICE NO.	Function	Companion Receiver	Type Output	Output Configuration	Output Current (mA)	Input Compatibility	Power Dissipation (mW) (Typ)	Number Drivers per Package	Supply Voltage (V)	Maximum Data Rate Line Length, etc.	tpd (ns)	Package(s)	Data Sheet Page No.
9612	Dual Diff. Driver	9613	Volt.	Diff.	40	TTL	150	2.0	+5		14	9T,8R,5B	11-19
9614	Dual Diff. Line Driver	9615	Volt.	Diff. or Single-Ended	40	TTL	170	2.0	+5		16	4L,6B,9B	11-27
9616	Triple RS 232 Line Driver	9627 9617	Volt.	Single Ended	17	TTL	250	3.0	+12; −12		300	6A,9A,3I	11-36
9621	Dual Line Driver	9622	Volt.	Diff. or Single Ended	20	TTL	100	2.0	+5; +12	See TTL Applications Handbook	13	6A,9A	11-47
55/75109	Dual Line Driver	75107 75108	Curr.	Diff.	6	TTL	180	2.0	+5; −5		9	6A,9A,3I	11-102
55/75110	Dual Line Driver	75107 75108	Curr.	Diff.	12	TTL	285	2.0	+5; −5		9	6A,9A,3I	11-109
55/75121	Dual Line Driver	75122	Volt	Single Ended	250 Fold-back Lim.	TTL	280	2.0	+5		20	6B,9B	11-113
75123	Dual IBM-360 Driver	75124	Volt.	Single Ended	250 Fold-back Lim.	TTL	280	2.0	+5		20	6B,9B	11-187
μA8T13	Dual Line Driver	μA8T14	Volt.	Single Ended	250 Fold-back Lim.	TTL	280	2.0	+5		15	6B,9B	11 3
μA8T23	Dual IBM-370 Line Driver	μA8T24	Volt.	Single Ended	250 Fold-back Lim.	TTL	280	2.0	+5		15	6B,9B	11-9
10123*	Triple Bus Driver	All 10K (ECL)	Volt.	Single Ended	20	ECL	312	3.0	−5.2		3	6B	
100123*	Hex Bus Driver	All 95K and 100K (ECL)	Volt	Single Ended	20	ECL	730	6.0	−4.5		1.8	4Q	

*Contact Fairchild ECL Product Marketing for product status and full product data.

Line Drivers – Differential or Single-Ended Output

DEVICE NO.	Function	Companion Receiver	Type Output	Output Configuration	Output Current (mA)	Input Compatibility	Supply Voltage (V)	Power Dissipation (mW) (Typ)	Number Drivers per Package	Line Length Operating Frequency	tpd (ns) (Typ)	Package(s)	Note
9H40/ 74H40	Dual 2-NAND Driver	Any TTL	Volt.	Single Ended	48	TTL	+5	88	2.0		7	TO-86 6A,9A	
9N37/ 7437	Quad 2-NAND Driver	Any TTL	Volt.	Single Ended	48	TTL	+5	108	4.0		10	TO-86 6A,9A	
9N38/ 7438	Quad 2-NAND Driver	96106	Volt.	Single Ended	48	TTL	+5	98	4.0		13	TO-86 6A,9A	
9N40/ 7440	Dual 2-NAND Driver	Any TTL	Volt.	Single Ended	48	TTL	+5	52	2.0		11	TO-86 6A,9A	
9S40/ 74S40	Dual 2-NAND Driver	Any TTL	Volt.	Single Ended	48	TTL	+5	88	2.0		4.0	TO-86 6A,9A	
9009	Dual 2-NAND Driver	Any TTL	Volt.	Single Ended	48	TTL	+5	54	2.0		10	TO-86 6A,9A	
74S140	Dual 2-NAND 50 Ω Driver	Any TTL	Volt.	Single Ended	40	TTL	+5	88	2.0		4.0	TO-86 6A,9A	
96101	Quad 2-NAND Driver	96106	Volt.	Single Ended	48	TTL	+5	98	4.0		13	TO-86 6A,9A	

See Fairchild TTL Application Handbook

Note: Contact Fairchild DIC Product Marketing for full data.

3

INTERFACE SELECTION GUIDE
BY DEVICE NUMBER

Line Receivers

DEVICE NO.	Function	Companion Driver	Input Threshold Sensitivity V_{TH} (mV)	Common Mode (V)	Hysteresis Capability	Output Compatibility	Power Supply Voltage (V)	Power Dissipation (mW) (Typ)	tpd (ns) (Typ)	Number Receivers per Package	Package(s)	Data Sheet Page No.
9613	Dual Diff. Line Receiver	9612	±500	±15	No	TTL	+5	143	25	2.0	9T,8B,5B	11-23
9615	Dual Diff. Line Receiver	9614	±1000	±15	No	TTL	+5	150	30	2.0	4L,6B,9B	11-31
9617	Triple RS 232 Line Receiver	9616	+1500	±25	Yes	TTL	+5	60	40	3.0	6A,9A,3I	11-39
9620	Dual Diff. Line Receiver	9621	±500	±15	No	TTL	+5 +12	110	35	2.0	6A,3I,9A	11-41
9622	Dual LIne Receiver	9621	+1500	±10	No	TTL	+5 −10	140	38	2.0	6A,3I,9A	11-53
55/75107A 55/75107B	Dual Line Receiver	75109 75110	±25	±3	No	TTL	±5	130	17	2.0	6A,9A,3I	11-102
55/75108A 55/75108B	Dual Line Receiver	75109 75110	±25	±3	No	TTL	±5	130	19	2.0	6A,9A,3I	11-102
75207	Dual MOS Sense Amp	75109 75110	±10	±3	No	TTL	±5	130	17	2.0	6A,9A	11-119
75208	Dual MOS Sense Amp	75109 75110	±10	±3	No	TTL	±5	130	19	2.0	6A,9A	11-119
55/75122	Triple Line Receiver	75121	+1500	+5	Yes	TTL	+5	315	20	3.0	6B,9B	11-116
75124	Triple IBM-370 Line Receiver	75123	+1500	+5	Yes	TTL	+5	315	20	3.0	6B,9B	11-190
μA8T14	Triple Line Receiver	μA8T13	+1500	+5	Yes	TTL	+5	315	20	3.0	6B,9B	11-6
μA8T24	Triple IBM-370 Line Receiver	μA8T23	+1500	+5	Yes	TTL	+5	315	20	3.0	6B,9B	11-12

INTERFACE SELECTION GUIDE
BY DEVICE NUMBER

Line Receivers

DEVICE NO.	Function	Companion Driver	Input Threshold Sensitivity V_{TH} (V)	Common Mode (V)	Hysteresis Capability	Output Compatibility	Power Supply Voltage (V)	Power Dissipation (mW) (Typ)	tpd (ns) (Typ)	Number Receivers per Package	Package(s)	Data Sheet Page No.
9582*	Triple Line Receiver	All ECL Logic	V_{REF}	±1	No	ECL	−5.2	250	2.2	3	6B	
9627	Dual RS 232/ MIL Std 188 Line Receiver	9616	45	±25	No	TTL	±12	234	70	2	6B,9B,3I	11-64
10014*	Active Termination	All ECL Logic	V_{REF}	NA	No	ECL	−5.2	65	NA	14	6B,9B	
10114*	Triple Line Receiver	All ECL Logic	V_{REF}	±1	No	ECL	−5.2	145	2.2	3	6B,9B	
10115*	Quad Line Receiver	All ECL Logic	V_{REF}	2	No	ECL	−5.2	95	1.9	4	6B,9B	
10116*	Triple LIne Receiver	All ECL Logic	V_{REF}	2	No	ECL	−5.2	75	1.9	3	6B,9B	
95115*	Quad Line Receiver	All ECL Logic	V_{REF}	2	No	ECL	−5.2	95	1.9	4	6B	
95116*	Triple LIne Receiver	All ECL Logic	V_{REF}	2	No	ECL	−5.2	75	1.9	3	6B	
96106**	Quad 2-NOR Bus Receiver	96101	1.5	-	No	TTL	5.0	90	20	4	TO-86 6A,9A	
100114*	Quint Line Receiver	All ECL Logic	V_{REF}	±1.0	No	ECL	−4.5	380	1.2	5	4Q	

*Contact Fairchild DIC Product Marketing for full data.
**Contact Fairchild ECL Product Marketing for full data.

INTERFACE SELECTION GUIDE
BY DEVICE NUMBER

Display Drivers

DEVICE NO.	Function	Input Compatibility	BCD Decoder	Ripple Blanking	Blanking Above BCD 9 Input	Output Current (mA)	Maximum Output Standoff Voltage (V)	Active HIGH/LOW	Display Type	Standby Power Dissipation (mW)	Package(s)	Data Sheet Page No.
9307	7-Segment Decoder	TTL	Yes	Yes	No	11	5.5	H	LED Com. Cathode	165	4L 7B,9B	11-15
9315	1-of-10 Cold Cathode	TTL	Yes	No	No	7	55	L	Gas Discharge	145	4L 6B,9B	
9317	7-Segment Decoder/Driver	TTL	Yes	Yes	Yes	"B"–40 mA "C"–20 mA	"B" –20 "C"–30	L	Common Anode LED	220	4L 7B,9B	11-16
9357	7-Segment Decoder/Driver	TTL	Yes	Yes	No	40	"A"–30 "B"–15	L	Common Anode LED	320	4L 7B,9B	
9358	7-Segment Decoder	TTL	Yes	Yes	No	8	5.5	H	Logic	265	4L 7B,9B	
9368	7-Segment LED Driver	TTL	Yes	Yes	No	20	5.5	H	LED Comm. Cathode	225	4L 6B,9B	11-17
9370	7-Segment LED Driver	TTL	Yes	Yes	No	25	5.5	L	Common Anode LED	350	4L 6B,9B	11-18
9374	7-Segment LED Driver	TTL-CMOS	Yes	Yes	No	15	10	L	Common Anode LED	175	4L 6B,9B	
9664A	Hex Digit Driver	MOS-TTL-CMOS	No	No	No	150	20	L	LED	Neg.	9A	11-68
75491A	Quad Digit Seg. Driver	MOS-TTL-CMOS	No	No	No	50	20	L	LED	Neg.	9A	11-198
75492A	Hex Digit Driver	MOS-TTL-CMOS	No	No	No	250	20	L	LED	Neg.	9A	11-198
93141*	1-of-10 Cold Cathode	TTL	Yes	No	No	7	55	L	Gas Discharge	80	4L 7B,9B	

*Contact Fairchild DIC Product Marketing for full data.

INTERFACE SELECTION GUIDE BY DEVICE NUMBER

Level Translators

DEVICE NO.	Function	Supply Voltage V^+	Supply Voltage V^-	V_{OH} (V)	V_{OL} (V)	t_{pd} (ns)	Power Dissipation (mW)	Package(s)	Data Sheet Page No.
9109*	HLDTL-TTL Hex	12 to 20	0.0	0.0	0.4	120	380	TO-86 6A,9A	
9112*	TTL-HLDTL Hex	12 to 20	0.0	(+V) −2.0	0.4	90	440	TO-86 6A,9A	
9595**	Dual ECL-TTL Translator	+5.0	−5.2	2.4	0.4	6.0	375	6B	
(3207A)* 9607	TTL-MOS Quad Clock Driver	15 to 21	0.0	(+V) −0.2	0.2	25	300	4L, 6B,9B	
9624	TTL-MOS Translator	+5.0	0.0 to −30	V_{TAP} −1.0	(−V) +2.0	120	40	6A,9A,3I	11-57
9625	MOS-TTL Dual Level Translator	+5.0	0.0 to −30	3.2	0.4	70	60	6A,9A,3I	11-57
10124**	TTL-ECL Quad Diff. Driver	+5.0	−5.2	−0.885	−1.750	3.0	150	6B,9B	
10125**	ECL-TTL Quad Buffer	+5.0	−5.2	2.5	0.5	3.0	300	6B,9B	
95124**	TTL-ECL Quad Diff. Driver	+5.0	−5.2	−0.965	−1.705	3.0	160	6B	

*Contact Fairchild DIC Product Marketing for full data.

**Contact Fairchild ECL Product Marketing for full data.

High Speed TTL Buffers and Peripheral Drivers

DEVICE NO.	Function	Switching Speed tpd (ns)	Output Current C.7 V (mA)	Gate Function	Circuit Function	Transistor Connection Mode	Input Compatibility	Output Voltage (V)	Min. Latchup Voltage (mV)	Number of Drivers	Package(s)	Data Sheet Page No.
55/75450A 55/75450B	Dual Peripheral Drivers	30	300	NAND	-	External	TTL	30	V_{CC} −6.5	2	6A,9A	11-137 11-151
55/75451A 55/75451B	Dual Peripheral Drivers	25	300	NAND	AND	Internal	TTL	30	V_{CC} −6.5	2	9T,5B,8B	11-137 11-151
55/75452A 55/75452B	Dual Peripheral Drivers	35	300	AND	NAND	Internal	TTL	30	V_{CC} −6.5	2	9T,5B,8B	11-137 11-151
55/75453A 55/75453B	Dual Peripheral Drivers	25	300	NOR	OR	Internal	TTL	30	V_{CC} −6.5	2	9T,5B,8B	11-137 11-151
55/75454A 55/75454B	Dual Peripheral Drivers	35	300	OR	NOR	Internal	TTL	30	V_{CC} −6.5	2	9T,5B,8B	11-137 11-151

INTERFACE SELECTION GUIDE
BY DEVICE NUMBER

High Current, High Voltage TTL Buffers and Peripheral Drivers

DEVICE NO.	Function	Maximum Output Current (mA)	Output Standoff Voltage (V)	Minimum Latchup Voltage (mV)	Input Compatibility	Gate Function	Logic Function	Switching Speed (ns)	Number Drivers per Package	Package(s)	Data Sheet Page No.
9664A	Hex Drivers	150 @ 1.2 V	20	-	MOS, TTL CMOS	-	-	600	6	9A	11-68
75491A	Quad Drivers	50 @ 1.2 V	20	-	MOS, TTL CMOS	-	-	600	4	9A	11-198
75492A	Hex Drivers	250 @ 1.2 V	20	-	MOS, TTL CMOS	-	-	600	6	9A	11-198
55/75450A 55/75450B	Dual Drivers	300 @ .7 V	30	V_{CC} −6.5	TTL	NAND	-	30	2	6A,9A	11-137 11-151
55/75451A 55/75451B	Dual Drivers	300 @ .7 V	30	V_{CC} −6.5	TTL	NAND	AND	30	2	9T,5B,8B	11-137 11-151
55/75452A 55/75452B	Dual Drivers	300 @ .7 V	30	V_{CC} −6.5	TTL	AND	NAND	30	2	9T,5B,8B	11-137 11-151
55/75453A 55/75453B	Dual Drivers	300 @ .7 V	30	V_{CC} −6.5	TTL	NOR	OR	30	2	9T,5B,8B	11-137 11-151
55/75454A 55/75454B	Dual Drivers	300 @ .7 V	30	V_{CC} −6.5	TTL	OR	NOR	30	2	9T,5B,8B	11-137 11-151
55/75460	Dual Drivers	300 @ .7 V	35	V_{CC}	TTL	NAND	-	35	2	6A,9A	11-165
55/75461	Dual Drivers	300 @ .7 V	35	V_{CC}	TTL	NAND	AND	35	2	9T,5B,8B	11-165
55/75462	Dual Drivers	300 @ .7 V	35	V_{CC}	TTL	AND	NAND	35	2	9T,5B,8B	11-165
55/75463	Dual Drivers	300 @ .7 V	35	V_{CC}	TTL	NOR	OR	35	2	9T,5B,8B	11-165
55/75464	Dual Drivers	300 @ .7 V	35	V_{CC}	TTL	OR	NOR	35	2	9T,5B,8B	11-165
SH2001	High Voltage High Current Driver	250	50	-	DTL,TTL	-	NAND	70	1	5E	11-202
SH2002	High Voltage High Current Driver	150	40	-	DTL,TTL	-	NAND	70	1	5E	11-202
SH2200	High Voltage High Current Driver	500	50	-	DTL,TTL	-	NAND	80	1	5E	11-206
SH2201	High Voltage High Current Driver	500	100	-	DTL,TTL	-	NAND	100	1	5E	11-206

INTERFACE SELECTION GUIDE BY DEVICE NUMBER

MOS and Core Memory Drivers

DEVICE NO.	Function	Supply Voltage (V)	Input Compatibility	Output Current Capability (mA)	Propagation Delay (ns)	Package(s)	Data Sheet Page No.
9607 (3207A)*	Quad MOS Driver	15 to 21	TTL	250	9	6B,9B	
55/75325	Core Driver	+5, +24	TTL	600	25	4L,7B,9B	11-125

*Contact Fairchild DIC Product Marketing for full data.

MOS and Core Sense Amplifiers

DEVICE NO.	Function	Differential Threshold Voltage (mV)	Common Mode Range (V)	Gate Function	Output Configuration	tpd (ns) (Typ)	Package(s)	Data Sheet Page No.
7524	Dual Sense Amp	11 Min to 19 Max V_{REF} = 15 mV	±2.5	AND	Com. Collector	25	6B,9B,3I	
7525	Dual Sense Amp	8 Min to 22 Max V_{REF} = 15 mV	±2.5	AND	Com. Collector	25	6B,9B,3I	
7528	Dual Sense Amp	11 Min to 19 Max V_{REF} = 15 mV	±2.5	AND	Com. Collector	25	6B,9B	
7529	Dual Sense Amp	8 Min to 22 Max V_{TH} = 15 mV	±2.5	AND	Com. Collector	25	6B,9B	

INTERFACE SELECTION GUIDE BY DEVICE NUMBER

MOS and Core Sense Amplifiers
(Cont'd)

DEVICE NO.	Function	Differental Threshold Voltage (mV)	Common Mode Range (V)	Gate Function	Output Configuration	tpd (ns) (Typ)	Package(s)	Data Sheet Page No.
7534	Dual Sense Amp	11 Min to 19 Max V_{REF} = 15 mV	±2.5	NAND	Uncom. Collector	25	6B,9B	11-71
7535	Dual Sense Amp	8 Min to 22 Max V_{REF} = 15 mV	±2.5	NAND	Uncom. Collector	25	6B,9B	11-71
55/75107A 55/75107B	Dual Sense Amp	±25	±3	NAND	Com. Collector	17	6A,9A,3I	11-102
55/75108A 55/75108B	Dual Sense Amp	±25	±3	NAND	Uncom. Collector	19	6A,9A,3I	11-102
75207	Dual Sense Amp	±10	±3	NAND	Com. Collector	17	6A,9A	11-119
75208	Dual Sense Amp	±10	±3	NAND	Uncom. Collector	19	6A,9A	11-119
75234	Dual Sense Amp	11 Min to 19 Max V_{REF} = 15 mV	±2.5	NAND	Com. Collector	25	6B,9B,3I	11-71
75235	Dual Sense Amp	11 Min to 19 Max V_{REF} = 15 mV	±2.5	NAND	Com. Collector	25	6B,9B,3I	11-71

D/A – A/D Conversion

DEVICE NO.	Function	Linearity (% Full Scale Max)	Full Scale Output Current Error (% Max)	Output Current Capability (mA) (MSB) (MAX)	Input Compatibility	Package(s)	
9650	4-Bit Current Source	±0.01	±.1	+2.0	TTL	6B	

Note: Contact Fairchild DIC Product Marketing for full data.

SENSE AMPLIFIER SELECTION GUIDE
BY DEVICE NUMBER

DEVICE	Supply Voltages (V)	TTL Compatible Outputs	Open Collector Outputs	V_{TH} (mV)	R_{IN} (kΩ)	P_D (mW)	t_{pd} (ns)	Output Enable	Wired-OR Output
55/7524	+5.0 −5.0	Yes		±4.0	2.5	180	25	Yes	
55/7525	+5.0 −5.0	Yes		±7.0	2.5	180	25	Yes	
55/7528	+5.0 −5.0	Yes		±4.0	2.5	180	25	Yes	
55/7529	+5.0 −5.0	Yes		±7.0	2.5	180	25	Yes	
55/7534	+5.0 −5.0	Yes	Yes	+4.0	2.5	180	25	Yes	Yes
55/7535	+5.0 −5.0	Yes	Yes	±7.0	2.5	180	25	Yes	Yes
55/7538	+5.0 −5.0	Yes	Yes	±4.0	2.5	180	25	Yes	Yes
55/7539	+5.0 −5.0	Yes	Yes	±7.0	2.5	180	25	Yes	Yes
55/75207	+5.0 −5.0	Yes		±10	10	130	15	Yes	
55/75208	+5.0 −5.0	Yes	Yes	±10	10	130	15	Yes	Yes
55/75224	+5.0 −5.0	Yes		±4.0	2.5	180	25	Yes	
55/75225	+5.0 −5.0	Yes		±7.0	2.5	180	25	Yes	
55/75232	+5.0 −5.0	Yes	Yes	±4.0	2.5	180	25	Yes	Yes
55/75233	+5.0 −5.0	Yes	Yes	±7.0	2.5	180	25	Yes	Yes
55/75234	+5.0 −5.0	Yes		±4.0	2.5	180	25	Yes	
55/75235	+5.0 −5.0	Yes		±7.0	2.5	180	25	Yes	
55/75238	+5.0 −5.0	Yes		±4.0	2.5	180	25	Yes	
55/75239	+5.0 −5.0	Yes		±7.0	2.5	180	25	Yes	

Note: All values are typical.

INTERFACE SELECTION GUIDE
BY DEVICE NUMBER

Tape – Disc Preamplifiers

DEVICE NO.	Function	Voltage Amplification	Bandwidth (–3 dB) (Hz) (Typ)	Bandwidth Unity Gain (Hz) (Typ)	Input Offset Current (μA) (Typ)	Input Offset Voltage (mV) (Typ)	Package(s)	Output Voltage Swing (V) (Typ)	Data Sheet Page No.
μA733	Diff. Video Amp	10-400 Adj.	200 MHz Gain 10	400 MHz	0.4	1.5 (Gain 400)	4.7	5B,6A,3F	13-16
μA739	Dual Low Noise Preamp.	6.5 k	300 k	1 M	.05	1.0	+2.8-−4.0	6A,9A	12-77

INTERFACE SELECTION GUIDE
BY DEVICE NUMBER

Monostables (One Shots)

DEVICE NO.	Function	Pulse Width Variation (%)		Number of Inputs		Resettable	Min Output (t_W) (ns)	Power Dissipation (mW) (Typ)	Package(s)	Note
		Temp	vs V_{CC}	Positive	Negative					
9600	Single Retriggerable	±1.5	±1.5	3.0	2.0	X	75	125	TO-86,6A	
9601	Single Retriggerable	±2.7	±1.0	2.0	2.0	-	50	125	TO-86, 6A,9A	
9602	Dual Retriggerable	±1.5	±1.5	1.0	1.0	X	72	250	4L,6B,9B	
96L02	Dual Retriggerable	±0.4	±0.5	1.0	1.0	X	110	50	4L,6B,9B	
9603/ 74121	Single Non-Retriggerable	±0.2	±0.15	1.0	2.0	-	40	90	TO-86, 6A,9A	
96S02	Dual Retriggerable	±0.2	±0.2	1.0	1.0	X	7	250	4L,6B,9B	
9N122/ 74122	Single Retriggerable	±2.7	±1.0	2.0	2.0	X	45	115	TO-86, 6A,9A	
9N123/ 74123	Dual Retriggerable	±2.7	±1.0	1.0	1.0	X	45	230	4L,6B,9B	

Note: Contact Fairchild DIC Product Marketing for full data.

Analog Switch

DEVICE NO.	Function	Switching Speed (ns)	Channel Resistance (Ω) (Max)	Supply Voltage (V)	Input Logic	Package(s)	Data Sheet Page No.
SH3002	SPDT Analog Switch	75	200	±12	TTL	5E	11-210
SH3003	DPST Analog Switch	75	200	±12	TTL	5E	11-210

FUNCTIONAL SELECTION GUIDE FOR LINE DRIVERS

Device Requirements

DEVICE	Supply Voltages (V)	TTL Compatible Inputs	V_{OH} (V)	V_{OL} (V)	I_{OH} (mA)	I_{OL} (mA)	t_{pd} (ns)	P_D at Channel (mW)
9612	+5.0	Yes	3.5	0.2	−40	40	15	75
9614	+5.0	Yes	3.5	0.2	−40	40	16	75
9616 (Note 1)	+12 −12	Yes	6.0	−6.0	−17	15	-	90
9621	+5.0 +12	Yes	4.3	0.2	−20	20	13	50
9624 (Note 2)	+5.0 −10 to −30	Yes	V_{TAP} −1.5	V_{DD} +0.2	−2.0	30	120	107
9634*	+5.0	Yes	3.5	0.35	−75	90	7.0	50
9636*	+12 −12	Yes	5.5	−5.5	−15	15	-	190
9638*	+5.0	Yes	3.5	0.35	−75	90	7.0	63
9640*	+5.0	Yes	-	0.35	-	40	10	200
75109	+5.0 −5.0	Yes	-	-	-	6.0	9.0	70
75110	+5.0 −5.0	Yes	-	-	-	12	9.0	70
μA8T13 (Note 3)	+5.0	Yes	3.5	-	−210	-	15	75
μA8T23 (Note 3)	+5.0	Yes	3.5	-	−210	-	15	75

NOTES FOR LINE DRIVERS/INTERFACE DRIVERS

(1) The 9616 is a triple EIA line driver. Each driver incorporates an internal response control circuit. The slew rate is a maximum of 30 V/μs and a minimum of 4 V/μs (3% of unit interval at 20 k baud). The two values for I_{SC} are the typical V_{OH} and V_{OL} short circuit currents. The t_{pd} is measured from 1.5 V on the input to the output passing through the 0 V point. The delay is caused by the internally controlled slew rate of the output. The 9616 meets the electrical interface requirements of EIA-RS-232C and the CCITT recommendation V.24. By using an external capacitor from the output to ground for wave shaping, the 9616 will also meet the low level digital interface for MIL-STD-188C.

(2) The 9624 dual TTL/DTL to MOS level converter is designed to operate with a V_{DD} from 0 to −30 V.

(3) The μA8T13 and μA8T23 have foldback current limited outputs. V_{OL} is a typical V_{CE} of the output transistor at collector currents of 100 mA (V_{OL} = 0.25 V) and 300 mA (V_{OL} = 0.5 V).

(4) All values are typical.

*To be announced

FUNCTIONAL SELECTION GUIDE FOR LINE RECEIVERS

Device Requirements

(Note 2)

DEVICE	Supply Voltages (V)	TTL Compatible Outputs	V_{TH} (V)	V_{CM} (V)	R_{IN} (kΩ)	P_D (mW)	t_{pd} (ns)	Differential Inputs	Output Enable	Response Control	Line Terminator	Wired-OR Output	Failsafe Control
9615	+5.0	Yes	±0.5	±15	7.0	150	30	Yes	Yes	Yes	Yes	Yes	
9617	+5.0	Yes	+1.5	±25	4.0	60	40			Yes	Yes	Yes	Yes
9620	+5.0 +12	Yes	±0.5	±15	2.4	110	35	Yes		Yes		Yes	
9622	+5.0 −10	Yes	+1.5	±10	5.0	140	38	Yes	Yes		Yes	Yes	Yes
9625	+5.0 −11 to −30	Yes	−3.0 to −9.0	-	22	60	90						
9627 (Note 1)	+12 −12	Yes Wired-OR	±0.6 ±2.4	±2.5	3 to 7 or > 6	234	84	Yes	Yes		Yes	Yes	
μA8T14	+5.0	Yes	+1.5	-	18	315	20						
μA8T24	+5.0	Yes	+1.5	-	18	315	20						
75107	+5.0 −5.0	Yes	±0.025	±3.0	16	130	17	Yes	Yes				
75108	+5.0 −5.0	Yes Open Collector	±0.025	±3.0	16	130	19	Yes	Yes			Yes	

NOTES:

(1) 9627 Dual EIA RS-232/MIL-STD 188C Line Driver allows two levels of hysteresis and a choice of input resistances to satisfy both the EIA RS-232 and MIL-STD 188C electrical specifications.

(2) All values are typical.

FUNCTIONAL SELECTION GUIDE FOR LINE DRIVERS/LINE RECEIVERS

System Requirements

Standard

Interface	Recommended		Comments
	Driver	Receiver	
EIA RS422	9638	9637	0 to 10M bps
EIA RS423	9636	9637	0 to 100K bps
EIA RS232-C	9616	9617	0 to 20,000 bps, maximum cable length implied in standard is 50'.
MIL-STD-188C	9616	9627	Use capacitor from 9616 output to ground to provide wave shaping at applicable modulation rate.
IBM 360 I/O	μA8T23, 75123	μA8T24, 75124	Recommended maximum of 10 ports on bus.

Single-Ended Simplex

Line Length (feet)	Maximum Data Rate (NRZ Data)	Line* Type and Z_O	Recommended		Comments
			Driver	Receiver	
0 – 2	20M bps	SW, TP, COAX $> 90\ \Omega$	TTL Gate	TTL Gate	Unterminated line. Obey loading rules.
2 – 20	10M bps	TP, TPS, COAX $> 90\ \Omega$	9009 or 7440	TTL Gate	Use parallel terminated line with more than one receiver. Use series terminated line with only one receiver.
		COAX $\geq 50\ \Omega$	9S140	TTL Gate	Use parallel terminated line with more than one receiver. Use series terminated line with only one receiver.
20 – 500	10M bps @ 20' 0.5M bps @ 500'	TPS, COAX $\geq 50\ \Omega$	μA8T13, 75121	μA8T14, 75122	Use parallel terminated line.
> 500					Not recommended. Use balanced differential form to gain system noise immunity.

Single-Ended Multiplex

0 – 2	10M bps	SW	Open Collector TTL	TTL Gate	Use wired-AND with low value (< 1 kΩ) collector pull-up resistor. Obey loading rules.
2 – 20	10M bps	TP, COAX $> 75\ \Omega$	μA8T13, 75121 or μA8T23, 75123	μA8T14, 75122 or μA8T24, 75124	Single +5 V supply. Use parallel termination at both ends of bus.
20 – 500	10M bps @ 20' 0.5M bps @ 500'	COAX $> 95\ \Omega$	μA8T23, 75123	μA8T24, 75124	Use parallel termination at both ends of bus. Single +5 V supply required.
> 500					Not recommended. Use balanced differential form to gain system noise immunity.

FUNCTIONAL SELECTION GUIDE FOR LINE DRIVERS/LINE RECEIVERS
System Requirements

Differential Simplex

Line Length (feet)	Maximum Data Rate (NRZ Data)	Line* Type and Z_O	Recommended Driver	Recommended Receiver	Comments
0 – 50	10M bps	TP, TPS > 50 Ω	9612 9614 9634 9638	9613/15 9613/15 9635 9637	Use parallel termination. Single +5 V supply required.
		TP, TPS > 80 Ω	75109/ 75110/ 75112	75107/ 75108	Split parallel termination. ±5 V supplies required.
50 – 4000	Use signal quality graph	TPS > 50 Ω	9612 9614 9634 9638	9613/15 9613/15 9635 9637	Use parallel termination. Single +5 V supply required.
		TPS > 80 Ω	75110/ 75112	75107/ 75108	Use split parallel termination. ±5 V supplies required.
> 4000					Cable loss exceeds 6 dB V. Perhaps non-baseband techniques should be used (i.e., MODEMS)

Differential Multiplex

0 – 50	15M bps	TP, TPS > 90 Ω	75110 75112	75107/ 75108	Use split parallel termination at each end of line. Requires +5 V and −5 V supplies.
		TP, TPS > 90 Ω	9614	9615	Connect as shown in half duplex differential circuit. Requires single +5 V supply.
			9634 9638	9635 9637	
50 – 4000	Use signal quality graph	TPS > 90 Ω	75110/ 75112	75107/ 75108	Use split parallel termination at each end of line. Requires +5 V and −5 V supplies.
> 4000					Cable loss exceeds 6 dB V. Perhaps non-baseband techniques should be used (i.e., MODEMS)

*SW – Single Wire over Grounded Connection; TP – Twisted Pair; TPS – Shielded Twisted Pair; COAX – Coaxial Cable

FUNCTIONAL SELECTION GUIDE FOR GENERAL PURPOSE – HIGH CURRENT DRIVERS

High Current Drivers are designed with inputs TTL and/or MOS compatible and output stage capable of handling high currents. These circuits are ideal as lamp, relay, LED, and memory drivers.

PERIPHERAL DRIVERS – 55/75450 SERIES, 55/75460 SERIES, 55/75470 SERIES: Peripheral Drivers are dual monolithic circuits, each circuit consisting of a TTL logic gate and a high current NPN transistor guaranteed to sink 300 mA.

DEVICE NUMBER	GATE FUNCTION	CIRCUIT FUNCTION	TRANSISTOR CONNECTION MODE	CURRENT CAPABILITY (TYP)
				I_{OUT} at V_{OUT}
55/75450, 460, 470	NAND	NA	External	300 mA at 0.7 V
55/75451, 461, 471	NAND	AND	Internal	300 mA at 0.7 V
55/75452, 462, 472	AND	NAND	Internal	300 mA at 0.7 V
55/75453, 463, 473	NOR	OR	Internal	300 mA at 0.7 V
55/75454, 464, 474	OR	NOR	Internal	300 mA at 0.7 V

PARAMETER	55/75450 SERIES	55/75460 SERIES	55/75470 SERIES
Stand-off Voltage (V)	30	40	50
No Output Latch-up (V)	20	30	40

FUNCTIONAL SELECTION GUIDE FOR A/D AND D/A SYSTEMS

CURRENT SOURCES

μA722 10-Bit Current Source
9650 4-Bit Current Source

OPERATIONAL AMPLIFIER

μA772 High Slew Rate Op Amp

FUNCTIONAL SELECTION GUIDE FOR LED DRIVERS

SEGMENT DRIVERS: LED Segment Drivers interface MOS and TTL signals to LEDs. The currents can be set for low currents for continuous operation or higher currents for multiplex operation.

DIGIT DRIVERS: LED Digit Drivers are used for multiplex operation for selection of the digit to be turned on. MOS and/or TTL signals are used to select proper digit and each has high output current capability.

SEGMENT DRIVERS

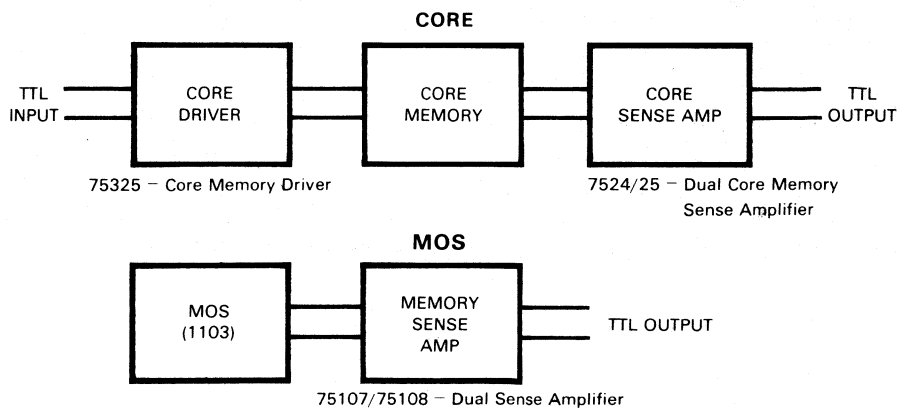
DEVICE NUMBER	INPUT COMPATIBILITY	BCD DECODER	NUMBER OF DRIVERS	MAXIMUM CURRENTS
75491	MOS	No	4	50 mA
9307	TTL	Yes	None	NA
9317	TTL	Yes	7	40 mA
9368	TTL	Yes	7	17 mA
9369	TTL	Yes	7	50 mA
9370	TTL	Yes	7	25 mA
9665*	TTL	No	7	350 mA, 50 V
9666/67*	MOS	No	7	350 mA, 50 V

DIGIT DRIVERS

DEVICE NUMBER	INPUT COMPATIBILITY	NUMBER OF DRIVERS	MAXIMUM CURRENT CAPABILITY
75492	MOS	4	V_{OUT} at I_{OUT} = 250 mA = 1.7 V Max

*To be announced

FUNCTIONAL SELECTION GUIDE FOR MEMORY SYSTEMS



TAPE AND DISC FILE AMPLIFIERS

μA733 Video Amplifier
μA739 Dual Low Noise Preamplifier

OPERATIONAL AMPLIFIERS SELECTION GUIDE BY DEVICE NUMBER

DEVICE NO.	TITLE	Input Offset Volt (mV) (Max)	Input Offset Volt Drift (μV/°C) (Max)	Input Offset Current (nA) (Max)	Input Bias Current (nA) (Max)	Common Mode Range (V)	Diff Input Volt (V)	Volt Gain (V/V)
μAF355	FET Input Op Amp	10.0	-	.05	.20	±10	±40	50 k
μAF355A	High Speed FET Input Op Amp	2.0	5	.01	.05	±11	±40	50 k
μAF356	FET Input Op Amp	10.0	-	.05	.20	±10	±40	50 k
μAF356A	High Speed FET Input Op Amp	2.0	5	.01	.05	±11	±40	50 k
μAF357	FET Input Op Amp	10.0	-	.05	.20	±10	±40	50 k
μAF357A	High Speed FET Input Op Amp	2.0	5	.01	.05	±11	±40	50 k
μA301A	General Purpose Op Amp	7.5	30	50	250	±12	±30	25 k
μA302	Voltage Follower	15	30	-	30	±10	-	0.9985
μA307	General Purpose Op Amp	7.5	30	50	250	±15	±30	25 k
μA308	Super Beta, Op Amp	7.5	30	1	7	±13.5	±0.5	15 k
μA308A	Super Beta, Op Amp	0.5	5	1	7	±13.5	±0.5	80 k
μA310	Voltage Follower	7.5	-	-	7	±10	-	0.999
μA702	Wide Band dc Amp	5.0	10	2000	7500	−4+0.5	±5	2 k
μA709	High Perf Op Amp	7.5	10	500	1500	±8	±5	15 k
μA715	High Speed Op Amp	7.5	6	250	1500	±10	±15	10 k
μA725	Instr Op Amp	2.5	5	35	125	±13.5	±22	250 k
μA725E	Instr Op Amp	0.5	2	5	75	±13.5	±22	1000 k
μA727	Temp Controlled Diff Amp	10	1.5	25	75	±12	±15	0.06 k
μA730	Differential Amp	5	-	3	16	±3.5	±5	0.1 k
μA739	Dual Low Noise Op Amp	6.0	-	1000	2000	±15	±5	6.5 k
μA740	FET Input Op Amp	100	-	0.3	2	±10	±30	25 k
μA741	Freq Comp Op Amp	6	-	200	500	±12	±30	20 k
μA741E	Freq Comp Op Amp	3	15	30	80	±12	±30	50 k
μA747	Dual Freq Comp Op Amp	6	-	200	500	±12	±30	20 k
μA747E	Dual Freq Comp Op Amp	3	-	200	500	±12	±30	20 k
μA748	High Perf Op Amp	6	-	200	500	±12	±30	20 k

NOTE: For temperature ranges and order information refer to specific data sheets and the Order Information Section.

OPERATIONAL AMPLIFIERS SELECTION GUIDE BY DEVICE NUMBER

Band-width $A_V = 1$ (MHz)	Output Current (mA) (Max)	Slew Rate $A_V = 1$ (V/μs)	Supply Min (V) (Typ)	Voltage Max (V) (Typ)	Supply Current (mA) (Max)	Compen-sation Compo-nents	MIL Grade Avail	Package(s)	Data Sheet Page No.
2.5	-	5	-	±22	4.0	0	X	TO-99	12-3
2.5	-	5	-	±22	4.0	0	X	TO-99	12-3
5.0	-	15	-	±22	10.0	0	X	TO-99	12-3
5.0	-	15	-	±22	7.0	0	X	TO-99	12-3
25.0	-	75	-	±22	10.0	0	X	TO-99	12-3
25.0	-	75	-	±22	7.0	0	X	TO-99	12-3
1.0	5.0	0.5	±3	±18	3	1	X	TO-99,6A,9T,6T	12-13
10.0	1.0	10	±12	±18	5.5	0	X	TO-99	12-20
1.0	5.0	0.5	±3	±18	3	0	X	TO-99,9T,6T	12-25
1.0	1.0	0.3	±5	±18	0.8	1	X	TO-99,6A,9T,6T	12-30
1.0	1.0	0.3	±2	±20	0.8	1	X	TO-99,6A	12-30
20.0	1.0	30	±5	±18	5.5	0	X	TO-99	12-20
30.0	3.5	3.5	+6–3	+14–7	6.7	2	X	TO-99,6A,3F	12-37
1.0	5.0	0.3	±9	±18	2.9	0	X	TO-99,6A,9A,3F	12-44
65.0	5.0	100	±6	±18	10	3	X	TO-100,6A	12-51
1.0	5.0	-	±3	±22	3	4	X	TO-99,9T,6T	12-57
1.0	5.0	-	±3	±22	3	4	X	TO-99,9T,6T	12-57
1.0	.001	-	±9	±18	5.7	2	X	TO-100,9T,6T	12-67
1.5	-	-	+6	+14	13	0	X	TO-99	12-71
10.0	6.0	0.5	±4	±18	14	3	X	9A,6A	12-77
3.0	5.0	6.0	±5	±22	8	0	X	TO-99	12-81
1.0	5.0	0.5	±5	±18	2.8	0	X	TO-99,6A,9A,3F,9T,6T	12-85
1.0	5.0	0.7	±5	±22	3.75	0	X	TO-99,6A,9A,3F	12-85
1.0	5.0	0.5	±5	±18	5.6	0	X	TO-100,6A	12-94
1.0	5.0	0.5	±5	±18	4.25	0	X	TO-100,6A	12-94
1.0	5.0	0.5	±5	±18	2.8	1	X	TO-99,6A,3F,9T	12-104

OPERATIONAL AMPLIFIERS SELECTION GUIDE BY DEVICE NUMBER

DEVICE NO.	TITLE	Input Offset Volt (mV) (Max)	Input Offset Volt Drift (μV/°C) (Max)	Input Offset Current (nA) (Max)	Input Bias Current (nA) (Max)	Common Mode Range (V)	Diff Input Volt (V)	Volt Gain (V/V)
μA749	Dual Low Noise Op Amp	6.0	-	500	1000	±15	±5	15 k
μA776	Multi-Purpose Prog Op Amp (I_{SET} = 15 mA)	6	-	25	50	±10	±30	50 k
μA776	Multi-Purpose Prog Op Amp (I_{SET} = 1.5 mA)	6	-	6	10	±10	±30	50 k
μA777	Precision Op Amp	7.5	-	50	250	±12	±30	25 k
μA791	Power Operational Amp	6.0	-	200	500	±12	±30	20 k
μA798	Dual Op Amp (Int Comp)	6.0	-	100	−500	$+13-V_S$	±30	20 k
μA799	Int Comp Op Amp	6.0	-	100	−500	$+13-V_S$	±30	20 k
μA1458	Internally Comp Dual Op Amp	6	-	200	500	±12	±30	20 k
μA3401	Quad Single Supply Amp	-	-	-	300	-	-	1 k
μA3403	Quad Op Amp	8	-	50	−500	$+13-V_S$	±30	25 k
μA4136	Quad Op Amp	6.0	-	200	500	±15	±30	20 k

NOTE: For temperature ranges and order information refer to specific data sheets and the Order Information Section.

OPERATIONAL AMPLIFIERS SELECTION GUIDE
BY DEVICE NUMBER

Bandwidth $A_V = 1$ (MHz)	Output Current (mA) (Max)	Slew Rate $A_V = 1$ (V/μs)	Supply Min (V) (Typ)	Voltage Max (V) (Typ)	Supply Current (mA) (Max)	Compensation Components	MIL Grade Avail	Package(s)	Data Sheet Page No.
10.0	6.0	0.5	±4	±18	14	3	X	9A,6A	12-112
1.0	2.0	0.8	±1.2	±18	0.19	1	X	TO-99,6A,9T,6T	12-120
0.2	0.12	0.1	±1.2	±18	0.03	1	X	TO-99,6A,9T,6T	12-120
1.0	5.0	0.5	±5	±20	2.8	1	X	TO-99,6A,3F,9T,6T	12-129
1.0	1000	0.5	±5	±18	25	4		Mul-L TO-3,9W,5H	12-135
1.0	6.0	0.6	+1.5(3)	+18(36)	4	0	X	9T,6T,5S	12-141
1.0	6.0	0.6	+1.5(3)	+18(36)	4	0	X	9T,6T,5S	12-147
1.0	5.0	0.5	±5	±18	2.9	0	X	TO-99,9T,6T	12-153
5.0	10.0	0.6	±2(4)	±9(18)	10	0		9A,6A	12-159
1.0	5.0	0.6	+1.5(3)	+18(36)	7	0	X	9A,6A	12-166
3.0	5.0	1.0	±5	±18	12	0	X	9A,6A	12-173

SPECIAL FUNCTIONS SELECTION GUIDE BY DEVICE NUMBER

Arrays

DEVICE NO.	Function	Balanced Input	Balanced Output	Low Noise	AGC Capability	Multiple Unit	Wide Band	Switching Application	BV_{CBO} (V)	BV_{CEO} (V)	BV_{EBO} (V)	I_C (mA)	Diode Matching (mV)	Reverse (ns) Recovery Time	Package(s)	Operating Temperature Range	Data Sheet Page No.
μA726C	Temp. Controlled Diff. Pair Trans	●	●	●					40	30	5	5			5U	0°C to 85°C	13-13
μA3018	Darlington Conn. Pair Plus Two Ind. Trans.	●	●		●	●	●		20	15	5	50			5G	−55°C to +125°C	13-50
μA3018A	Darlington Conn. Pair Plus Two Ind. Trans.	●	●		●	●	●		20	15	5	50			5G	−55°C to +125°C	13-50
μA3019	Ind. Diode							●					1		5E	−55°C to +125°C	13-50
μA3026	Dual Independent Diff. Trans.								20	15	5	50			5G	0°C to 85°C	13-50
μA3036	Dual Darlington Conn. Trans.	●	●	●		●			30	15	5	50			5E	−55°C to +125°C	13-50
μA3039	Quad Plus Two Diodes							●					1	1	5G	−55°C to +125°C	13-50
μA3045	Diff. Conn. Pair Plus Three Ind. Trans.	●	●			●	●		20	15	5	50			6A	−55°C to +125°C	13-50
μA3046	Diff. Conn. Pair Plus Three Ind. Trans.	●	●			●	●		20	15	5	50			6A	0°C to +85°C	13-50
μA3054	Dual Independent Diff. Trans.					●			20	15	5	50			6A	−55°C to +125°C	13-50
μA3086	Diff. Conn. Pair Plus Three Ind. Trans.	●	●			●	●		20	15	5	50	1		6A	−40°C to +85°C	13-50

Note: For temperature ranges and order information refer to the Order Information Section and specific data sheets.

SPECIAL FUNCTIONS SELECTION GUIDE
BY FUNCTION OR SYSTEM USE

Function/System Use	DEVICE NO.	Data Sheet Page No.
AC Power Controller	μA742	13-22
A to D Converter	μA2240	13-38
Amplifier		
AGC	μA757	13-28
Gained Controlled IF	μA757	13-28
Limiting	μA757	13-28
Luminance	μA733	13-16
Video	μA733	13-16
Counter/Timer	μA2240	13-38
Frequency Doubler	μA796	13-34
Frequency Synthesizer	μA2240	13-38
Generator, Staircase	μA2240	13-38
IF Mixer	μA757	13-28
IF Modulator	μA757	13-28
Modulator/Demodulator	μA796	13-34
Motor Speed Controller	μA7391	13-83
Multiplexer/Demultiplexer		
Dual 4-Channel	F4052/34052	13-76
8-Channel	F4051/34051	13-73
Preamplifier, Tape-Disc	μA733	13-16
Sample and Hold, Digital	μA2240	13-38
Switches	μA796	13-34
	F4051/34051	13-73
	F4052/34052	13-76
Quad Bilateral	F4016/34016	13-70
	F4066/34066	13-79
Tachometer Time Base	μA2240	13-38
Thyristor and SCR Controller	μA742	13-22
Timer	μA555	13-3
	μA2240	13-38
Dual	μA556	13-8
Trigger (TRIGAC)	μA742	13-22

Note: For temperature ranges and order information, refer to specific data sheets and the order information section.

VOLTAGE REGULATOR SELECTION GUIDE
BY DEVICE NUMBER

DEVICE NO.	Function and Polarity	Input Voltage Range (V)	Output Voltage Range (V)	Output Current Max (A)	Output Current Peak (A)	Line Regulation (%)	Load Regulation (%)	Quiescent Current (mA)	Ripple Rejection Min (dB)	Dropout Voltage Min (V)	Avg. Temp. Coefficient (mV/°C)	MAX θ_{JC} (°C/W)	MAX θ_{JA} (°C/W)	Package(s)	Data Sheet Page No.
μA304	Neg. Adj.	−40 −9.5	−30 0	.020	-	0.1	0.2	5.0	60	3.0	1.0	40	190	TO-100	14-3
μA305	Pos. Adj.	8.0 40	4.5 30	.020	-	.060	.050	2.0	60	3.0	1.0	- 40	190 190	9T TO-99	14-8
μA309	3-Term. 5 V	7.0 35	4.8 5.2	1.0	2.2	2.0	2.0	5.0	-	2.0	−0.8	5.0 5.5	65 45	TO-220 TO-3	14-18
μA376	Pos. Adj.	9.0 40	5.0 37	.025	-	.050	0.2	2.5	-	3.0	1.0	-	190	9T	14-8
μA723	Precision	9.5 40	2.0 37	.125	.150	0.1	0.6	2.3	74	3.0	.015	40 -	190 160	TO-100 9A, 6A	14-21
μA7805	3-Term. Pos.	7.0 35	4.8 5.2	1.0	2.2	1.0	1.0	4.2	62	2.0	−1.1	5.0 5.5	65 45	TO-220 TO-3	14-44
μA7806	3-Term. Pos.	8.0 35	5.75 6.25	1.0	2.2	1.0	1.0	4.3	59	2.0	−0.8	5.0 5.5	65 45	TO-220 TO-3	14-44
μA7808	3-Term. Pos.	10 35	7.7 8.3	1.0	2.2	1.0	1.0	4.3	56	2.0	−0.8	5.0 5.5	65 45	TO-220 TO-3	14-44
μA7885 (8.5 V)	3-Term. Pos.	10.5 35	8.2 8.8	1.0	2.2	1.0	1.0	4.3	54	2.0	−1.0	5.0 5.5	65 45	TO-220 TO-3	14-44
μA7812	3-Term. Pos.	14 35	11.5 12.5	1.0	2.2	1.0	1.0	4.3	55	2.0	−1.0	5.0 5.5	65 45	TO-220 TO-3	14-44
μA7815	3-Term. Pos.	17 35	14.4 15.6	1.0	2.2	1.0	1.0	4.4	54	2.0	−1.0	5.0 5.5	65 45	TO-220 TO-3	14-44
μA7818	3-Term. Pos.	20 35	17.3 18.7	1.0	2.2	1.0	1.0	4.5	53	2.0	−1.0	5.0 5.5	65 45	TO-220 TO-3	14-44
μA7824	3-Term. Pos.	26 40	23 25	1.0	2.2	1.0	1.0	4.6	50	2.0	−1.5	5.0 5.5	65 45	TO-22 TO-3	14-44
μA78G	Pos. Adj.	7.5 4.0	5.0 30	1.0	2.2	.75	1.0	3.2	62	2.5	−0.5	11 6.0	80 47	8Z TO-3	14-28
78H05	5 A Pos.	8.5 20	4.8 5.5	5	7	1.0	1.0	Max 10	60	3.5	-	2.0	40	TO-3	14-102
μA78L26 (2.6 V)	3-Term. Pos.	4.3 30	2.5 2.7	0.15	-	2.0	1.0	3.6	51	1.7	-	40 -	190 180	TO-39 TO-92	14-57

Note: All values are typical unless otherwise indicated. Only commercial part numbers are listed. Military, automotive and industrial temperature range devices are available upon request. Refer to specific data sheet for details.

VOLTAGE REGULATOR SELECTION GUIDE
BY DEVICE NUMBER

DEVICE NO.	Function and Polarity	Input Voltage Range (V)	Output Voltage Range (V)	Output Current Max (A)	Output Current Peak (A)	Line Regulation (%)	Load Regulation (%)	Quiescent Current (mA)	Ripple Rejection Min (dB)	Dropout Voltage Min (V)	Avg. Temp. Coefficient (mV/°C)	MAX θ_{JC} (°C/W)	MAX θ_{JA} (°C/W)	Package(s)	Data Sheet Page No.
μA78L05	3-Term. Pos.	6.7 30	4.8 5.2	0.15	-	2.0	1.0	3.8	49	1.7	-	40 -	190 180	TO-39 TO-92	14-57
μA78L62 (6.2 V)	3-Term. Pos.	7.7 30	5.95 6.45	0.15	-	2.0	1.0	3.9	46	1.7	-	40 -	190 180	TO-39 TO-92	14-57
μA78L82 (8.2 V)	3-Term. Pos.	9.9 30	7.9 8.5	0.15	-	2.0	1.0	4.0	44	1.7	-	40 -	190 180	TO-39 TO-92	14-57
μA78L12	3-Term. Pos.	13.7 35	11.5 12.5	0.15	-	2.0	1.0	4.2	42	1.7	-	40 -	190 180	TO-39 TO-92	14-57
μA78L15	3-Term. Pos.	16.7 35	14.4 15.6	0.15	-	2.0	1.0	4.4	39	1.7	-	40 -	190 180	TO-39 TO-92	14-57
μA78L18*	3-Term. Pos.	19.7 35	17.3 18.9	0.15	-	2.0	1.0	4.6		1.7	-	40 -	190 180	TO-39 TO-92	14-57
μA78L24*	3-Term. Pos.	25.7 35	23.1 24.9	0.15	-	2.0	1.0	4.8		1.7	-	40 -	190 180	TO-39 TO-92	14-57
μA78M05	3-Term. Pos.	7.0 30	4.8 5.2	0.5	0.75	1.0	1.0	4.2	78	2.0	−1.0	5.0 25	70 185	TO-220 TO-39	14-66
μA78M06	3-Term. Pos.	8.0 30	5.75 6.25	0.5	0.75	1.0	1.0	4.3	75	2.0	−0.5	5.0 25	70 185	TO-220 TO-39	14-66
μA78M08	3-Term. Pos.	10 30	7.7 8.3	0.5	0.75	1.0	1.0	4.3	72	2.0	−0.5	5.0 25	70 185	TO-220 TO-39	14-66
μA78M12	3-Term. Pos.	14 35	11.5 12.5	0.5	0.75	1.0	1.0	4.3	71	2.0	−1.0	5.0 25	70 185	TO-220 TO-39	14-66
μA78M15	3-Term. Pos.	17 35	14.4 15.6	0.5	0.75	1.0	1.0	4.4	70	2.0	−1.0	5.0 25	70 185	TO-220 TO-39	14-66
μA78M20	3-Term. Pos.	22 40	19.0 21.0	0.5	0.75	1.0	1.0	4.5	69	2.0	−1.1	5.0 25	70 185	TO-220 TO-39	14-66
μA78M24	3-Term. Pos.	26 40	23 25	0.5	0.75	1.0	1.0	4.6	66	2.0	−1.2	5.0 25	70 185	TO-220 TO-39	14-66
μA78MG	Pos.Adj.	7.5 40	5.0 30	0.5	0.8	.75	1.0	2.8	78	2.5	−0.5	25 11 12	185 80 80	TO-39 9V 8Z	14-36
μA7905	3-Term. Neg.	−7.2 −35	−4.8 −5.2	1.0	2.1	1.0	1.0	1.0	54	2.0	−0.4	5.5 5.0	45 65	TO-3 TO-220	14-78
μA7952	3-Term. Neg.	−7.4 −35	−5.0 −5.4	1.0	2.1	1.0	1.0	1.0	54	2.0	−0.4	5.5 5.0	45 65	TO-3 TO-220	14-78

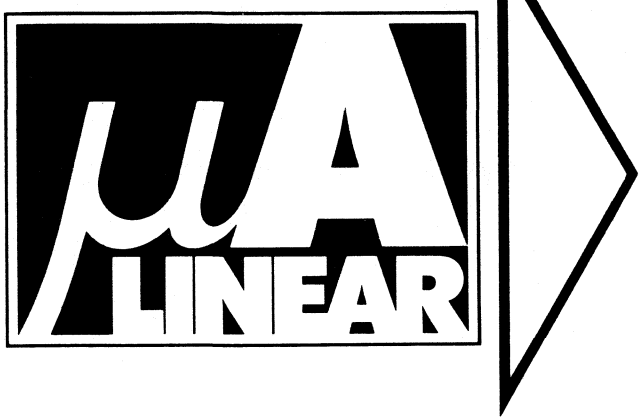
*Introduction 1st Qtr., 1976

Note: All values are typical unless otherwise indicated. Only commercial part numbers are listed. Military, automotive and industrial temperature range devices are available upon request. Refer to specific data sheet for details.

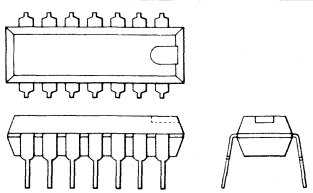
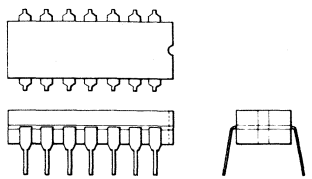
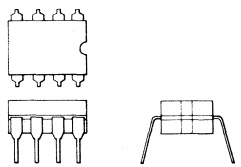
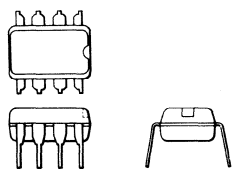
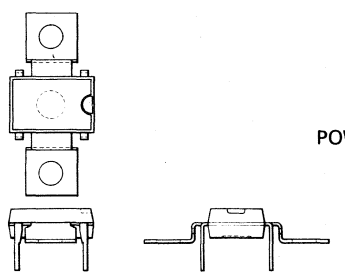
VOLTAGE REGULATOR SELECTION GUIDE
BY DEVICE NUMBER

DEVICE NO.	Function and Polarity	Input Voltage Range (V)	Output Voltage Range (V)	Output Current Max (A)	Output Current Peak (A)	Line Regulation (%)	Load Regulation (%)	Quiescent Current (mA)	Ripple Rejection Min (dB)	Dropout Voltage Min (V)	Avg. Temp. Coefficient (mV/°C)	MAX θ_{JC} (°C/W)	MAX θ_{JA} (°C/W)	Package(s)	Data Sheet Page No.
μA7906	3-Term. Neg.	−8.3 −35	−5.75 −6.25	1.0	2.1	1.0	1.0	1.0	54	2.0	−0.4	5.5 5.0	45 65	TO-3 TO-220	14-78
μA7908	3-Term. Neg.	−10.3 −35	−7.7 −8.3	1.0	2.1	1.0	1.0	1.0	54	2.0	−0.6	5.5 5.0	45 65	TO-3 TO-220	14-78
μA7912	3-Term. Neg.	−14.5 −35	−11.5 −12.5	1.0	2.1	1.0	1.0	1.0	54	2.0	−0.8	5.5 5.0	45 65	TO-3 TO-220	14-78
μA7915	3-Term. Neg.	−17.6 −35	−14.4 −15.6	1.0	2.1	1.0	1.0	1.0	54	2.0	−1.0	5.5 5.0	45 65	TO-3 TO-220	14-78
μA7918	3-Term. Neg.	−20.7 −35	−17.3 −18.7	1.0	2.1	1.0	1.0	1.0	54	2.0	−1.0	5.5 5.0	45 65	TO-3 TO-220	14-78
μA7924	4-Term. Neg.	−27 −40	−23.0 −25.0	1.0	2.1	1.0	1.0	1.0	54	2.0	−1.0	5.5 5.0	45 65	TO-3 TO-220	14-78
μA79G	Adj. Neg.	−7.0 −40	−2.23 −30	1.0	2.2	1.0	1.0	0.5	50	2.3	0.4	11 6.0	80 47	TO-202 TO-3	14-28
μA79M05	Fixed Neg.	−7.5 −35	−5.2 −4.8	0.5	.65	1.0	1.0	1.0	60	1.0	−0.4	5.0 25	70 185	TO-220 TO-39	14-90
μA79M06	Fixed Neg.	−7.35 −35	−6.25 −5.75	0.5	.65	1.0	1.0	1.0	60	1.0	−0.4	5.0 25	70 185	TO-220 TO-39	14-90
μA79M08	Fixed Neg.	−9.4 −35	−8.3 −7.7	0.5	.65	1.0	1.0	1.0	60	1.0	−0.6	5.0 25	70 185	TO-220 TO-39	14-90
μA79M12	Fixed Neg.	−13.6 −35	−12.5 −11.5	0.5	.65	1.0	1.0	1.0	60	1.0	−0.8	5.0 25	70 185	TO-220 TO-39	14-90
μA79M15	Fixed Neg.	−16.7 −35	−15.6 −14.4	0.5	.65	1.0	1.0	1.0	60	1.0	−1.0	5.0 25	70 185	TO-220 TO-39	14-90
μA79M20	Fixed Neg.	−22.1 −40	−20.0 −19.0	0.5	.65	1.0	1.0	1.0	59	1.0	−1.0	5.0 25	70 185	TO-220 TO-39	14-90
μA79M24	Fixed Neg.	−26.1 −40	−25 −23	0.5	.65	1.0	1.0	1.0	58	1.0	−1.0	5.0 25	70 185	TO-220 TO-39	14-90
μA79MG	Adj. Neg.	−7.0 −40	−2.2 −30	0.5	.65	.75	1.0	0.5	60	2.3	−0.4	25 11 12	185 80 80	TO-39 9V 8Z	14-36

Note: All values are typical unless otherwise indicated. Only commercial part numbers are listed. Military, automotive and industrial temperature range devices are available upon request. Refer to specific data sheet for details.



INDUSTRY PACKAGE CROSS REFERENCE

	Fairchild	NSC	Signetics	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 PLASTIC DIP VARIATIONS	P	N	A, B	P	N		N		
 CERAMIC DIP (14 or 16-Lead)	D	D	I	L		D	D	D	D, M
 CERAMIC MINI DIP	R	J		L	J				DC, DD
 PLASTIC MINI DIP	T	N	V	P	P	E	M	PC	N, DN, DP, MP
 POWER MINI DIP	T2								

INDUSTRY PACKAGE CROSS REFERENCE (Cont'd)

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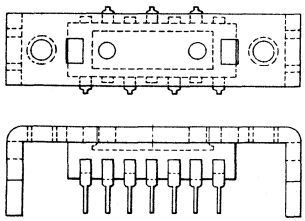
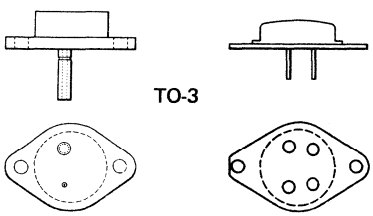
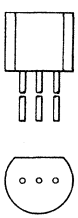
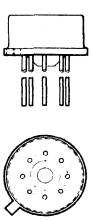
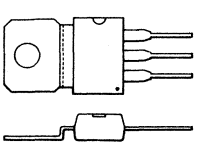
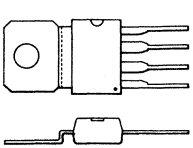
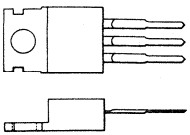
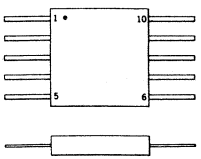
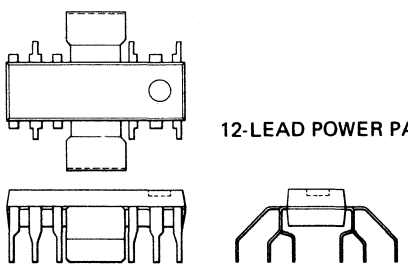
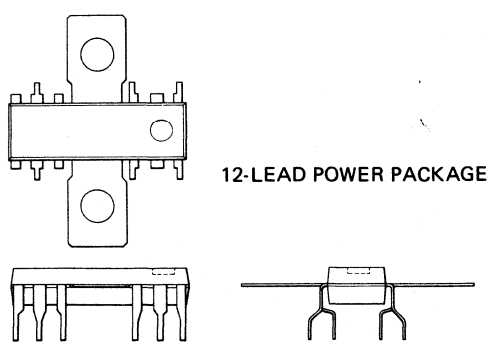
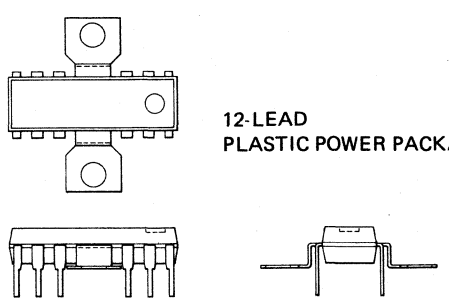
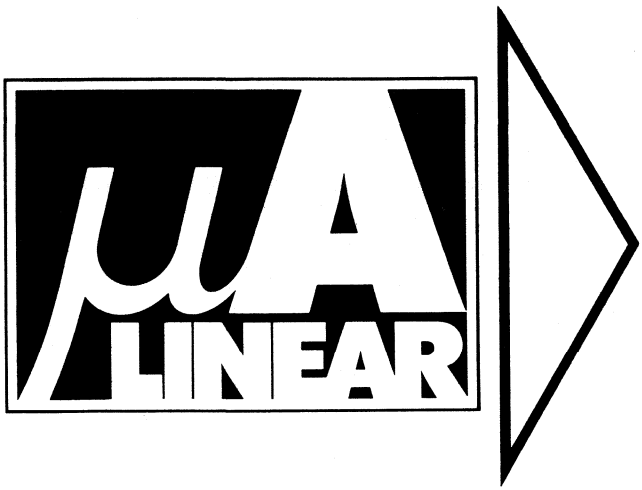
 POWER DIP	BP	S							
 TO-3 4-LEAD TO-3 TYPE	K	K	DA	K			K		K, LK, TK
 PLASTIC TO-92	W	Z		G					
 TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	S, V1	T	H	T, H
 3-LEAD POWER TAB	U1	P							
 4-LEAD POWER TAB	U1								

INDUSTRY PACKAGE CROSS REFERENCE (Cont'd)

	Fairchild	NSC	Signetics	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 TO-220	U	T							
 FLATPAK VARIATIONS	F	F, W	Q	F	F, S, W	K	F	F, FM	J, F, Q
 12-LEAD POWER PACKAGE	P3				ND	Q			
 12-LEAD POWER PACKAGE	P4					QM			
 12-LEAD PLASTIC POWER PACKAGE	P5								

4



LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
AM1489APC		9617PC
AM1489PC		9617PC
AM2614DC		9614DC
AM2614DM		9614DM
AM2614FM		9614FM
AM2615DC		9615DC
AM2615DM		9615DM
AM2615FM		9615FM
AM2615PC		9615PC
AM685DL		μA760DC
AM685DM		μA760DM
AM685HL		μA760HC
AM685HM		μA760HM
AM9616PC	9616DC	
CA3002T		μA703HC
CA3004T		μA703HC
CA3005T		μA703HC
CA3006T		μA703HC
CA3008		μA741FM
CA3008A		μA741FM
CA3010		μA741HM
CA3010A		μA741HM
CA3011T		μA753TC
CA3012T		μA753TC
CA3013T		μA753TC
CA3014T		μA753TC
CA3015		μA741HM
CA3015A		μA741HM
CA3016		μA741FM
CA3016A		μA741FM
CA3018	μA3018HM	
CA3018A	μA3018AHM	
CA3019	μA3019HM	
CA3021T		μA757PC
CA3022T		μA757PC
CA3023T		μA757PC
CA3026	μA3026HM	
CA3028AT		μA703HC
CA3028T		μA703HC
CA3029		μA741TC
CA3029A		μA741TC
CA3030		μA741TC
CA3030A		μA741TC
CA3036	μA3036HM	
CA3037		μA741DM
CA3037A		μA741DM
CA3038		μA741DM
CA3038A		μA741DM
CA3039	μA3039HM	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3041E		μA3065PC
CA3042E		μA3065PC
CA3043T		μA3065PC
CA3044T	μA3064HC	
CA3045	μA3045DM	
CA3046	μA3046DC	
CA3054	μA3054DC	
CA3058E		μA742DC
CA3059		μA742DC
CA3059E		μA742DC
CA3064E	μA3064PC	
CA3064T	μA3064HC	
CA3065E	μA3065PC	
CA3066E	μA3066PC	
CA3070E	μA780PC	
CA3071E	μA781PC	
CA3072E	μA746PC	
CA3075E	μA3075PC	
CA3078AS		μA776DM
CA3078AT		μA776HM
CA3078S		μA776TC
CA3078T		μA776HC
CA3079		μA742DC
CA3085		μA723HC
CA3085A		μA723HC
CA3085AF		μA723DC
CA3085AS		μA723DC
CA3085B		μA723HM
CA3085BF		μA723DM
CA3085BS		μA723DC
CA3085F		μA723DC
CA3085S		μA723DC
CA3086	μA3086DC	
CA3088E		μA720PC
CA3089E	μA3089E	
CA3090E		μA758PC
CA3126Q	μA787PC	
CA3458S	μA1458TC	
CA3458T	μA1458HC	
CA3558S		μA1558HM
CA3558T	μA1558HM	
CA3741CS	μA741TC	
CA3741CT	μA741HC	
CA3741S		μA741HM
CA3741T	μA741HM	
CA3747CE	μA747PC	
CA3747CF		μA747DC
CA3747CT	μA747HC	
CA3747E	μA747DM	
CA3747F	μA747DM	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3747T	μA747HM	
CA3748CS	μA748TC	
CA3748CT	μA748HC	
CA3748S		μA748HM
CA3748T	μA748HC	
CA758E	μA758PC	
DM55121J	55121DM*	
DM55122J	55122DM*	
DM75121J	75121DC*	
DM75121N	75121PC*	
DM75122J	75122DC*	
DM75122N	75122PC*	
DM75123J	75123DC*	
DM75123N	75123PC*	
DM75124J	75124DC*	
DM75124N	75124PC*	
DM75491N	75491PC	
DM75492N	75492PC	
DM7820AD		9615DM
DM7820J		9615DM
DM7820N		9615DM
DM7820W		9615FM
DM7822J		9617DM
DM7830J		9614DM
DM7830W		9614FC
DM8820AN		9615DM
DM8820J		9615DM
DM8820N		9615PC
DM8820W		9615FM
DM8822J		9617DC
DM8822N		9617PC
DM8830J		9614DM
DM8830N		9614DM
DM8830W		9614FM
D555CJ		μA556PC
LF111	μAF111	
LF211	μAF211	
LF311	μAF311	
LF155	μAF155HM	
LF155A	μAF155AHM	
LF156	μAF156HM	
LF156A	μAF156AHM	
LF157	μAF157HM	
LF157A	μAF157AHM	
LF355	μAF355HC	
LF355A	μAF355AHC	
LF356	μAF356HC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LF356A	μAF356AHC	
LF357	μAF357HC	
LF357A	μAF357AHC	
LH0021CK		μA791KC
LH0021G/883		μA791KMQB
LH0021K		μA791KM
LH0061C		μA791KC
LH0061CK		μA791KM
LH0061K		μA791KM
LM101AD	μA101ADM	
LM101AF	μA101AFM	
LM101AH	μA101AHM	
LM101D	μA101DM	
LM101H	μA101HM	
LM102H	μA102HM	
LM104H	μA104HM	
LM105H	μA105HM	
LM106F		μA710FM
LM106H		μA710HM
LM107H	μA107HM	
LM108AD	μA108ADM	
LM108AF	μA108AFM	
LM108AH	μA108AHM	
LM108D	μA108DM	
LM108F	μA108FM	
LM108H	μA108HM	
LM111H	μA111HM	
LM120H-05		μA79M05HM
LM120H-12		μA79M12HM
LM120H-15		μA79M15HM
LM120K-05		μA7905KM*
LM120K-12		μA7912KM*
LM124D	μA124DM*	μA3503DM
LM1303N		μA749PC
LM1304N	μA732PC	
LM1307N	μA767PC	
LM139	μA139DM	
LM139A	μA139ADM	
LM139D	μA775DM	
LM139F	μA775FM	
LM1414J		μA711DC
LM1458H	μA1458HC	
LM1458N	μA1458TC	
LM1488J		9616DC
LM1489AJ		9617DC
LM1489J		9617DC
LM1496H	μA796HC	
LM1514J		μA711DM

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM1558H	μA1558HM	
LM160H	μA760HM	
LM1800N	μA758PC	
LM1820N	μA720PC	
LM1829N	μA787PC	
LM1841N	μA2136PC	
LM201AF	μA201AFM	
LM201AH	μA201AHM	
LM201D	μA201DM	
LM201H	μA201HM	
LM202H	μA202HM	
LM204H	μA204HM***	
LM205H	μA205HM***	
LM206F		μA710FM
LM206H		μA710HC
LM207H	μA207HM	
LM208AD	μA208ADM	
LM208AF	μA208AFM	
LM208AH	μA208AHM	
LM208D	μA208DM	
LM208F	μA208FM	
LM208H	μA208HM	
LM220H-05		μA79M05HM
LM220H-12		μA79M12HM
LM220H-15		μA79M15HM
LM220K-05		μA7905KM*
LM220K-12		μA7912KM*
LM220K-15		μA7915KM*
LM222N		μA555TC
LM224D		μA3503DM
LM2900N	μA2900PC**	
LM2901N	μA2901PC**	μA775PC
LM2902N	μA2902PC**	
LM2905N		μA555TC
LM301AD	μA301ADC	
LM301AH	μA301AHC	
LM301AN	μA301ATC	
LM3018AH	μA3018AHM	
LM3018H	μA3018HM	
LM3019H	μA3019HM	
LM302H	μA302HC	
LM3026H	μA3026HM	
LM3039H	μA3039HM	
LM304H	μA304HC	
LM3045D	μA3045DM	
LM3046N	μA3046DC	
LM305AH	μA305AHC	
LM305H	μA305HC	
LM3053N	μA753TC	
LM3054N	μA3054DC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM306H		μA710HC
LM3064H	μA3064HC	
LM3065N	μA3065PC	
LM3066N	μA3066PC	
LM3067N	μA3067PC	
LM307H	μA307HC	
LM307N	μA307TC	
LM3070N	μA780DC	
LM3075N	μA3075E	
LM308AD	μA308ADC	
LM308AH	μA308AHC	
LM308D	μA308DC	
LM308H	μA308HC	
LM308N	μA308TC	
LM3086N	μA3086DC	
LM311H	μA311HC	
LM311N	μA311TC	
LM320H-05		μA79M05HC
LM320H-12		μA79M12HC
LM320H-15		μA79M15HC
LM320K-05		μA7905KC
LM320K-12		μA7912KC
LM320K-15		μA7915KC
LM320T-12		μA7912UC
LM320T-15		μA7915UC
LM320T-18		μA7918UC
LM320T-24		μA7924UC
LM320T-5		μA7905UC
LM320T-6		μA7906UC
LM320T-8		μA7908UC
LM323K	SH0323K	
LM324D	μA324DC*	μA3403DC
LM324N	μA324PC*	μA3403PC
LM339A	μA339ADC*	
LM339D	μA775DC	
LM339N	μA775PC	
LM340K-05	μA7805KC	
LM340K-06	μA7806KC	
LM340K-08	μA7808KC	
LM340K-12	μA7812KC	
LM340K-15	μA7815KC	
LM340K-18	μA7818KC	
LM340K-24	μA7824KC	
LM340T-05	μA7805UC	
LM340T-06	μA7806UC	
LM340T-08	μA7808UC	
LM340T-12	μA7812UC	
LM340T-15	μA7815UC	
LM340T-18	μA7818UC	
LM340T-24	μA7824UC	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM350N		75453BPC
LM351N	75453BPC	
LM360H	μA760HC	
LM376N	μA376TC	
LM380N		TBA641A12
LM381AN	μA739DC	
LM381N		μA739PC
LM382N		μA739PC
LM387N		μA739PC
LM388N		TBA641A12
LM3900N	μA3900PC**	
LM3905N		μA555TC
LM4250CH		μA776HC
LM4250CN		μA776DC
LM4250H		μA776HM
LM55107AJ	55107ADM	
LM55108AJ	55108ADM	
LM55109J	55109DM	
LM55110J	55110DM	
LM5524J	5524DM	
LM5525J	5525DM	
LM5528J	5528DM	
LM5529J	5529DM	
LM5534J	5534DM	
LM5535J	5535DM	
LM555CN	μA555TC	
LM556CN	μA556PC	
LM703LH	μA703HC	
LM709AH	μA709AHM	
LM709CH	μA709HC	
LM709CN	μA709PC	
LM709H	μA709HM	
LM710CH	μA710HC	
LM710CN	μA710PC	
LM710H	μA710HM	
LM711CH	μA711HC	
LM711CN	μA711PC	
LM711H	μA711HM	
LM723CD	μA723DC	
LM723CH	μA723HC	
LM723CN	μA723PC	
LM723D	μA723DM	
LM723H	μA723HM	
LM725AH	μA725AHM	
LM725CH	μA725HC	
LM725H	μA725HM	
LM733CD	μA733DC	
LM733CH	μA733CH	
LM733CN	μA733PC	
LM733D	μA733DM	
LM733H	μA733HM	
LM741CD	μA741DC	
LM741CH	μA741HC	
LM741CN-08	μA741TC	
LM741CN-14	μA741PC	
LM741F	μA741FM	
LM741H	μA741HM	
LM746N	μA746PC	
LM747CD	μA747DC	
LM747CH	μA747HC	
LM747CN	μA747PC	
LM747D	μA747DM	
LM747H	μA747HM	
LM748CH	μA748HC	
LM748CN	μA748TC	
LM748H	μA748HM	
LM75107AJ	75107ADC	
LM75107AN	75107APC	
LM5108AJ	75108ADC	
LM75108AN	75108APC	
LM75109J	75109DC	
LM75109N	75109PC	
LM75110J	75110DC	
LM75110N	75110PC	
LM75150J	75150DC**	
LM75150N	75150PC**	9616DC
LM75154J	75154DC**	9617DC
LM75154N	75154PC**	
LM75207J	75207DC	
LM75207N	75207PC	
LM75208J	75208DC	
LM75208N	75208PC	
LM7524J	7524DC	
LM7524N	7524PC	
LM7525J	7525DC	
LM7525N	7525PC	
LM7528J	7528DC	
LM7528N	7528PC	
LM7529J	7529DC	
LM7529N	7529PC	
LM75325J	75325DC	
LM75325N	75325PC	
LM7534J	7534DC	
LM7534N	7534PC	
LM7535J	7535DC	
LM7535N	7535PC	
LM75450J	75450BDC	
LM75450N	75450BPC	
LM75451N	75451BTC	
LM75452N	75452BTC	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM75453N	75453BTC	
LM75454N	75454BTC	
MC1303P		μA749PC
MC1304P	μA732PC	
MC1305P		μA732PC
MC1307P	μA767PC	
MC1310P		μA758PC
MC1311P	μA758PC	
MC1312P	μA1312PC	
MC1324P		μA746PC
MC1326P		μA746PC
MC1328P		μA746PC
MC1339P		μA749PC
MC1350P		μA757PC
MC1351P		μA3065PC
MC1352P		μA757PC
MC1353P		μA757PC
MC1355P		μA3065PC
MC1357P	μA2136PC	
MC1358P	μA3065PC	
MC1364P	μA3064PC	
MC1370P	μA780PC	
MC1371P	μA781PC	
MC1375P	μA3075PC	
MC1391P	μA1391TC	
MC1394P	μA1394TC	
MC1398P		μA787PC
MC1410G		μA733HC
MC1414L		μA711DC
MC1414P		μA711PC
MC1420G		μA733HC
MC1435G		μA749DHC
MC1435L		μA749DC
MC1437L		μA749DC
MC1437P		μA749PC
MC1438R		μA791KC
MC1455P1	μA555TC	
MC1456CG		μA776HC
MC1456CL		μA776DC
MC1456G		μA776HC
MC1456L		μA776DC
MC1458CG	μA1458CHC	
MC1458CP1	μA1458CTC	
MC1458G	μA1458HC	
MC1458P1	μA1458TC	
MC1460G		μA78MGHC
MC1460R		μA78MGHC
MC1461G		μA78MGHC
MC1461R		μA78MGHC
MC1463G		μA79MGHC
MC1463R		μA79MGHC
MC1466L		μA723DC
MC1469G		μA78MGHC
MC1469R		μA78MGHC
MC1488L		9616DM
MC1489AL		9617DM
MC1489L		9617DM
MC1496G	μA796HC	
MC1510F		μA733FM
MC1510G		μA733HM
MC1514F		μA711FM
MC1514L		μA711DM
MC1520G		μA733HM
MC1535G		μA749HM
MC1535L		μA749DM
MC1537L		μA749DM
MC1550G		μA757DC
MC1556G		μA776HM
MC1556L		μA776DM
MC1558G	μA1558HM	
MC1560G		μA78M00HM
MC1560R		μA7800KM
MC1561G		μA78MGHM
MC1561R		μA78MGHM
MC1563G		μA79MGHM
MC1563R		μA79MGHM
MC1566L		μA723DM
MC1569G		μA78MGHM
MC1569R		μA78GKM
MC1590		μA757DC
MC1596G	μA796HC	
MC1709CG	μA709HC	
MC1709CL	μA709DC	
MC1709CP1	μA709TC	
MC1709CP2	μA709PC	
MC1709F	μA709FM	
MC1709G	μA709HM	
MC1709L	μA709DM	
MC1710CG	μA710HC	
MC1710CL	μA710DC	
MC1710CP	μA710PC	
MC1710F	μA710FM	
MC1710G	μA710HM	
MC1710L	μA710DM	
MC1711CG	μA711HC	
MC1711CL	μA711DC	

5

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC1711CP	μA711PC	
MC1711F	μA711FM	
MC1711G	μA711HM	
MC1711L	μA711DM	
MC1712CG	μA702HC	
MC1712CL	μA702DC	
MC1712F	μA702FM	
MC1712L	μA702DM	
MC1723CG	μA723HC	
MC1723CL	μA723DC	
MC1723G	μA723HM	
MC1723L	μA723DM	
MC1741CG	μA741HC	
MC1741CL	μA741DC	
MC1741CP1	μA741TC	
MC1741CP2	μA741PC	
MC1741F	μA741FM	
MC1741G	μA741HM	
MC1741L	μA741DM	
MC1747CG	μA747HC	
MC1747CL	μA747DC	
MC1747G	μA747HM	
MC1747L	μA747DM	
MC1748CG	μA748HC	
MC1748CP1	μA748TC	
MC1748G	μA748HM	
MC1776CG	μA776HC	
MC1776G	μA776HM	
MC3301P	μA3301PC	
MC3302P	μA3302PC	
MC3401P	μA3401PC	
MC3403L	μA3403DC	
MC3403P	μA3403PC	
MC3503L	μA3503DM	
MC55107L	55107ADM	
MC55108L	55108ADM	
MC55109L	55109DM	
MC55110L	55110DM	
MC5528L	5528DM	
MC5529L	5529DM	
MC55325L	55325DM	
MC5534L	5534DM	
MC5535L	5535HM	
MC75107L	75107ADC	
MC75107P	75107APC	
MC75108L	75108ADC	
MC75108P	75108APC	
MC75109L	75109DC	
MC75109P	75109PC	
MC75110L	75110DC	
MC75110P	75110PC	
MC75207L	75207DC	
MC75207P	75207PC	
MC75208L	75208DC	
MC75208P	75208PC	
MC7524L	7524DC	
MC7524P	7524PC	
MC7525L	7525DC	
MC7525P	7525PC	
MC7528L	7528DC	
MC7528P	7528PC	
MC7529L	7529DC	
MC7529P	7529PC	
MC75325L	75325DC	
MC75325P	75325PC	
MC7534L	7534DC	
MC7534P	7534PC	
MC7535L	7535DC	
MC7535P	7535PC	
MC75450L	75450BDC	
MC75450P	75450BPC	
MC75451P	75451BTC	
MC75452P	75452BTC	
MC75453P	75453BTC	
MC75454P	75454BTC	
MC75491P	75491PC	
MC75492P	75492PC	
MC7705CP		μA78M05UC
MC7706CP		μA78M06UC
MC7708CP		μA78M08UC
MC7712CP		μA78M12UC
MC7715CP		μA78M15UC
MC7718CP		μA7818UC
MC7720CP		μA78M20UC
MC7724CP		μA78M24UC
MC7805CK	μA7805KC	
MC7805CP	μA7805UC	
MC7806CK	μA7806KC	
MC7806CP	μA7806UC	
MC7808CK	μA7808KC	
MC7808CP	μA7808UC	
MC7812CK	μA7812KC	
MC7812CP	μA7812UC	
MC7815CK	μA7815KC	
MC7815CP	μA7812UC	
MC7818CK	μA7812KC	
MC7818CP	μA7812UC	
MC7824CK	μA7824KC	
MC7824CP	μA7824UC	
MC7905CK	μA7905KC	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC7905CP	μA7905UC	
MC7906CK	μA7906KC	
MC7906CP	μA7906UC	
MC7908CK	μA7908KC	
MC7908CP	μA7908UC	
MC7912CK	μA7912KC	
MC7912CP	μA7912UC	
MC7915CK	μA7915KC	
MC7915CP	μA7915UC	
MC7918CK	μA7918KC	
MC7918CP	μA7918UC	
MC7924CK	μA7924KC	
MC7924CP	μA7924UC	
MC8T13L	μA8T13DM	
MC8T13P	μA8T13PC	
MC8T14L	μA8T14DM	
MC8T23P	μA8T23PC	
MC8T24P	μA8T24PC	
MFC4060A		μA78MGT2C
MFC4062A		μA78MGT2C
MFC4063A		μA78MGT2C
MFC4064A		μA78MGT2C
MFC6030A		μA78MGT2C
MFC6032A		μA78MGT2C
MFC6033A		μA78MGT2C
MFC6034A		μA78MGT2C
MFC8000		μA739PC
MFC8001		μA739PC
MFC8002		μA739PC
MFC8030		μA703HC
MFC8070		μA742DC
MLM101AG	μA101AHM	
MLM104G	μA104HM	
MLM105G	μA105HM	
MLM107G	μA107HM	
MLM109G		μA78M05HM
MLM109K		μA109KM
MLM110G	μA110HM	
MLM201AG	μA201AHM	
MLM204G	μA204HM***	
MLM205G	μA205HM***	
MLM207G	μA207HM	
MLM209G		μA78M05HM
MLM209K	μA209KM	μA7805KM
MLM210G	μA210HM***	
MLM301AG	μA301AHC	
MLM301AP1	μA301ATC	
MLM304G	μA304HC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MLM305G	μA305HC	
MLM307G	μA307HC	
MLM309G		μA78M05HC
MLM309K	μA309KC	
MLM310G	μA310HC	
MLM311G	μA311HC***	
MLM311P1	μA311TC***	
NE515A	μA733PC	
NE515K		μA733HC
NE521A		75107APC
NE521F		75107ADC
NE522A		75108APC
NE522F		75108ADC
NE526A		μA760DC
NE526K		μA760HC
NE527K		μA760HC
NE529K		μA760HC
NE536T	μA740HC	μA740HC
NE550A		μA723PC
NE550L		μA723HC
NE555V	μA555TC	
NE556A	μA556PC	
NE556F	μA556DC	
NE592A		μA733PC
N3207A-1F	9607DC	
N5071A	μA781PC	
N5072A	μA746PC	
N5558T	μA1458HC	
N5558V	μA1458TC	
N5570B	μA780PC	
N8T13B	μA8T13PC	
N8T13F	μA8T13DC	
N8T14B	μA8T14PC	
N8T14F	μA8T14DC	
N8T15F		9616DC
N8T16F		9627DC
N8T23B	μA8T23PC	
N8T23F	μA8T23DC	
N8T24B	μA8T24PC	
N8T24F	μA8T24DC	
OP-07	μA714HC	
PA239A		μA739PC
RC1488D		9616DC

5

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
RC1489AD		9617DC
RC1489D		9617DC
RC4136D	μA4136DC/DM	
RC4136DB	μA4136PC	
RC4136DP	μA4136PC	
RC4558DN	μA4558TC*	
RC4558T	μA4558HC*	
RC55109D	55109DM	
RC555DN	μA555TC	
RC556D	μA556DC	
RC556DP	μA556PC	
RC733TF	μA733HC	
RC75107AD	75107ADC	
RC75107AP	75107APC	
RC75108AD	75108ADC	
RC75108ADP	75108APC	
RC75109D	75109DC	
RC75109DP	75109PC	
RC75110D	75110DC	
RC75110DP	75110PC	
RC75150D		9616DC
RC75154M		9617DC
RC7524M	7524DC	
RC7524MP	7524PC	
RC7525M	7525DC	
RC7525MP	7525PC	
RC7528M	7528DC	
RC7528MP	7528PC	
RC7529M	7529DC	
RC7529MP	7529PC	
RC75325M	75325DC	
RC75325MP	75325PC	
RC8T13M	μA8T13DC	
RC8T13MP	μA8T13PC	
RC8T14M	μA8T14DC	
RC8T14MP	μA8T14PC	
RC8T23M	μA8T23DC	
RC8T23MP	μA8T23PC	
RC8T24M	μA8T24DC	
RC8T24MP	μA8T24PC	
RC9621D	9621DC	
RC9622D	9622DC	
RM4136D	μA4136DM	
RM55107AD	55107ADM	
RM55108AD	55108ADM	
RM55110D	55110DM	
RM5524M	5524DM	
RM5525M	5525DM	
RM55325M	55325DM	
RM555T	μA555HM	
RM556D	μA556DM	
RM733TF	μA733HM	
RM8T13M	μA8T13DM	
RM8T14M	μA8T14DM	
RM9621D	9621DM	
RM9621J	9621FM	
RM9622D	9622DM	
RM9622J	9622FM	
SE515K		μA733HM
SE526A		μA760DM
SE526K		μA760HM
SE527K		μA760HM
SE529K		μA760HM
SE536T		μA740HM
SE550L		μA723HM
SE592A		μA733DM
SE592K		μA733HM
SN52L022L		μA798HM
SN52L044JA		μA3503DM
SN52309LA		μA78M05HM
SN52506J		μA711DM
SN52510L		μA710HM
SN52514J		μA711DM
SN52520J		μA710DM
SN52558L	μA1558HM	
SN52660JA		μA776DM
SN52660L		μA776HM
SN52702J	μA702DM	
SN52702L	μA702HM	
	SN52709J	μA709DM
SN52709L	μA709HM	
SN52710J	μA710DM	
SN52710L	μA710HM	
SN52711J	μA711DM	
SN52711L	μA711HM	
SN52723J	μA723DM	
SN52723L	μA723HM	
SN52741J	μA741DM	
SN52741L	μA741HM	
SN52747J	μA747DM	
SN52747L	μA747HM	
SN52748J	μA748DM	
SN52748L	μA748HM	
SN52771J		μA776DM
SN52771L		μA776HM
SN52777J	μA777DM	
SN52777L	μA777HM	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN52810J		μA710DM
SN52810L		μA710HM
SN52811J		μA711DM
SN52811L		μA711HM
SN52820J		μA711DM
SN5510FA		μA733FM
SN5510L		μA733HM
SN55107AJ	55107ADM	
SN55107BJ	55107BDM	
SN55108AJ	55108ADM	
SN55108BJ	55108BDM	
SN55109J	55109DM	
SN5511FA		μA733FM
SN5511L		μA733HM
SN55110J	55110DM	
SN55112J	55112DM	
SN55114J	9614DM	
SN55114SB	9614FM	
SN55115J	9615DM	
SN55115SB	9615FM	
SN5512L		μA733HM
SN55121J	55121DM	
SN55122J	55122DM	
SN55123J	55123DM	
SN55124J	55124DM	
SN5514L		μA733HM
SN55207J	55207DM	
SN55208J	55208DM	
SN55224J	55224DM	
SN55225J	55225DM	
SN55232J	55232DM	
SN55233J	55233DM	
SN55234J	55234DM	
SN55235J	55235DM	
SN55238J	55238DM	
SN55239J	55239DM	
SN5524J	5524DM	
SN5525J	5525DM	
SN5528J	5528DM	
SN5529J	5529DM	
SN55325J	55325DM	
SN55325SB	55325FM	
SN55326SB	55326DM*	
SN55327SB	55327DM*	
SN5534J	5534DM	
SN5535J	5535DM	
SN5538J	5538DM	
SN5539J	5539DM	
SN55450BJ	55450BDM	
SN55450J	55450DM	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN55451BL	55451BHM	
SN55451L	55451HM	
SN55452BL	55452BHM	
SN55452L	55452HM	
SN55453BL	55453BHM	
SN55453L	55453HM	
SN55454BL	55454BHM	
SN55454L	55454HM	
SN55460J	55460DM	
SN55461L	55461HM	
SN55462L	55462HM	
SN55463L	55463HM	
SN55464L	55464HM	
SN55470J	55470DM	
SN55471L	55471HM	
SN55472L	55472HM	
SN55473L	55473HM	
SN55474L	55474HM	
SN592K		μA733HC
SN71710J	μA710DC	
SN72L022L		μA798HC*
SN72L022P		μA798TC*
SN72L044JA		μA3403DC
SN72L044N		μA3403PC
SN72301AN	μA301ADC	
SN72301L	μA301AHC	
SN72301P	μA301ATC	
SN72304L	μA104HM	
SN72305AL	μA305AHC	
SN72305L	μA305HC	
SN72307L	μA307HC	
SN72307P	μA307TC	
SN72308AL	μA308AHC	
SN72308AN	μA308ADC	
SN72308L	μA308HC	
SN72308N	μA308DC	
SN72309LA		μA78M05HC
SN72310L	μA310HC	
SN72311L	μA311HC	
SN72311P	μA311TC	
SN72376P	μA376TC	
SN72440J		μA742DC
SN72440N		μA742DC
SN72506J		μA711DC
SN72506N		μA711PC
SN72510J		μA710DC
SN72510L		μA710HC
SN72510N		μA710PC
SN72514J		μA711DC
SN72514N		μA711PC

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN72555P	μA555TC	
SN72556N	μA556PC	
SN72558L	μA1458HC	
SN72558P	μA1458TC	
SN72660JA		μA776DC
SN72660L		μA776HC
SN72660N		μA776DC
SN72660P		μA776TC
SN72702J	μA702DC	
SN72702L	μA702HC	
SN72709J	μA709DC	
SN72709L	μA709HC	
SN72709P	μA709TC	
SN72710L	μA710HC	
SN72710N	μA710PC	
SN72711J	μA711DC	
SN72711L	μA711HC	
SN72711N	μA711PC	
SN72720J		μA710DC
SN72720N		μA710PC
SN72723J	μA723DC	
SN72723L	μA723HC	
SN72723N	μA723PC	
SN72733J	μA733DC	
SN72733L	μA733HC	
SN72733N	μA733PC	
SN72741J	μA741DC	
SN72741L	μA741HC	
SN72741N	μA741PC	
SN72741P	μA741TC	
SN72747J	μA747DC	
SN72747L	μA747HC	
SN72747N	μA747PC	
SN72748J	μA748DC	
SN72748L	μA748HC	
SN72748N	μA748DC	
SN72748P	μA748TC	
SN72771J		μA776DC
SN72771L		μA776HC
SN72771N		μA776DC
SN72771P		μA776TC
SN72777J	μA777DC	
SN72777L	μA777HC	
SN72777N	μA777DC	
SN72777P	μA777TC	
SN72810J		μA710DC
SN72810L		μA710HC
SN72810N		μA710PC
SN72811J		μA711DC
SN72811L		μA711HC
SN72811N		μA711PC
SN72820J		μA711DC
SN72820N		μA711PC
SN7510L		μA733HC
SN75107AJ	75107ADC	
SN75107AN	75107APC	
SN75107BJ	75107BDC	
SN75107BN	75107BPC	
SN75107J	75107DC	
SN75108AJ	75108ADC	
SN75108AN	75108APC	
SN75108BJ	75108BDC	
SN75108BN	75108BPC	
SN75108J	75108DC	
SN75109J	75109DC	
SN75109N	75109PC	
SN7511L		μA733HC
SN7511N		μA733PC
SN75110J	75110DC	
SN75110N	75110PC	
SN75112J	75112DC	
SN75112N	75112PC	
SN75114J	9614DC	
SN75114N	9614PC	
SN75115J	9615DC	
SN75115N	9615PC	
SN7512L		μA733HC
SN7512N		μA733PC
SN75121J	75121DC	
SN75121N	75121PC	
SN75122J	75122DC	
SN75122N	75122PC	
SN75123J	75123DC	
SN75123N	75123PC	
SN75124J	75124DC	
SN75124N	75124PC	
SN7514L		μA733HC
SN7514P		μA733PC
SN75150J	75150DC	9616DC
SN75150P	75150PC	9616DC
SN75152J		9627DC
SN75154J	75154DC	9617DC
SN75182N		9615DC
SN75183N		9614DC
SN75188J		9616DC
SN75189AJ		9617DC
SN75189J		9617DC
SN75207J	75207DC	
SN75207N	75207PC	
SN75208J	75208DC	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN75208N	75208PC	
SN75224J	75224DC	
SN75224N	75224PC	
SN75225J	75225DC	
SN75225N	75225PC	
SN75232J	75232DC	
SN75232N	75232PC	
SN75233J	75233DC	
SN75233N	75233PC	
SN75234J	75234DC	
SN75234N	75234PC	
SN75235J	75235DC	
SN75235N	75235PC	
SN75238J	75238DC	
SN75238N	75238PC	
SN75239J	75239DC	
SN75239N	75239PC	
SN7524J	7524DC	
SN7524N	7524PC	
SN7525J	7525DC	
SN7525N	7525PC	
SN7528J	7528DC	
SN7528N	7528PC	
SN7529J	7529DC	
SN7529N	7529PC	
SN75325J	75325DC	
SN75325N	75325PC	
SN75326J	75326DC*	
SN75326N	75326PC*	
SN75327J	75327DC	
SN75327N	75327PC	
SN7534J	7534DC	
SN7534N	7534PC	
SN7535J	7535DC	
SN7535N	7535PC	
SN75365J		9607DC
SN75365N		9607PC
SN7538J	7538DC	
SN7538N	7538PC	
SN7539J	7539DC	
SN7539N	7539PC	
SN75450BJ	75450BDC	
SN75450BN	75450BPC	
SN75450N	75450BPC	
SN75451BL	75451BHC	
SN75451BP	75451BTC	
SN75451P	75451BTC	
SN75452BL	75452BHC	
SN75452BP	75452BTC	
SN75452P	75452BTC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN75453BL	75453BHC	
SN75453BP	75453BTC	
SN75453P	75453BTC	
SN75454BL	75454BHC	
SN74545BP	75454BTC	
SN75454P	75454BTC	
SN75460J	75460DC	
SN75460N	75460PC	
SN75461L	75461HM	
SN75461P	75461TC	
SN75462L	75462HM	
SN75462P	75462TC	
SN75463L	75463HM	
SN75463P	75463TC	
SN75464L	75464HM	
SN75464P	75464TC	
SN75470J	75470DC	
SN75470N	75470PC	
SN75471L	75471HC	
SN75471P	75471TC	
SN75472L	75472HC	
SN75472P	75472TC	
SN75473L	75473HC	
SN75473P	75473TC	
SN75474L	75474HC	
SN75474P	75474TC	
SN75491N	75491PC	
SN75492N	75492PC	
SN76001N		TBA641A12
SN76005ND		μA706BPC
SN76024ND		μA706BPC
SN76104N	μA732PC	
SN76105N		μA732PC
SN76111N	μA767PC	
SN76116N	μA758PC	
SN76131N	μA739PC	
SN76149N	μA749PC	
SN76242N	μA780PC	
SN76243N	μA781PC	
SN76246N	μA746PC	
SN76298N		μA787PC
SN76545		TBA920
SN76565N	μA3064PC	
SN76591P	μA1391TC	
SN76594P	μA1394TC	
SN76600P		μA757PC
SN76635N	μA720PC	
SN76642N		μA2136PC
SN76650N		μA757PC
SN76666N	μA3065PC	

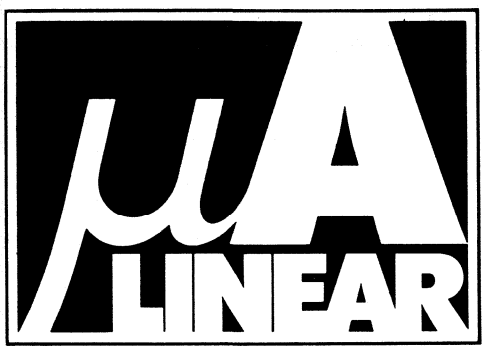
LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN76669N	μA2136PC	
SN76675N	μA3075PC	
SN76678P	μA753TC	
SN76689N	μA3089PC	
SSS725AJ		μA725AHM
SSS725BJ		μA725EHM
SSS725EJ		μA725EHC
SSS741CJ		μA741EHC
SSS741J		μA741AHM
SSS747CK		μA747EHC
SSS747CP		μA747EDC
SSS747K		μA747AHM
SSS747P		μA747ADM
S5558T	μA1558HM	
S5596K	μA796H	
S8T13F	μA8T13DM	
S8T14F	μA8T14DM	
S8T15F		9616DM
S8T16F		9627DM
TAA630S	TAA630S	
TBA510	TBA510	
TBA520	TBA520	
TBA530	TBA530	
TBA540	TBA540	
TBA560C	TBA560C	
TBA641A12	TBA641A12	
TBA641B11	TBA641B11	
TBA800	TBA800	
TBA810AS	TBA810AS	
TBA810S	TBA810S	
TBA920	TBA920	
TBA920S	TBA920S	
TBA970	TBA970	
TBA990	TBA990	
μA709CA	μA709PC	
μA709CT	μA709HC	
μA709Q	μA709FM	
μA709T	μA709HM	
μA710CA	μA710HC	
μA710CT	μA710HC	
μA710Q	μA710FM	
μA710T	μA710HM	
μA711CA	μA711PC	
μA711CK	μA711HC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA711K	μA711HM	
μA723CA	μA723PC	
μA723CL	μA723HC	
μA723L	μA723HM	
μA733A	μA733DM	
μA733CI	μA733DC	
μA733CK	μA733HC	
μA733I	μA733DM	
μA733K	μA733HM	
μA7330A	μA733PC	
μA740CT	μA740HC	
μA741CA	μA741PC	
μA741CT	μA741HC	
μA741CV	μA741TC	
μA741T	μA741HM	
μA747CA	μA747PC	
μA747CK	μA747HC	
μA747K	μA747HM	
μA748CA	μA748DC	
μA748CT	μA748HC	
μA748CV	μA748TC	
μA748T	μA748HC	
ULN2111A	μA2136PC	
ULN2113A		μA3065PC
ULN2114A	μA746PC	
ULN2114K	μA746HC	
ULN2120A	μA732PC	
ULN2121A		μA767PC
ULN2122A		μA732PC
ULN2124A	μA780PC	
ULN2126A	μA739PC	
ULN2127A	μA781PC	
ULN2128A	μA767PC	
ULN2129A		μA3075PC
ULN2136A	μA2136PC	
ULN2137A	μA720PC	
ULN2165A	μA3065PC	
ULN2209M	μA753TC	
ULN2210A		μA758PC
ULN2224A		μA788PC
ULN2228A		μA788PC
ULN2244A	μA758PC	
ULN2298A		μA787PC
ULX2262A	μA787PC	
ULX2264A	μA3064PC	
ULX2267A	μA3067PC	
ULX2289A	μA3089PC	
1458CE	μA1458CHC	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
1458CP	μA1458CTC	
1458E	μA1458HC	
1458P	μA1458TC	
1558E	μA1558HM	
2740BE	μA740HC	
2740CE	μA740HC	
556CJ	μA556PC	
709AE	μA709AHM	
709AH	μA709AFM	
709AL	μA709ADM	
709BE	μA709HM	
709BH	μA709FM	
709BL	μA709DM	
709CE	μA709HC	
709CJ	μA709PC	
709CL	μA709DC	
710BE	μA710HM	
710BH	μA710FM	
710BL	μA710DM	
710CE	μA710HC	
710CL	μA710DC	
711BE	μA711HM	
711BH	μA711FM	
711BL	μA711DM	
711CE	μA711HC	
711CJ	μA711PC	
711CL	μA711DC	
723BE	μA723HM	
723BL	μA723DM	
723CE	μA723HC	
723CJ	μA723PC	
723CL	μA723DC	
733DC	μA733DC	
733DM	μA733DM	
733FM	μA733FM	
733HC	μA733HC	
733HM	μA733HM	
741BE	μA741HM	
741BH	μA714FM	
741BL	μA741DM	
741CE	μA741HC	
741CJ	μA741PC	
741CP	μA741TC	
747BE	μA747HM	
747BL	μA747DM	
747CE	μA747HC	
747CJ	μA747PC	
747CL	μA747DC	
748BE	μA748HM	
748BH	μA748FM	
748BL	μA748DM	
748CE	μA748HC	
748CL	μA748DC	
748CP	μA748TC	
75450N	75450APC	
78M05BE	μA78M05HM	
78M05CE	μA78M05HC	
78M06BE	μA78M06HM	
78M06CE	μA78M06HC	
78M08BE	μA78M08HM	
78M08CE	μA78M08HC	
78M12BE	μA78M12HM	
78M12CE	μA78M12HC	
78M15BE	μA78M15HM	
78M15CE	μA78M15HC	
78M20BE	μA78M20HM	
78M20CE	μA78M20HC	
78M24BE	μA78M24HM	
78M24CE	μA78M24HC	



ORDER INFORMATION

Three basic units of information are contained in the code.

μA741	D	C
Device Type	Package Type	Temperature Range

DEVICE TYPE

This group of alpha numeric characters defines the data sheet which specifies the device functional and electrical characteristics.

PACKAGE TYPE

One letter represents the basic package style.

- D = Dual In-line Package (Hermetic, Ceramic)
- F = Flatpak (Hermetic)
- H = Metal Can Package
- J = Metal Power Package (TO-66 Outline)
- K = Metal Power Package (TO-3 Outline)
- P = Dual In-line Package (Molded)
- R = Mini DIP (Hermetic, Ceramic)*
- T = Mini DIP (Molded)
- U = Power Package (Molded, TO-220 Outline)

*Refer to individual data sheets for details. For special requirements, contact factory.

Different outlines exist within each package style to accommodate various die sizes and number of leads. Specific dimensions for each package can be found in the PACKAGE OUTLINES section of this catalog.

TEMPERATURE RANGE

Two basic temperature grades are in common use:

C = Commercial/Industrial/Consumer	M = Military
0°C to +70/75°C	−55°C to +125°C
−20°C to +85°C	−55°C to + 85°C
−40°C to +60°C	
−40°C to +85°C	

Exact values and conditions are indicated on the individual data sheets.

EXAMPLES

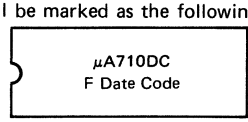
1. μA710FM
   This number code indicates a μA710 Voltage Comparator in a flatpak with military temperature rating capability.

2. μA725EHC
   This number code indicates a μA725 Instrumentation Operational Amplifier, electrical option E, in a metal can with a commercial temperature rating capability.

3. μA725EHCG
   This number code indicates the identical device as in example 2. Except it has a gold plated kovar header; the standard header is tin dipped.

DEVICE IDENTIFICATION/MARKING

All Fairchild standard catalog linear circuits will be marked as the following example:



UNIQUE 38510 PROCESSING

Additional processing to Fairchild Unique 38510 specifications is indicated by noting the appropriate requirements (QB, QC) after the standard order code.

Detailed ordering procedures are provided in the OEM price list.

MATRIX VI PROGRAM

Additional screening to the Fairchild Matrix VI program is indicated by the QM or QR suffix to the standard order code.

OLD ORDER CODES

Devices may continue to be purchased against old order codes (Example: U5R7723393; now 723HC). However, all products will be marked with new order codes unless otherwise specified.

PROCESS SCREENING REQUIREMENTS

MIL-STD-883A TEST METHODS	DESCRIPTION	JAN M38510 CLASS B	JAN M38510 CLASS C
Preseal Visual MTD. 2010	Cond. A Maximum Visual Criteria Cond. B. Optimum Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B
Bond Strength	Bond strength is monitored on a sample basis three times per shift per machine	BOND STRENGTH ACCEPTANCE	BOND STRENGTH ACCEPTANCE
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL
High Temp Storage	Cond. B Tstg = 125°C Specify Time Cond. C Tstg = 150°C Cond. D Tstg = 200°C	BAKE COND. C 24 HRS.	BAKE COND. C 24 HRS.
Thermal Shock MTD 1011	Cond. A 0°/100°C 15 cycles Cond. B −55°/125°C		
Temperature Cycle MTD 1010	Cond. B −55°/125°C Cond. C −65°/150°C 10 cycles Cond. D −65°/200°C	TEMP CYCLE COND. C	TEMP CYCLE COND. C
Mechanical Shock MTD 2002	Cond. A 500 G's 5 Shocks in X_1, X_2 Cond. B 1500 G's Y_1, Y_2, Z_1 and Z_2		
Constant Acceleration MTD 2001	Cond. D 20000 G's 1 minute in each Cond. E 30000 G's X_1, X_2, Y_1, Y_2 Cond. F 50000 G's Z_1, Z_2	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY
Hermetic Seal MTD 1014	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C1 Gross-FC43/Hot 10^{-3} cc/sec Cond. C2 Gross-FC78/Vacuum 10^{-5} cc/sec	HERMETICITY COND. A/B COND. C1-2	HERMETICITY COND. A/B COND. C1-2
Pre Burn-in Electrical 5004	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	OPTIONAL PRE B/I ELECT 25°C dc	
Burn-in Screen MTD 1015	Cond. A, Cond. B, Cond. C Cond. D, Cond. E, Cond. F	BURN-IN 160 HRS.	
Post Burn-in Electrical 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include: 25°C dc, 125°C dc, −55°C dc, 25°C dc, 25°C ac and 25°C Functional tests.	PST B/I ELECT 25°C dc +125°C dc −55°C dc 25°C ac	ELECTRICAL 25°C dc 25°C FUNCTIONAL
Radiography MTD 2012	6X, 8X magnification Specify number of views		
Quality Conformance Inspection MTD 5005	Group A: Electrical Characteristics Group B: Package oriented Tests Group C: Environmental and Life Tests	QUALITY CONFORMANCE Gp A, B and C	QUALITY CONFORMANCE Gp A, B and C
External Visual MTD 2009	3X, 10X magnification: Verify dimensions, configuration, lead structure, marking and workmanship	EXTERNAL VISUAL 100%	EXTERNAL VISUAL 100%
	RELIABILITY Figure of Merit	15	2
	ORDERING Part Number	JM38510/ 10101BCB	JM38510/ 10101CCB
	Part Marking	JM38510/ 10101BCB	JM38510/ 10101CCB

NOTE: RELIABILITY Figure of Merit is the Reliability Improvement Factor from RADC Reliability Notebook, Vol II, RADC-TR-67-108, Table XII-6, page 419.

MATRIX VI

COMMERCIAL AND INDUSTRIAL RELIABILITY PROGRAM FOR INTEGRATED CIRCUITS

Commercial and industrial users increasingly demand both optimized quality and reliability for the semiconductor integrated circuits purchased for their systems. Specific factors such as increased integrated circuit usage per board, high costs for receiving inspection, PC board and systems repair . . . and the frequently immeasureable cost associated with field failures, require the user to attain high quality and reliability coupled with total cost. MATRIX VI is designed to meet these user requirements.

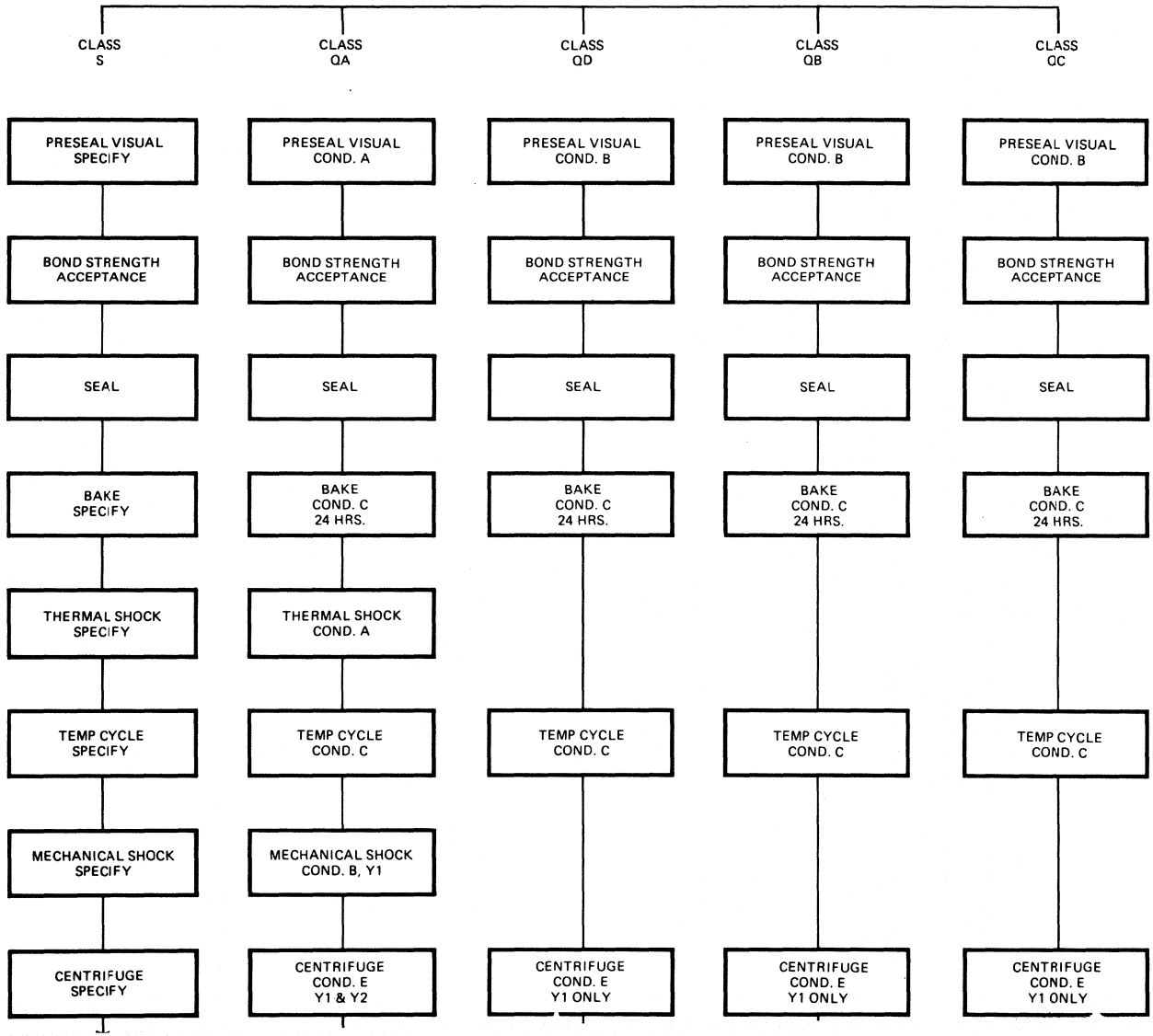
Fairchild's MATRIX VI PROGRAM offers a broad spectrum of screens and high technology/high volume integrated circuit products to meet the user's quality and reliability requirements typically associated with the commercial and industrial market place.

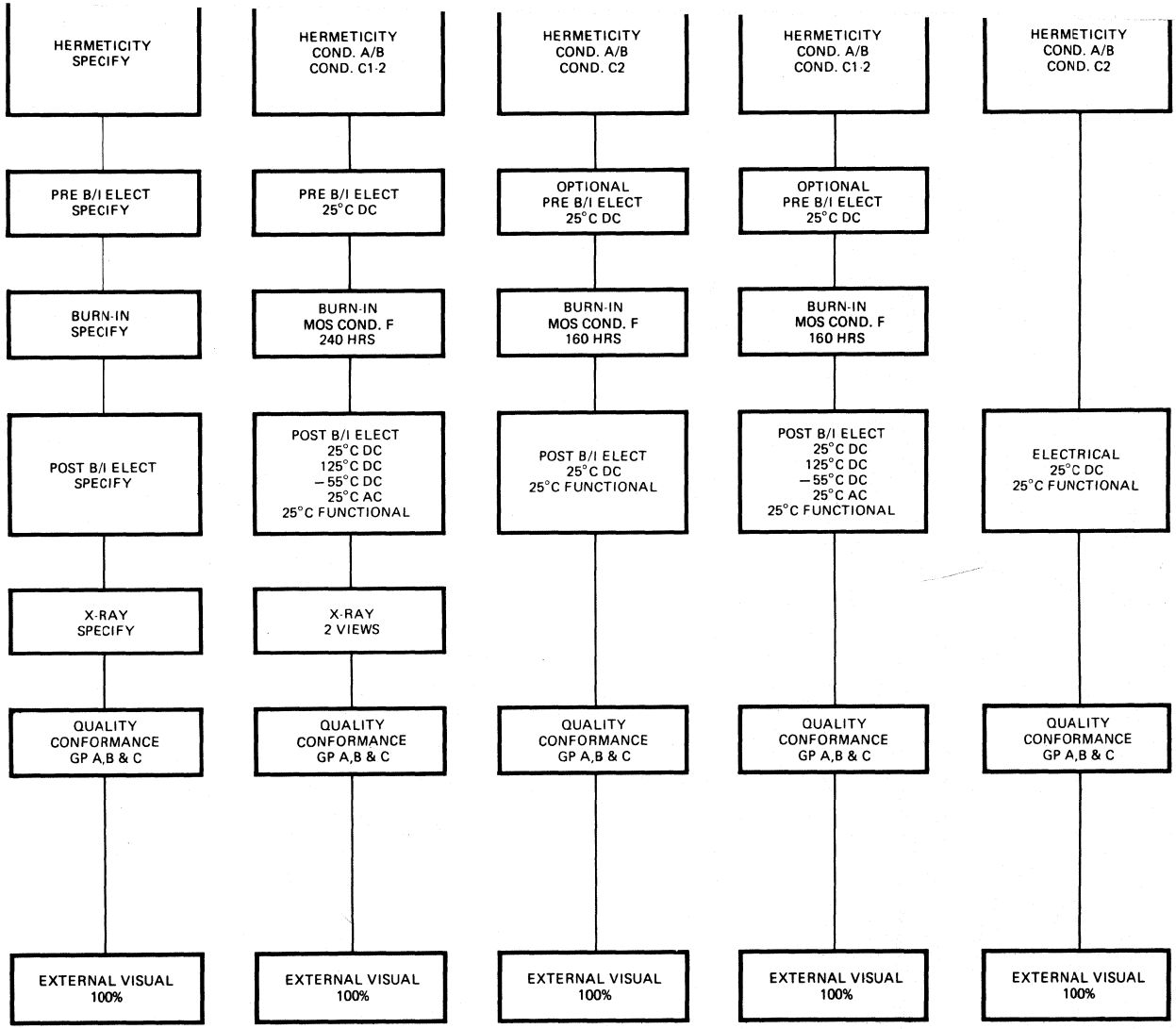
There are two screening options, each with a separate degree of reliability and cost level. To simplify a cost effective analysis, Reliability Factors have been assigned to each screening level. (See following pages.)

It is the goal of MATRIX VI to achieve the highest possible reliability consistent with the user's needs and to avoid "overbuying". Cost effective reliability is the essence of MATRIX VI.

We consider MATRIX VI to be the most comprehensive program of its kind to be offered to the industrial/commercial market place.

UNIQUE 38510




HERMETICITY SPECIFY
PRE B/I ELECT SPECIFY
BURN-IN SPECIFY
POST B/I ELECT SPECIFY
X-RAY SPECIFY
QUALITY CONFORMANCE GP A,B & C
EXTERNAL VISUAL 100%
( )
PER DRAWING
PER DRAWING
HERMETICITY COND. A/B COND. C1-2
PRE B/I ELECT 25°C DC
BURN-IN MOS COND. F 240 HRS
POST B/I ELECT 25°C DC 125°C DC −55°C DC 25°C AC 25°C FUNCTIONAL
X-RAY 2 VIEWS
QUALITY CONFORMANCE GP A,B & C
EXTERNAL VISUAL 100%
30
μA741 DMQA
μA741 DMQA
HERMETICITY COND. A/B COND. C2
OPTIONAL PRE B/I ELECT 25°C DC
BURN-IN MOS COND. F 160 HRS
POST B/I ELECT 25°C DC 25°C FUNCTIONAL
QUALITY CONFORMANCE GP A,B & C
EXTERNAL VISUAL 100%
15
μA741 DMQD
μA741 DMQD
HERMETICITY COND. A/B COND. C1-2
OPTIONAL PRE B/I ELECT 25°C DC
BURN-IN MOS COND. F 160 HRS
POST B/I ELECT 25°C DC 125°C DC −55°C DC 25°C AC 25°C FUNCTIONAL
QUALITY CONFORMANCE GP A,B & C
EXTERNAL VISUAL 100%
15
μA741 DMQB
μA741 DMQB
HERMETICITY COND. A/B COND. C2
ELECTRICAL 25°C DC 25°C FUNCTIONAL
QUALITY CONFORMANCE GP A,B & C
EXTERNAL VISUAL 100%
2
μA741 DMQC
μA741 DMQC

MIL-M-38510/MIL-STD-883

Fairchild Linear Products has within it a unique "company" totally dedicated to the processing of Hi-Rel parts. This company is complete with marketing, production, engineering, production control and quality assurance functions designed specifically to serve the special needs of the Hi-Rel customer.

Our standard Hi-Rel process flow is MIL-M-38510. Fairchild maintains an inventory of MIL-M-38510 Class B processed parts.

Where an approved JAN slash specification exists (*i.e.,* M38510/10101- - -) inventory is maintained for the JAN Class B part (*i.e.,* JM38510/10101 BGC).

Where an approved slash specification does not exist, product is processed per Fairchild's UNIQUE 38510 program Class B and inventoried. This UNIQUE 38510 inventory is available for processing to specific customer drawings or may be ordered directly from one of the standard processing options listed below.

UNIQUE 38510 IS A FULL SPECTRUM HI-REL PROGRAM

Fairchild's UNIQUE 38510 Program was established shortly after the release of MIL-M-38510 to provide JAN-equivalent processing for device types for which either a qualified source was not yet available or for which a MIL-M-38510 slash sheet was not yet established. Since the establishment of the program, many device types have become available as qualified JAN devices. The list of device types and vendors is expanding, offering the user a more complete list of qualified, multiple-sourced products available for design and production systems.

The list of device types utilizing new technologies or superior circuit design is also increasing. Many of these improvements solve specific or general circuit design needs and are desirable to use as quickly as possible.

As more and more programs require JAN qualified devices, but with increasingly sophisticated designs requiring newer technologies and devices not yet covered by JAN, there is a need for commonality in the reliability objectives and realizations in systems using both JAN and non-JAN devices. Fairchild's UNIQUE 38510 Full Spectrum Hi-Rel Program satisfies that need.

UNIQUE 38510 offers the following: (Processing Flows for each of the listed classes can be found on the following pages.)

- JAN CLASS B
- JAN CLASS C
- UNIQUE CLASS S
- UNIQUE CLASS QA
- UNIQUE CLASS QD
- UNIQUE CLASS QB (100% AC-25°C/DC HI-LO TEMP)
- UNIQUE CLASS QC

As a Full Spectrum supplier, Fairchild offers a complete product line processed to requirements ranging from the least demanding to the most complex with the technical expertise necessary for a thorough understanding of your requirements.

JAN PART NUMBERING SYSTEM

J M 38510/ 101 01 B G C

JAN DESIGNATOR

Cannot be marked with "J" unless qualified on Part I or Part II of the QPL

General Procurement Spec.

REFERS TO DETAIL SPEC

101 Op Amps
102 Voltage Regulators
103 Comparators
104 Interface
105 733
106 Voltage Followers
107 3-Terminal Voltage Regulators
108 Transistor Arrays
109 Timers

Defines Device Type

PROCESSING LEVEL

A
B
C

PACKAGE TYPE

A 14-lead 1/4 x 1/4 Flatpak
B 14-lead 1/4 x 1/8 Flatpak
C 14-lead 1/4 x 3/4 DIP
D 14-lead 1/4 x 3/8 Flatpak
E 16-lead 1/4 x 3/4 DIP
F 16-lead 1/4 x 3/8 Flatpak
G 8-lead Can
H 10-lead 1/4 x 1/4 Flatpak
I 10-lead Can
J 24-Lead 1/2 x 1 1/4 DIP
K 24-lead 3/8 x 1/2 Flatpak
L 24-lead 3/8 x 1/2 Flatpak
X 3-lead TO-5 Can
Y 2-lead TO-3 Can
Z 24-lead 1/4 x 3/8 Flatpak

LEAD FINISH

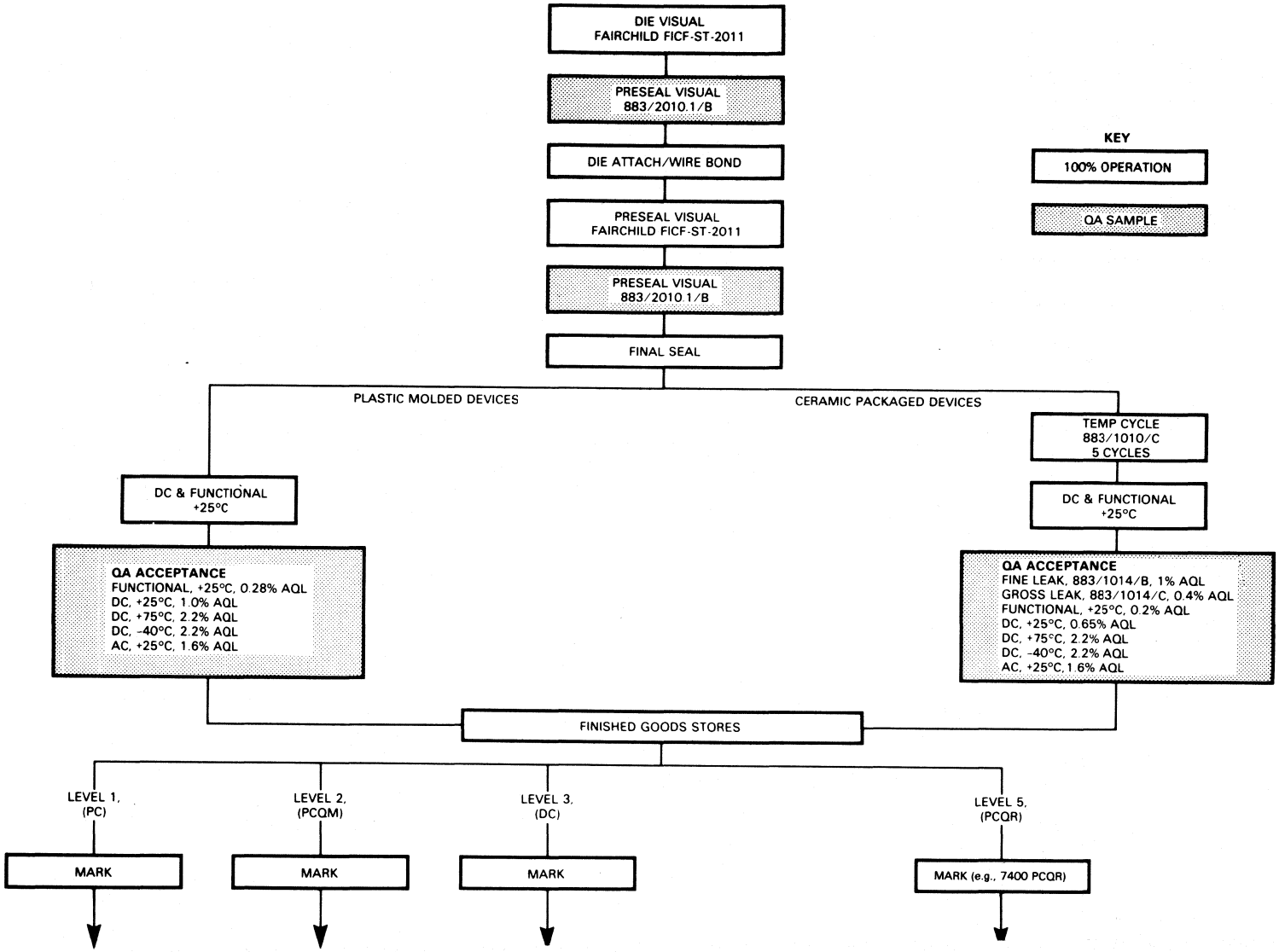
A Hot Solder DIP
B Tin Plate
C Gold Plate
D Nickel Plate

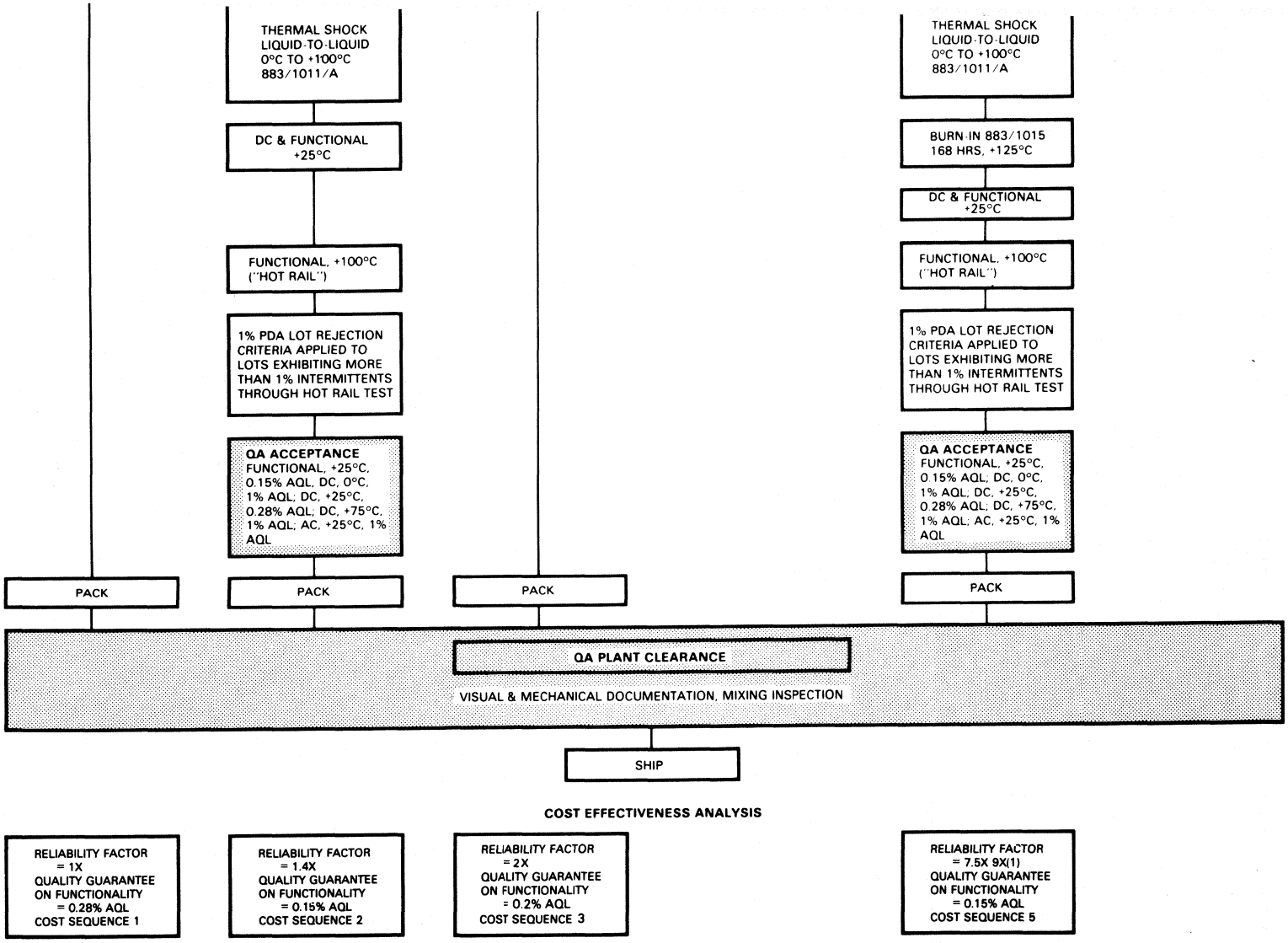
LINEAR JAN GENERIC PART NUMBERS – EXAMPLES

JM38510/	01	02	03	04	05	06	07	08	09	10
101	741	747	101A	108A	2101	2108	118			
102	723									
103	710	711	106	111						
104	55107	55108	9614	9615	55113	7831	7832			
105	733									
106	102	110								
107	7805	7812	7815	7824						
108	3018	3045								
109	555	556								
110										

Note: Dated material. Please contact Fairchild for latest revisions.

MATRIX VI PROCESS FLOW OPTIONS AND COST EFFECTIVENESS





NOTE (1): Burn-in has the same relative effectiveness for plastic molded devices as for ceramic/hermetic packaged devices. Assuming a controlled (air conditioned and constant power) field application/environment, the reliability factor would be approximately 9X. But should the field application be in a less controlled and power on/off application, the reliability factor would be approximately 7.5X.

DICE POLICY

GENERAL INFORMATION

Fairchild linear integrated circuits, constructed using the Fairchild Planar* epitaxial process, are available in dice form incorporating these features:

- Commercial or Military Selection (Military Limits Probed at 25°C)
- MIL-STD-883, Method 2010.2, Condition B Visual
- Gold Backing
- Glass Passivation
- Protective Packaging

ELECTRICAL CHARACTERISTICS

Each die is electrically tested at 25°C to guaranteed commercial dc parameters.

Military grade dice are guardband tested at 25°C dc to guarantee military temperature range operation.

QUALITY ASSURANCE

All Fairchild linear dice are 100% visually inspected and conform to MIL-STD-883, Method 2010.2, Condition B. In addition, quality control visually inspects the dice to a given sampling plan.

Each die is gold backed to aid die attach. Most dice are available with glass passivation coating with only the bonding pads exposed.

SHIPPING PACKAGES

Linear dice are packaged in containers with an anti-static sheet inserted between the lid and the dice. This sheet guards against electrostatic damage during shipment and storage.

The clear plastic carrier allows visual inspection of all the packaged dice. Each carrier is heat sealed within a transparent bag. A small piece of dehydrator paper with humidity indicating color is inserted in each bag prior to sealing.

ORDER INFORMATION

The minimum order quantity is 100 pieces and 100 piece increments of value greater than $1000.00 per line item.

Each linear integrated circuit die has a unique order code which describes the device type, the dice designation and type of electrical tests performed. The dice designation is denoted by an "X" and is substituted for the package code. Examples follow:

Generic Type	Order Code
μA741C**	μA741XC
μA3045	μA3045XC
μA75450	μA75450XC
μA101A	μA101AXC

**Some device types imply a military or commercial range by the generic type. Where this does not occur the suffix should be:

XM Military Grade Die

or XC Commercial Grade Die

SPECIAL CHIP PROCESSING

If there is a need for additional testing or processing, Fairchild will negotiate with the customer to meet his requirements.

PRODUCT AVAILABLE IN DICE FORM

Please refer to FSC OEM Price List for product available in die form.

*Planar is a patented Fairchild process.

INDEX

Comparator Data Sheets are presented in alphanumeric sequence.

μAF111 • μAF311

VOLTAGE COMPARATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

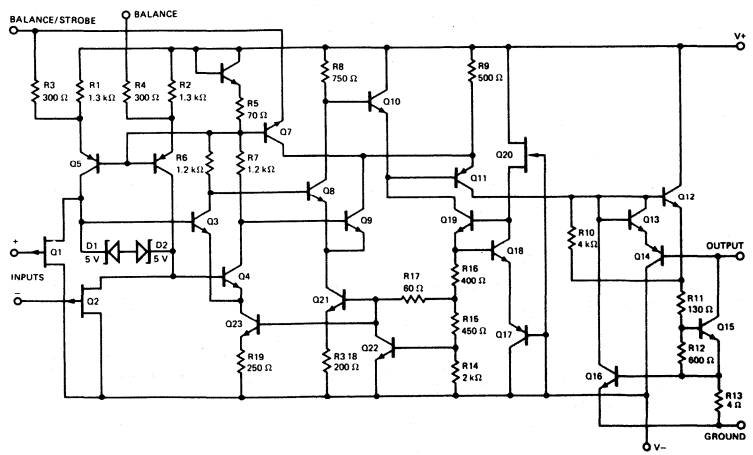
GENERAL DESCRIPTION – The μAF111 and μAF311 are monolithic, FET input Voltage Comparators, constructed using the Fairchild Planar* epitaxial process. The μAF111 series operates from the single 5 V integraetd circuit logic supply to the standard ±15 V operational amplifier supplies. The μAF111 series is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- **EXTREMELY LOW INPUT BIAS CURRENT** . . . 50 pA MAX (μAF111), 150 pA MAX (μAF311)
- **EXTREMELY LOW INPUT OFFSET CURRENT** . . . 25 pA MAX (μAF111), 75 pA MAX (μAF311)
- **DIFFERENTIAL INPUT VOLTAGE** . . . ±30 V
- **POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ±15 V**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **STROBE CAPABILITY**

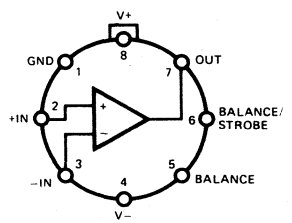
ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	36 V
Output to V– (μAF111)	50 V
(μAF311)	40 V
Ground to V–	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 s
Storage Temperature Range (Metal Can)	
Metal Can	–65°C to +150°C
Hermetic DIP	–55°C to +125°C
Operating Temperature Range	
Military (μAF111)	–55°C to +125°C
Commercial (μAF311)	0°C to +70°C
Lead Temperature	
Metal Can, Hermetic DIP (Soldering, 60 s)	300°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

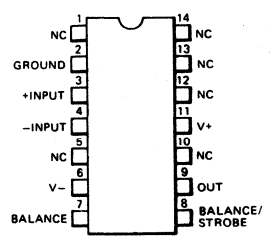


ORDER INFORMATION

TYPE	PART NO.
μAF111	μAF111H
μAF311	μAF311H

NOTE: Pin 4 connected to case.

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μAF111	μAF111D
μAF311	μAF311D

μAF111

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = −55°C to +125°C unless otherwise specified) Note 3

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, $R_S \leq$ 50 kΩ		0.7	4.0	mV
Input Offset Current (Note 4)	T_A = 25°C, V_{CM} = 0 (Note 6)		5.0	25	pA
Input Bias Current	T_A = 25°C, V_{CM} = 0 (Note 6)		20	50	pA
Voltage Gain	T_A = 25°C		200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	$V_{IN} \leq$ −5 mV, I_{OUT} = 50 mA T_A = 25°C		0.75	1.5	V
Strobe On Current	T_A = 25°C		3.0		mA
Output Leakage Current	$V_{IN} \geq$ 5 mV, V_{OUT} = 35 V T_A = 25°C		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq$ 50 kΩ			6.0	mV
Input Offset Current (Note 4)	V_S = ±15 V, V_{CM} = 0 (Note 6)		2.0	3.0	nA
Input Bias Current	V_S = ±15 V, V_{CM} = 0 (Note 6)		5.0	7.0	nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq$ 4.5 V, V^- = 0 $V_{IN} \leq$ −6 mV, $I_{SINK} \leq$ 8 mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq$ 5 mV, V_{OUT} = 35 V		0.1	0.5	μA
Positive Supply Current	T_A = 25°C		5.1	6.0	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

μAF311

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 0°C to 70°C unless otherwise specified) Note 3

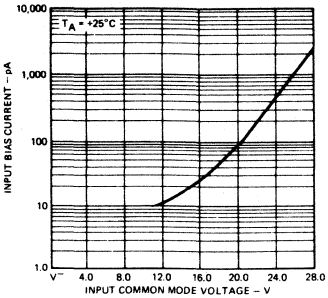
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, $R_S \leq$ 50 kΩ		2.0	10	mV
Input Offset Current (Note 4)	T_A = 25°C, V_{CM} = 0 (Note 6)		5.0	75	pA
Input Bias Current	T_A = 25°C, V_{CM} = 0 (Note 6)		25	150	pA
Voltage Gain	T_A = 25°C		200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	$V_{IN} \leq$ −10 mV, I_{OUT} = 50 mA T_A = 25°C		0.75	1.5	V
Strobe On Current	T_A = 25°C		3.0		mA
Output Leakage Current	$V_{IN} \geq$ 10 mV, V_{OUT} = 35 V T_A = 25°C		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq$ 50 kΩ			15	mV
Input Offset Current (Note 4)	V_S = ±15V, V_{CM} = 0 (Note 6)		1.0		nA
Input Bias Current	V_S = ±15 V, V_{CM} = 0 (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq$ 4.5 V, V^- = 0 $V_{IN} \leq$ −10 mV, $I_{SINK} \leq$ 8 mA		0.23	0.4	V
Positive Supply Current	T_A = 25°C		5.1	7.5	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

NOTES:

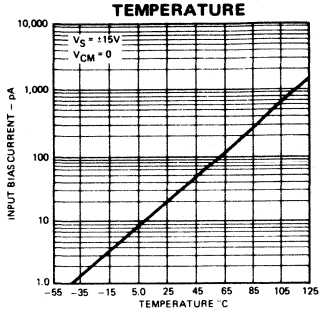
1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can; 8.3 mW/°C for mini DIP.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to ±15 V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.
6. For input voltages greater than 15 V above the negative supply the bias and offset currents will increase — see typical performance curves.

TYPICAL PERFORMANCE CURVES

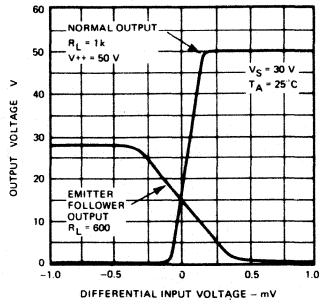
INPUT BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



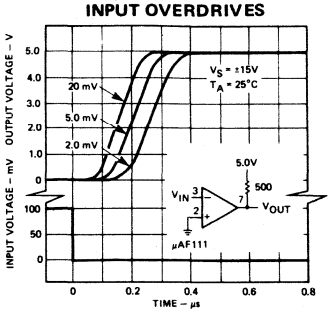
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



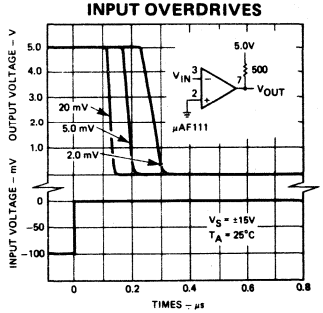
TRANSFER FUNCTION



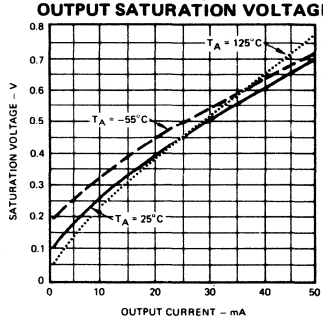
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



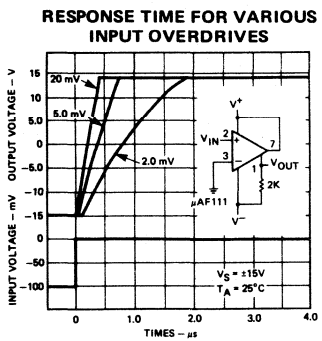
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



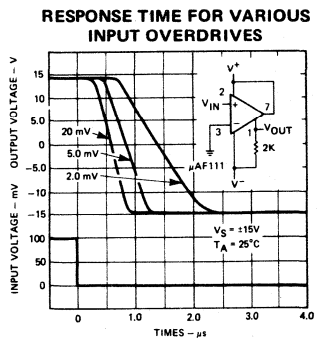
OUTPUT SATURATION VOLTAGE



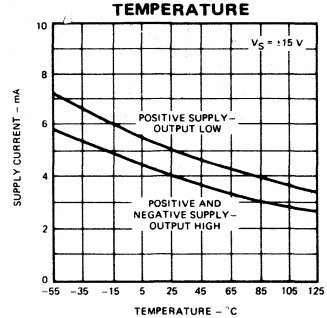
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



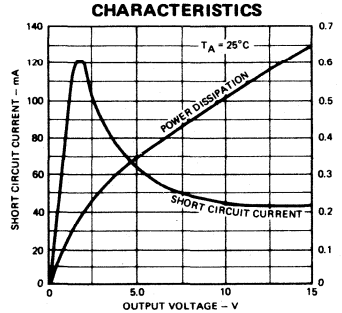
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



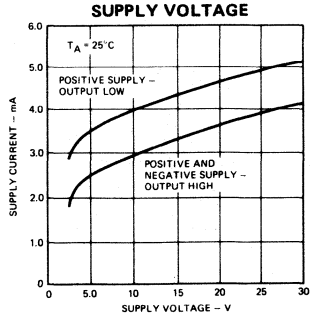
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



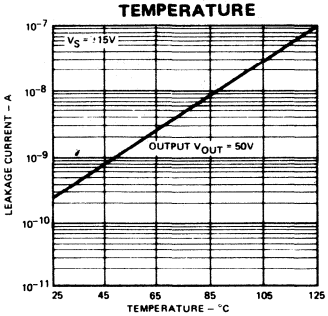
OUTPUT LIMITING CHARACTERISTICS



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



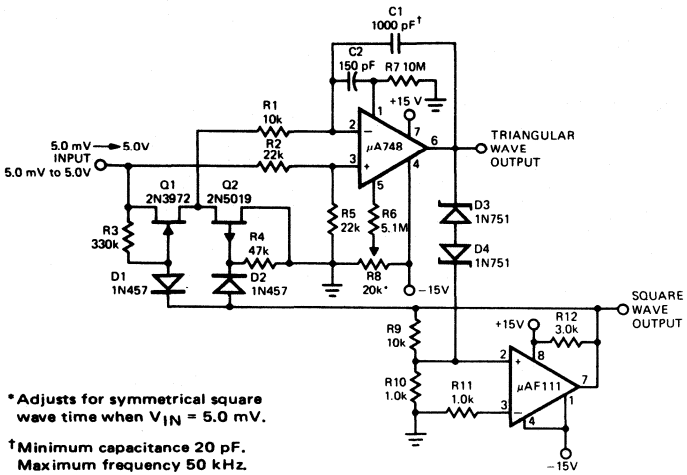
OUTPUT LEAKAGE CURRENT AS A FUNCTION OF TEMPERATURE



9

TYPICAL APPLICATIONS

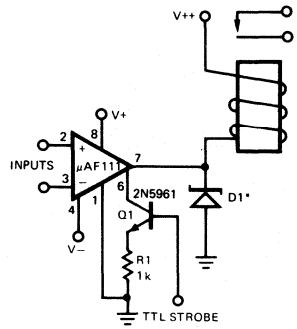
10 Hz TO 10 kHz VOLTAGE CONTROLLED OSCILLATOR



*Adjusts for symmetrical square wave time when V_{IN} = 5.0 mV.

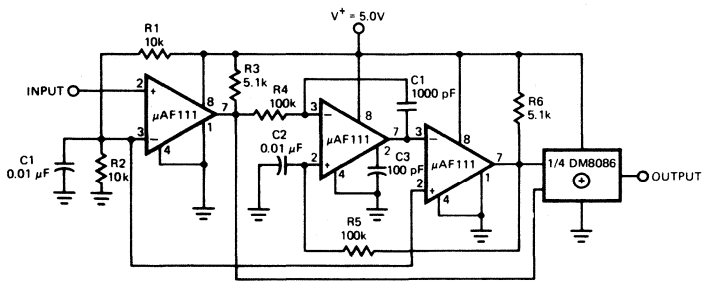
†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

RELAY DRIVER WITH STROBE



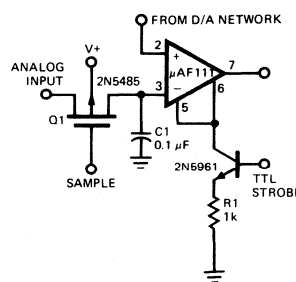
*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

FREQUENCY DOUBLER



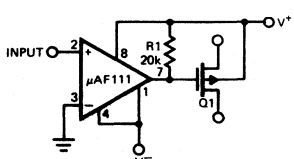
Frequency range:
Input — 5.0 kHz to 50 kHz
Output — 10 kHz to 100 kHz

STROBING OFF BOTH INPUT* AND OUTPUT STAGES

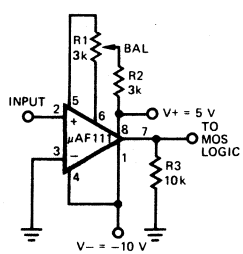


*Typical input current is 50 pA with inputs strobed off.

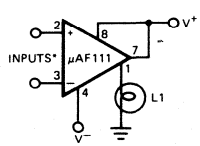
ZERO CROSSING DETECTOR DRIVING MOS SWITCH



ZERO CROSSING DETECTOR DRIVING MOS LOGIC



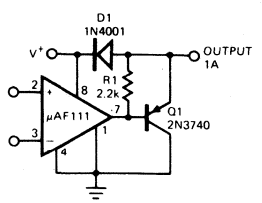
DRIVING GROUND-REFERRED LOAD



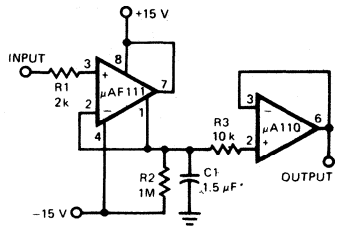
*Input polarity is reversed when using pin 1 as output.

TYPICAL APPLICATIONS (Cont'd)

COMPARATOR AND SOLENOID DRIVER

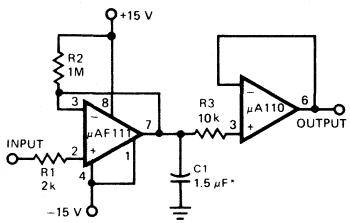


POSITIVE PEAK DETECTOR



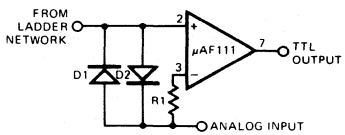
*Solid tantalum

NEGATIVE PEAK DETECTOR

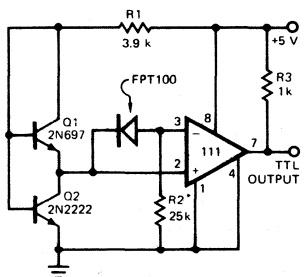


*Solid tantalum

USING CLAMP DIODES TO IMPROVE RESPONSE

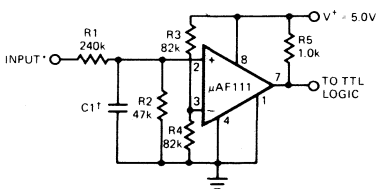


PRECISION PHOTODIODE COMPARATOR



*R2 sets the comparison level. At comparison, the photodiode has less than 5.0 mV across it, decreasing leakages by an order of magnitude.

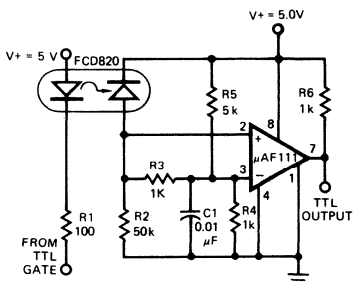
TTL INTERFACE WITH HIGH LEVEL LOGIC



*Values shown are for a 0 to 30 V logic swing and a 15 V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

DIGITAL TRANSMISSION ISOLATOR



DEFINITIONS:

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT – The change in input offset current over the operating temperature range divided by the operating temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE – The change in input offset voltage over the operating temperature range divided by the operating temperature range.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage applied between the input terminals for which operation within specifications is assured.

INPUT BIAS CURRENT – The average of the two input currents with no signal applied.

INPUT COMMON MODE VOLTAGE RANGE – The range of common mode input voltage over the device will operate within specifications.

INPUT OFFSET CURRENT – The difference between the two input currents with the output at the logic threshold voltage.

INPUT OFFSET VOLTAGE – The voltage which must be applied to the input terminals to give the logic threshold voltage at the output.

INPUT VOLTAGE RANGE – The range of voltage on either input terminal over which the device will operate as specified.

NEGATIVE OUTPUT VOLTAGE LEVEL – The dc output voltage in the negative direction with the input voltage equal to, or greater than, a minimum specified value.

RESPONSE TIME – The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level.

STROBE CURRENT – The maximum current taken by the strobe terminal during activation.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the dc output in the vicinity of the logic threshold.

μA111 • μA311

VOLTAGE COMPARATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

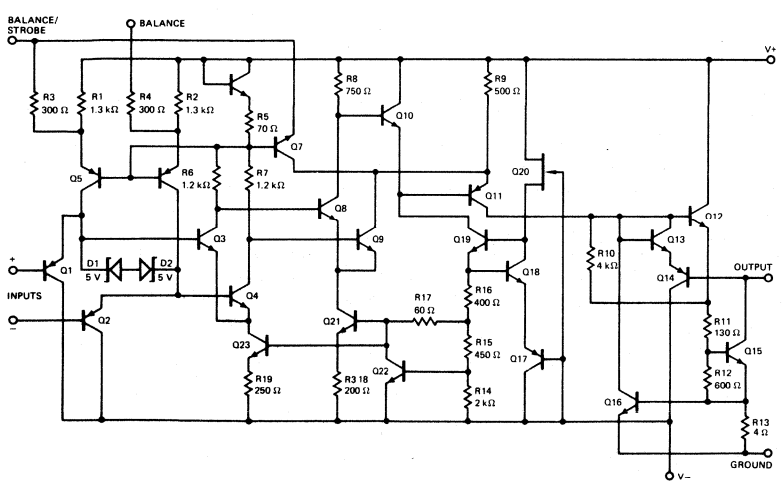
GENERAL DESCRIPTION — The 111 and 311 are monolithic, low input current Voltage Comparators, each constructed using the Fairchild Planar* epitaxial process. The 111 series operates from the single 5 V integrated circuit logic supply to the standard ±15 V operational amplifier supplies. The 111 series is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- **LOW INPUT BIAS CURRENT — 150 nA MAX (111), 250 nA MAX (311)**
- **LOW INPUT OFFSET CURRENT — 20 nA MAX (111), 50 nA MAX (311)**
- **DIFFERENTIAL INPUT VOLTAGE — ±30 V**
- **POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ±15 V**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **STROBE CAPABILITY**

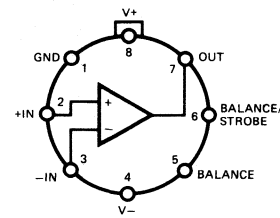
ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	36 V
Output to V− (μA111)	50 V
(μA311)	40 V
Ground to V−	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 s
Storage Temperature Range (Metal Can and Hermetic Mini DIP)	−65°C to +150°C
(Molded Mini DIP)	−55°C to +125°C
Operating Temperature Range	
Military (μA111)	−55°C to +125°C
Commercial (μA311)	0°C to +70°C

EQUIVALENT CIRCUIT



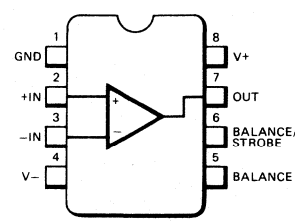
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA111	μA111H
μA311	μA311H

8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA111	μA111R
μA311	μA311R
μA311	μA311T

μA111

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = −55°C to +125°C unless otherwise specified) Note 3

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, $R_S \leq$ 50 kΩ		0.7	3.0	mV
Input Offset Current (Note 4)	T_A = 25°C		4.0	10	nA
Input Bias Current	T_A = 25°C		60	100	nA
Voltage Gain	T_A = 25°C		200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	$V_{IN} \leq$ −5 mV, I_{OUT} = 50 mA				
	T_A = 25°C		0.75	1.5	V
Strobe On Current	T_A = 25°C		3.0		mA
Output Leakage Current	$V_{IN} \geq$ 5 mV, V_{OUT} = 35 V				
	T_A = 25°C		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq$ 50 kΩ			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq$ 4.5 V, V^- = 0				
	$V_{IN} \leq$ −6 mV, $I_{SINK} \leq$ 8 mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq$ 5 mV, V_{OUT} = 35 V		0.1	0.5	μA
Positive Supply Current	T_A = 25°C		5.1	6.0	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

9

μA311

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 0°C to 70°C unless otherwise specified) Note 3

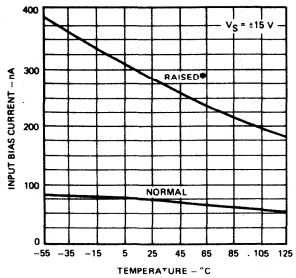
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	T_A = 25°C, $R_S \leq$ 50 kΩ		2.0	7.5	mV
Input Offset Current (Note 4)	T_A = 25°C		6.0	50	nA
Input Bias Current	T_A = 25°C		100	250	nA
Voltage Gain	T_A = 25°C		200		V/mV
Response Time (Note 5)	T_A = 25°C		200		ns
Saturation Voltage	$V_{IN} \leq$ −10 mV, I_{OUT} = 50 mA				
	T_A = 25°C		0.75	1.5	V
Strobe On Current	T_A = 25°C		3.0		mA
Output Leakage Current	$V_{IN} \geq$ 10 mV, V_{OUT} = 35 V				
	T_A = 25°C		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq$ 50 kΩ			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq$ 4.5 V, V^- = 0				
	$V_{IN} \leq$ −10 mV, $I_{SINK} \leq$ 8 mA		0.23	0.4	V
Positive Supply Current	T_A = 25°C		5.1	7.5	mA
Negative Supply Current	T_A = 25°C		4.1	5.0	mA

NOTES:

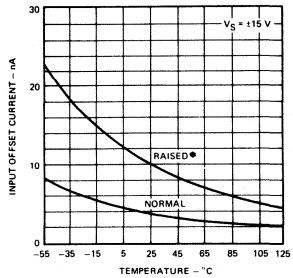
1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can; 8.3 mW/°C for mini DIP.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to ±15 V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR μA111

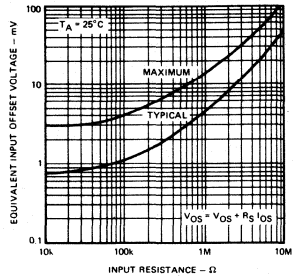
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

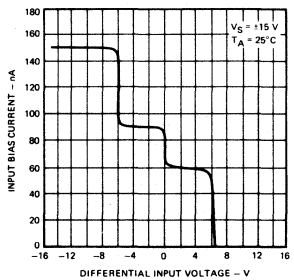


OFFSET VOLTAGE AS A FUNCTION OF INPUT RESISTANCE

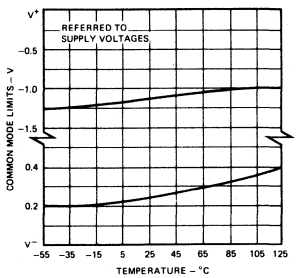


*Pins 5,6 and 8 are shorted.

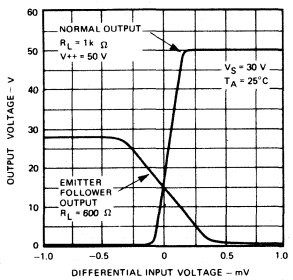
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



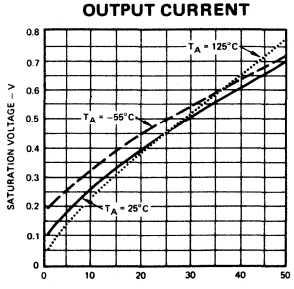
COMMON MODE LIMITS AS A FUNCTION OF TEMPERATURE



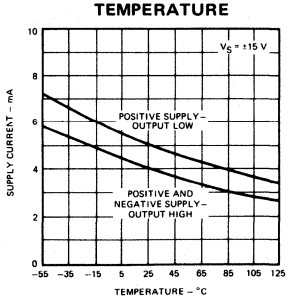
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



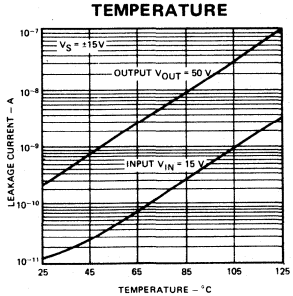
OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

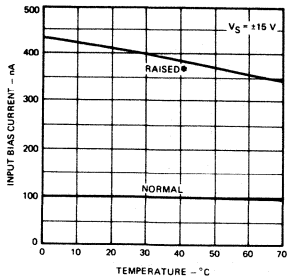


LEAKAGE CURRENTS AS A FUNCTION OF TEMPERATURE

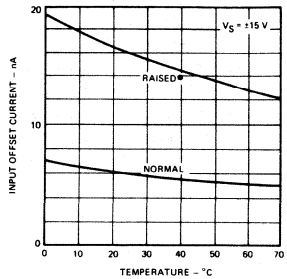


TYPICAL PERFORMANCE CURVES FOR μA311

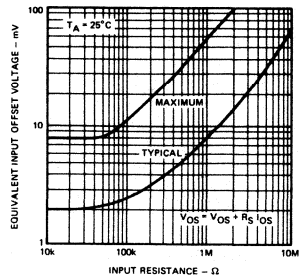
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

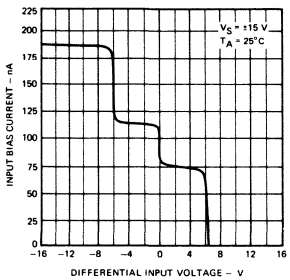


OFFSET VOLTAGE AS A FUNCTION OF INPUT RESISTANCE

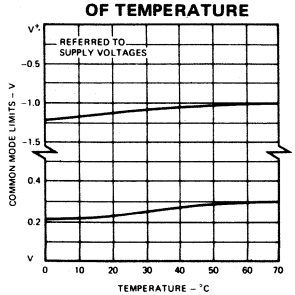


*Pins 5, 6 and 8 are shorted.

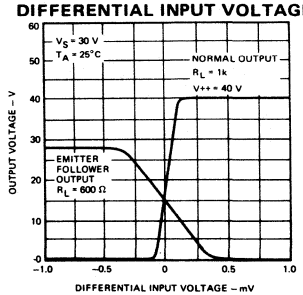
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



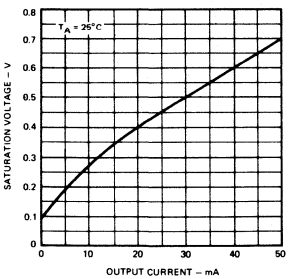
COMMON MODE LIMITS AS A FUNCTION OF TEMPERATURE



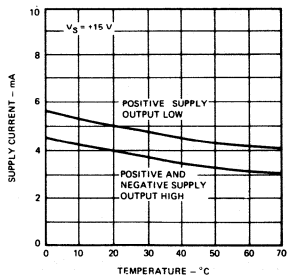
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



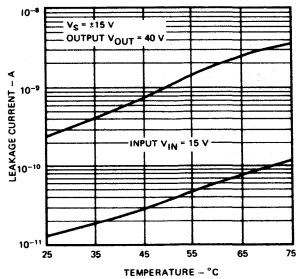
SATURATION VOLTAGE AS A FUNCTION OF CURRENT



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

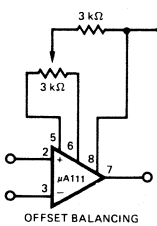


LEAKAGE CURRENT AS A FUNCTION OF TEMPERATURE

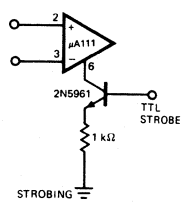


TYPICAL APPLICATIONS

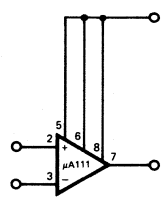
OFFSET NULL CIRCUIT



STROBE CIRCUIT



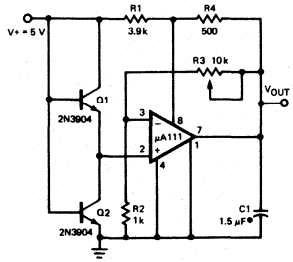
INCREASING INPUT STAGE CURRENT*



*Increases typical common mode slew rate from 7.0 V/μs to 18 V/μs.

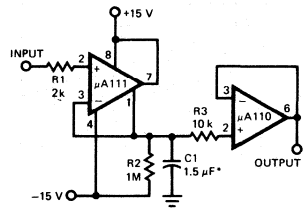
TYPICAL APPLICATIONS (Cont'd)

ADJUSTABLE LOW VOLTAGE REFERENCE SUPPLY



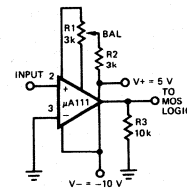
•Solid tantalum

POSITIVE PEAK DETECTOR

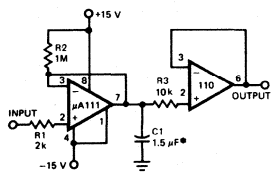


•Solid tantalum

ZERO CROSSING DETECTOR DRIVING MOS LOGIC

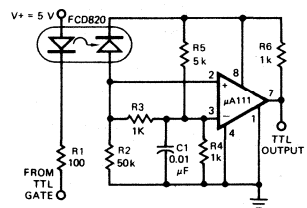


NEGATIVE PEAK DETECTOR

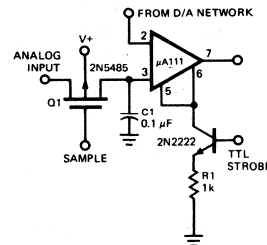


•Solid tantalum

DIGITAL TRANSMISSION ISOLATOR

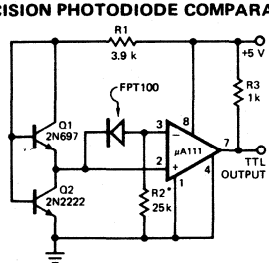


STROBING OF BOTH INPUT AND OUTPUT STAGES



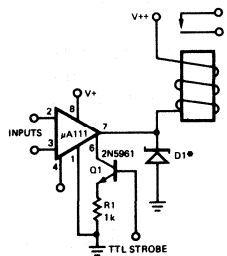
•Typical input current is 50 pA with inputs strobed off.

PRECISION PHOTODIODE COMPARATOR



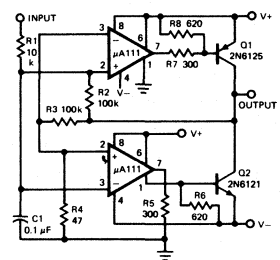
•R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

RELAY DRIVER WITH STROBE

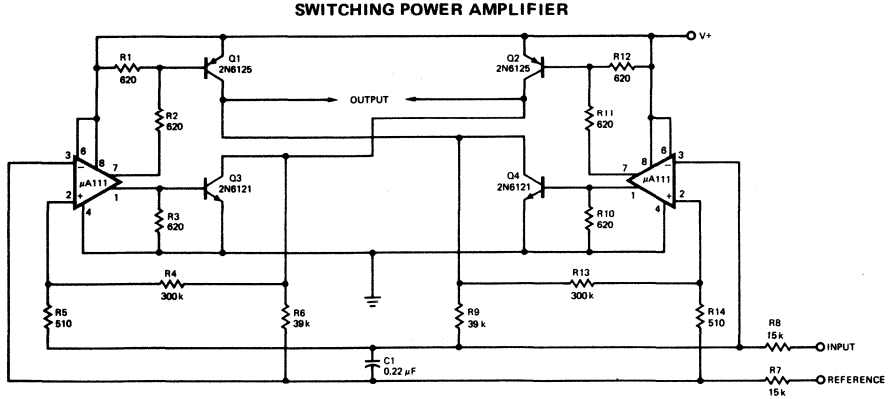


•Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

SWITCHING POWER AMPLIFIER



SWITCHING POWER AMPLIFIER



μA710
HIGH SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

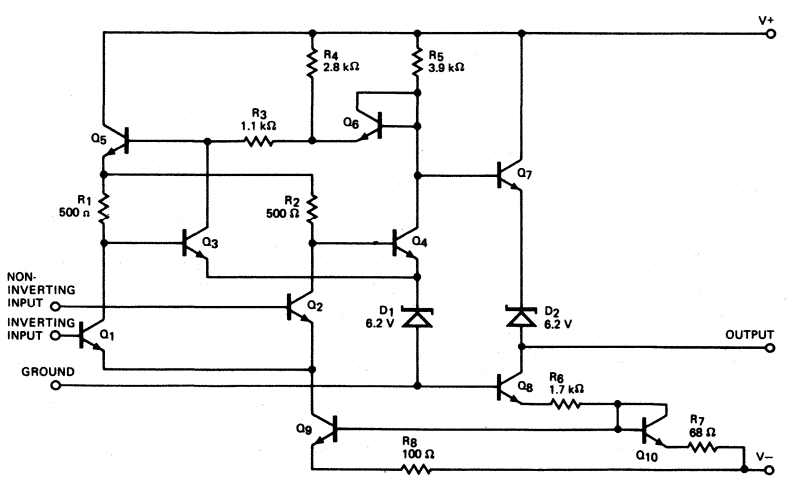
GENERAL DESCRIPTION – The μA710 is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

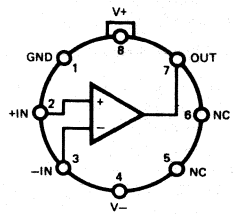
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Ouput Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Storage Temperature Range	
Metal Can, Hermetic DIP and Flatpak	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA710)	−55°C to +125°C
Commercial (μA710C)	0°C to +70°C
Lead Temperature	
Metal Can, Hermetic DIP and Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

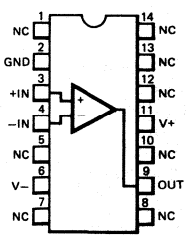


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA710	μA710HM
μA710C	μA710HC

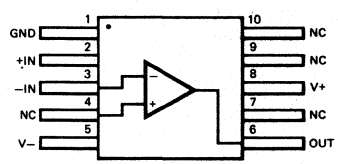
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA710	μA710DM
μA710C	μA710DC
μA710C	μA710PC

10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA710	μA710FM

9

Notes on following pages.

*Planar is a patented Fairchild process.

μA710

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified)

PARAMETER	CONDITIONS (Note 2)	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 3)			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = +125°C$		3.5	10	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = -55°C$		2.7	10	μV/°C
Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		5.0	25	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		15	75	nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	V− = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5 mV		4.6	7.0	mA
Power Consumption	V_{OUT} = Gnd, Inverting Input = +10 mV		90	150	mW

μA710C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified)

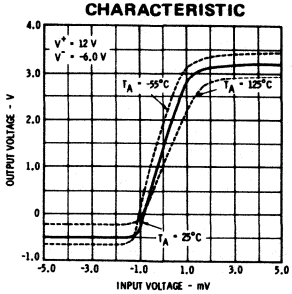
PARAMETER	CONDITIONS (Note 2)	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		15	50	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		24	100	nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	V− = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5 mV		4.6	7.0	mA
Power Consumption	V_{OUT} = Gnd, Inverting Input = +10 mV		90	150	mW

NOTES:

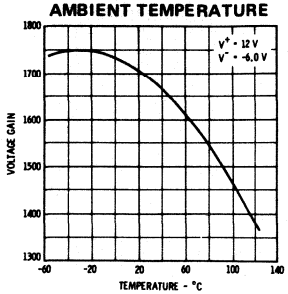
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for DIP, and 7.1 mW/°C for the Flatpak.
2. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage as follows: For 710, 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C. For 710C, 1.5 V at 0°C, 1.4 V at +25°C, and 1.2 V at +70°C.
3. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR μA710

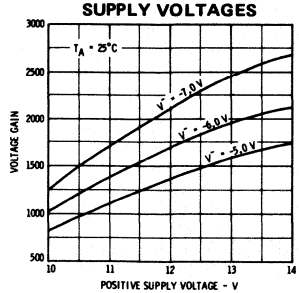
VOLTAGE TRANSFER CHARACTERISTIC



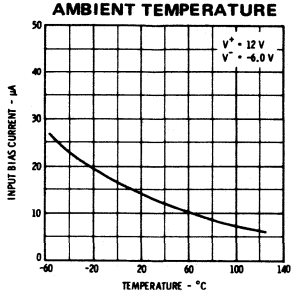
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



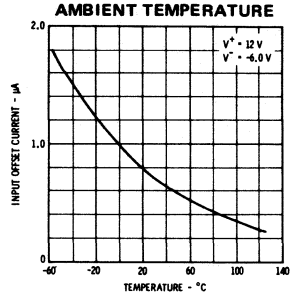
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



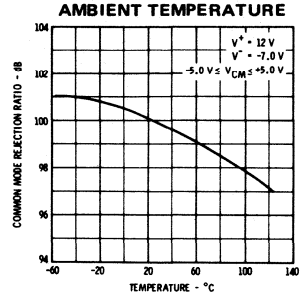
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



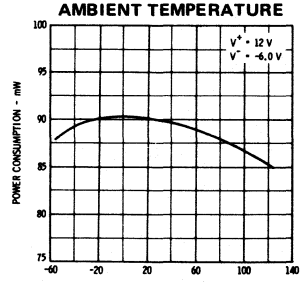
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



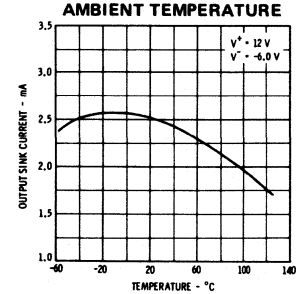
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



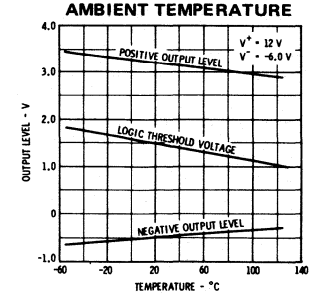
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



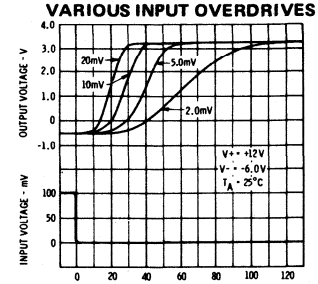
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



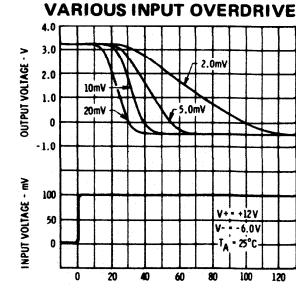
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



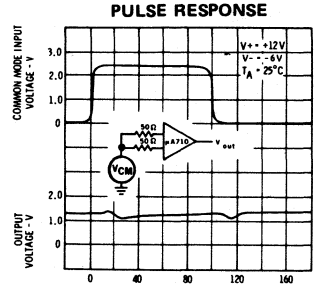
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



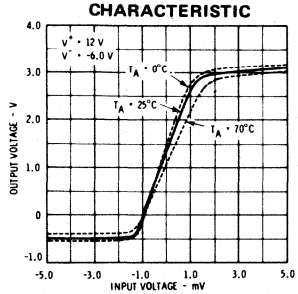
COMMON MODE PULSE RESPONSE



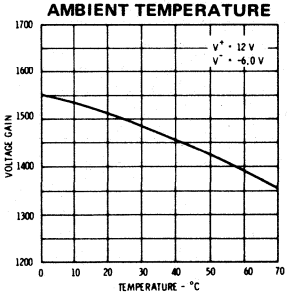
9

TYPICAL PERFORMANCE CURVES FOR μA710C

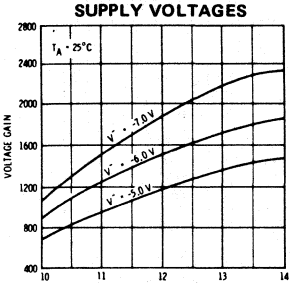
VOLTAGE TRANSFER CHARACTERISTIC



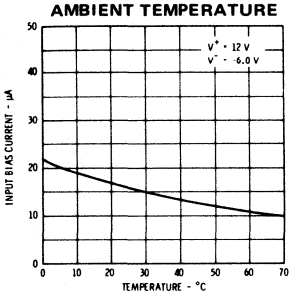
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



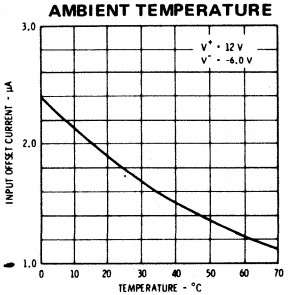
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



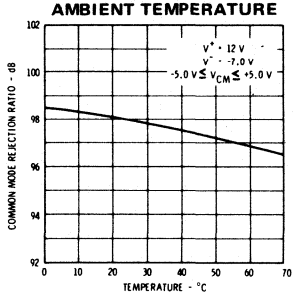
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



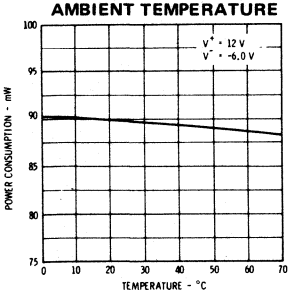
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



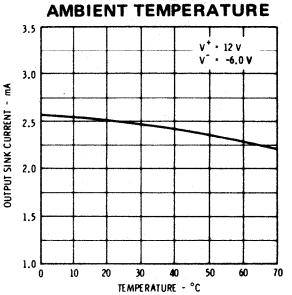
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



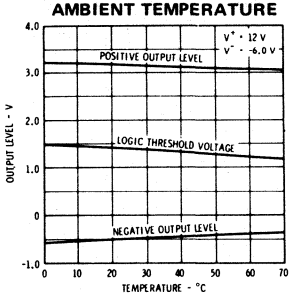
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



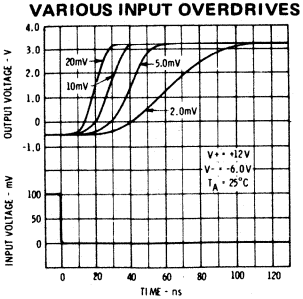
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



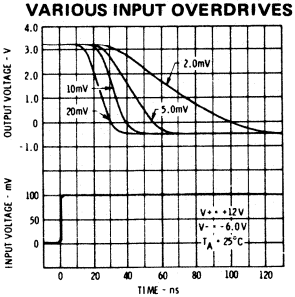
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



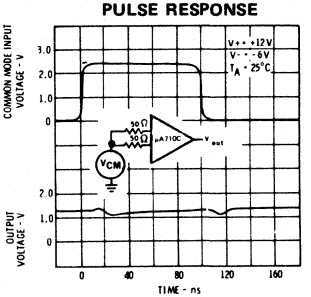
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



μA711
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

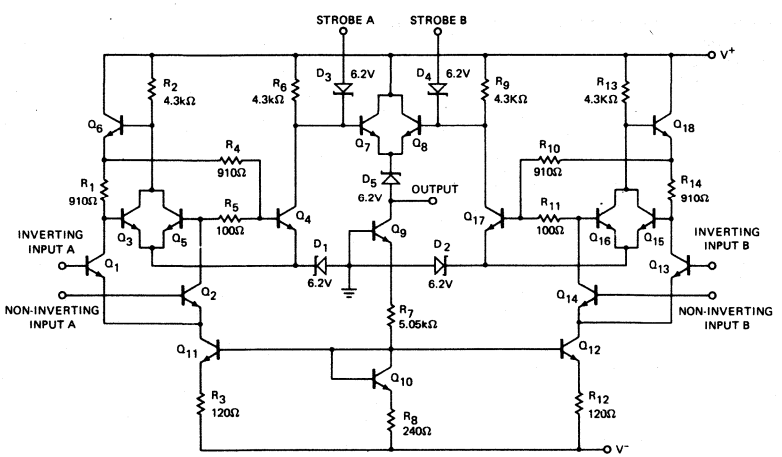
GENERAL DESCRIPTION – The μA711 is a Dual, Differential Voltage Comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-Go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed using the Fairchild Planar* epitaxial process.

- **FAST RESPONSE TIME . . . 40 ns TYPICAL**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **10μA MAXIMUM OFFSET CURRENT**
- **INDEPENDENT STROBING OF EACH COMPARATOR**

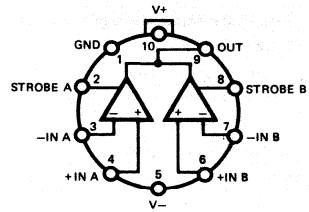
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14 V
Negative Supply Voltage	−7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (μA711)	−55°C to +125°C
Commercial (μA711C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Metal Can, Hermetic DIP and Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEWS)
PACKAGE OUTLINES 5F 5N
PACKAGE CODES H H

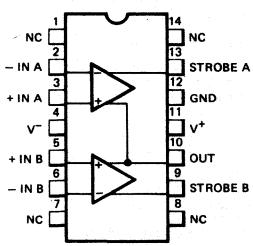


NOTE: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA711	μA711HM
μA711C	μA711HC

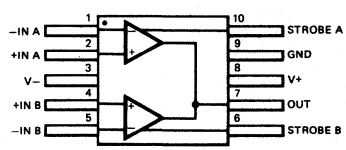
14-LEAD DIP
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA711	μA711DM
μA711C	μA711DC
μA711C	μA711PC

10-LEAD FLATPAK
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA711	μA711FM

Notes on following page.

*Planar is a patented Fairchild process.

μA711

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V, V^- = −6.0 V unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OUT} = +1.4 V, $R_S \leq 200\ \Omega$, V_{CM} = 0		1.0	3.5	mV
	V_{OUT} = +1.4 V, $R_S \leq 200\ \Omega$		1.0	5.0	mV
Input Offset Current	V_{OUT} = 1.4 V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = −7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10$ mV, I_O = 5mA	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10$ mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3$ V	−1.0		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{STROBE} = 100 mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		8.6		mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		3.9		mA
Power Consumption			130	200	mW

The following specifications apply for $-55° C \leq T_A \leq +125°C$:

Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, V_{CM} = 0			4.5	mV
	$R_S \leq 200\ \Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP, and 7.1 mW/°C for the Flatpak.
2. The response time specified (see definitions) is for a 100 mV step input with 5 mV overdrive.
3. The input offset voltage is specified for a logic threshold as follows:
   711: 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C
   711C: 1.5 V at 0°C, 1.4 V at +25°C, 1.2 V at +70°C

μA711C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V, V^- = −6.0 V unless otherwise specified)

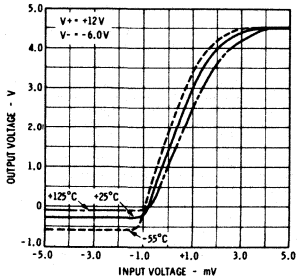
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OUT} = +1.4 V, $R_S \leq$200 Ω, V_{CM} = 0		1.0	5.0	mV
	V_{OUT} = +1.4 V, $R_S \leq$200 Ω		1.0	7.5	mV
Input Offset Current	V_{OUT} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = −7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq$10 mV		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq$10 mV, I_O = 5 mA	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq$10 mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq$0.3 V	−1.0		0	V
Output Sink Current	$V_{IN} \geq$10 mV, $V_{OUT} \geq$0	0.5	0.8		mA
Strobe Current	V_{STROBE} = 100 mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} Gnd, Inverting Input = +10mV		8.6		mA
Negative Supply Current	V_{OUT}Gnd, Inverting Input = +10mV		3.9		mA
Power Consumption			130	230	mW

The following specifications apply for 0° C ≤ T_A ≤ +70° C:

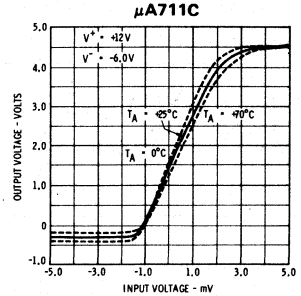
Input Offset Voltage (Note 3)	$R_S \leq$ 200 Ω, V_{CM} = 0			6.0	mV
	$R_S \leq$ 200 Ω			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

TYPICAL PERFORMANCE CURVES FOR μA711 AND μA711C

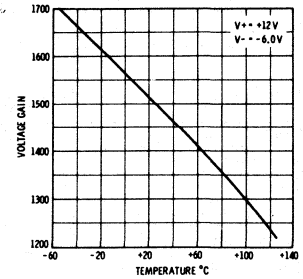
VOLTAGE TRANSFER CHARACTERISTIC μA711



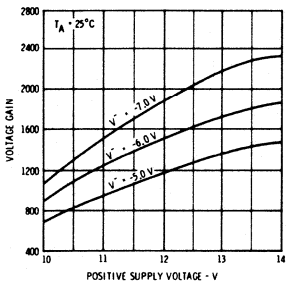
VOLTAGE TRANSFER CHARACTERISTIC μA711C



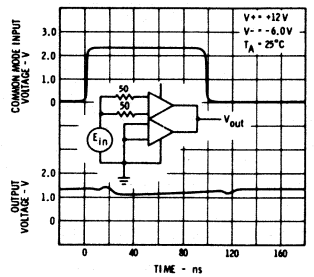
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



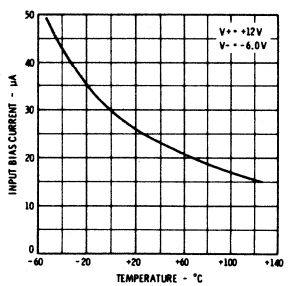
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



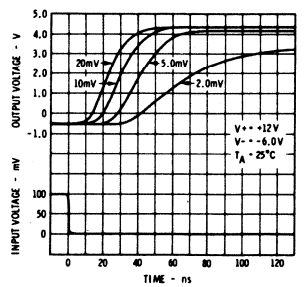
COMMON MODE PULSE RESPONSE



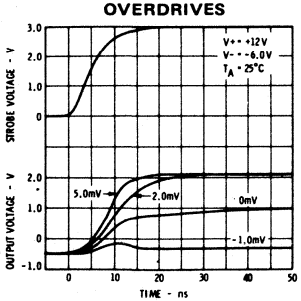
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



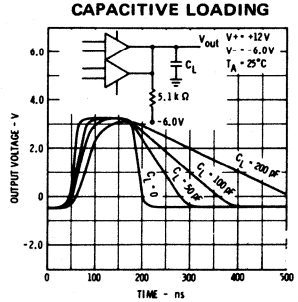
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



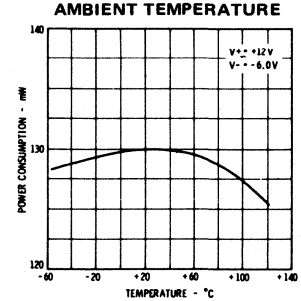
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



μA734

PRECISION VOLTAGE COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

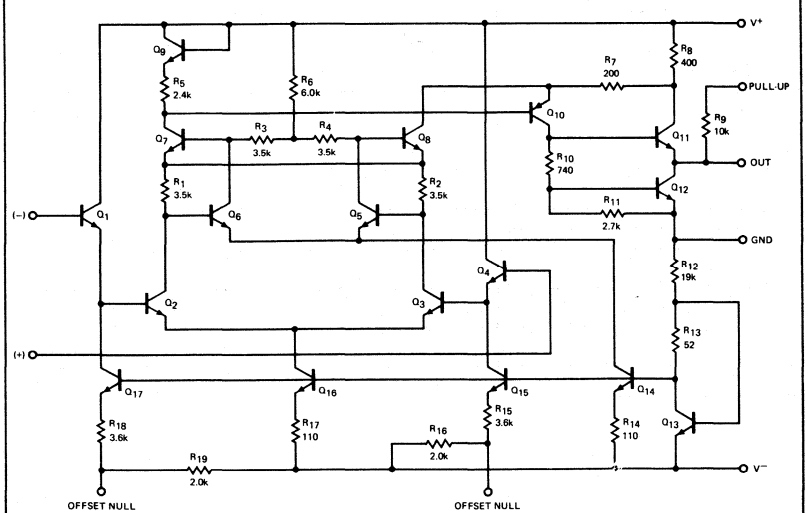
GENERAL DESCRIPTION – The μA734 is a Precision Voltage Comparator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is specifically designed for high accuracy level sensing and measuring applications. The μA734 is extremely useful for analog-to-digital converters with twelve bit accuracies and one mega-bit conversion rates. Maximum resolution is obtained by high gain, low input offset current, and low input offset voltage. Its superior temperature stability can be improved by offset nulling which further reduces offset voltage drift. Balanced or unbalanced supply operation and standard TTL logic compatibility enhance the μA734's versatility.

- **CONSTANT INPUT IMPEDANCE OVER DIFFERENTIAL INPUT RANGE**
- **HIGH INPUT IMPEDANCE – 55 MΩ**
- **LOW DRIFT – 3.5 μV/°C**
- **HIGH GAIN – 60 k**
- **BALANCED OFFSET NULL CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE – ±5 V to ±18 V**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

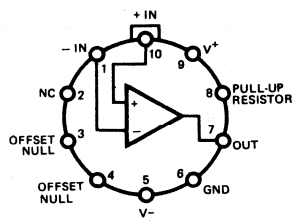
Supply Voltage	±18 V
Peak Output Current	10 mA
Differential Input Voltage	±10 V
Input Voltage Range (Note 1)	±13 V
Voltage Between Offset Null and V⁻	±0.5 V
Internal Power Dissipation (Note 2)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA734)	−55°C to +125°C
Commercial (μA734C)	0°C to +70°C
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Lead Temperature (Soldering, 60 s Max)	300°C

EQUIVALENT CIRCUIT



Notes on following pages.

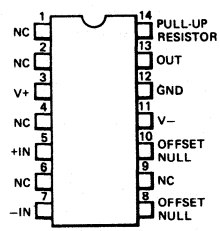
CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5N
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA734	μA734HM
μ734C	μA734HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA734	μA734DM
μA734C	μA734DC

*Planar is a patented Fairchild process.

±15 VOLT OPERATION FOR μA734C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Pin 8 tied to +15 V, unless otherwise specified) Note 3.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1 [1]	5.0	mV
Input Offset Current			3.5	25	nA
Input Bias Current			30	100	nA
Input Resistance		7.0	55		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	60 k		V/V
Positive Supply Current — Output LOW			4.0	5.0	mA
Negative Supply Current — Output LOW			1.5	2.0	mA
Power Consumption — Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns

The following specifications apply for 0°C ≤ T_A ≤ +70°C

Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.2	7.5	mV
Input Offset Current			4.0	45	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50\ \Omega$		3.5	20	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +70°C		0.02	0.3	nA/°C
	T_A = +25°C to 0°C		0.05	0.75	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leq 50\ k\Omega$		6.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA	7.0			V
	I_{OUT} = 0.080 mA, V_S = +5.0 V	2.4		5.0	V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current — Output LOW				7.0	mA
Negative Supply Current — Output LOW				2.5	mA
Power Dissipation — Output LOW				145	mW

±15 VOLT OPERATION FOR μA734

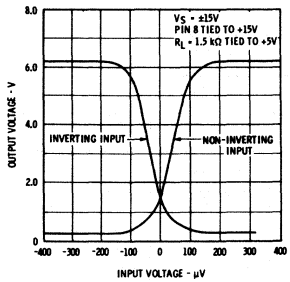
ELECTRICAL CHARACTERISTICS (T_A = 25°C, Pin 8 tied to +15 V, unless otherwise specified) Note 3.

PARAMETERS	CONDITIONS	MIN	YP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.9	3.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			28	50	nA
Input Resistance		20	60		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	70 k		V/V
Positive Supply Current — Output LOW			4.0	5.0	mA
Negative Supply Current — Output LOW			1.5	2.0	mA
Power Consumption — Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	4.0	mV
Input Offset Current			3.0	20	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50\ k\Omega$		2.5	15	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +125°C T_A = +25°C to −55°C		0.01 0.05	0.1 0.4	nA/°C nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leq 50\ k\Omega$		5.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA I_{OUT} = 0.080 mA, V_8 = +5.0 V	7.0 2.4		 5.0	V V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current — Output LOW				7.0	mA
Negative Supply Current — Output LOW				2.5	mA
Power Dissipation — Output LOW				145	mW

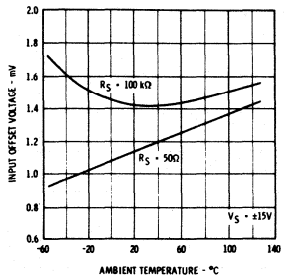
NOTES:
1. Rating applies for ±15 V supplies. For other supply voltages the rating is within 2 V of either supply.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for DIP.
3. Pin numbers refer to metal can package.

TYPICAL PERFORMANCE CURVES FOR μA734 AND μA734C (Note 2)

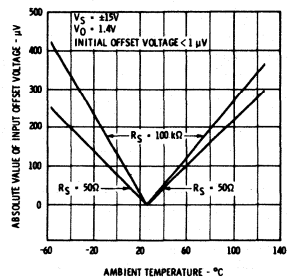
TRANSFER CHARACTERISTICS



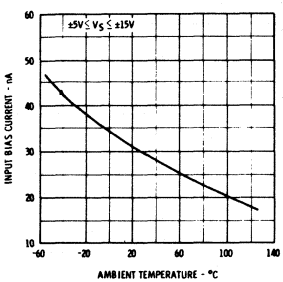
UN-NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



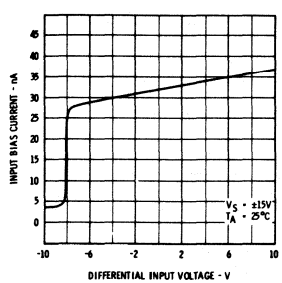
INPUT OFFSET VOLTAGE CHANGE AS A FUNCTION OF AMBIENT TEMPERATURE - NULLED TO ZERO AT 25°C



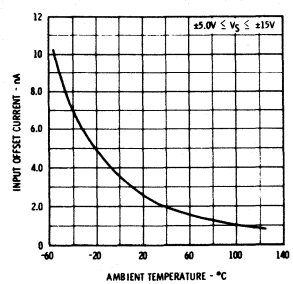
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



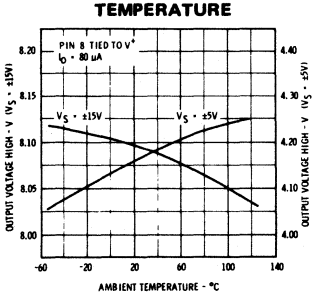
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



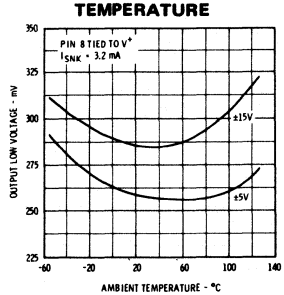
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



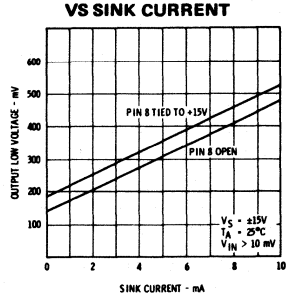
OUTPUT HIGH VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



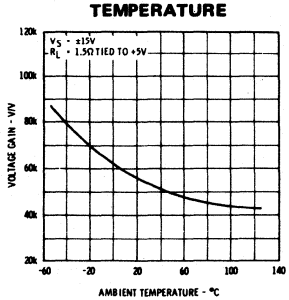
OUTPUT LOW VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



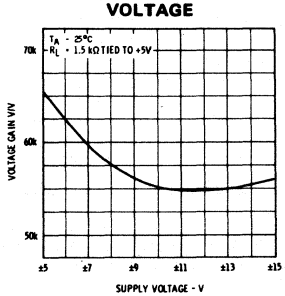
OUTPUT VOLTAGE LOW VS SINK CURRENT



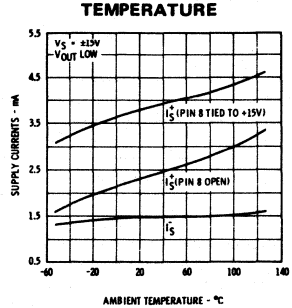
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

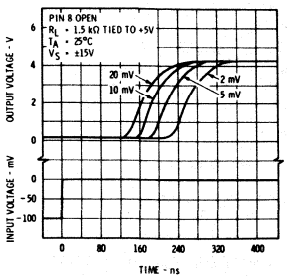


POSITIVE AND NEGATIVE SUPPLY CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE

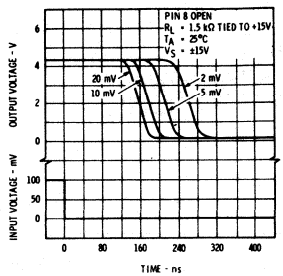


TYPICAL PERFORMANCE CURVES FOR μA734 AND μA734C (Note 2)

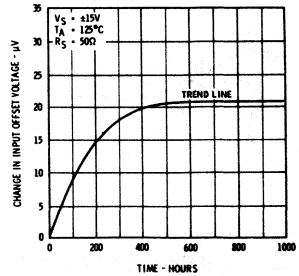
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



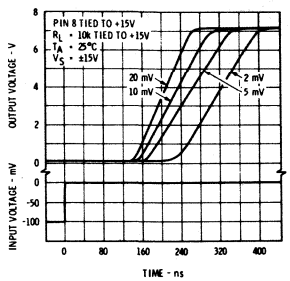
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



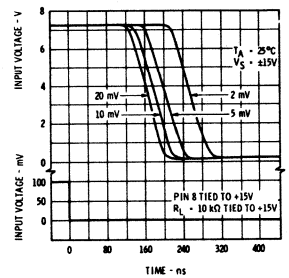
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



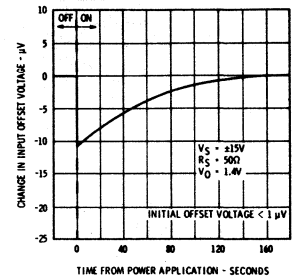
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



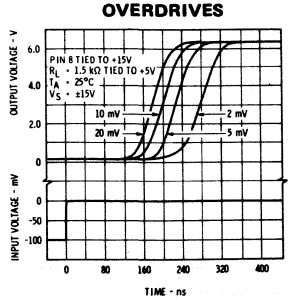
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



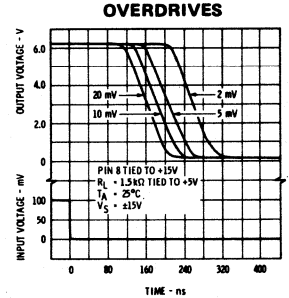
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



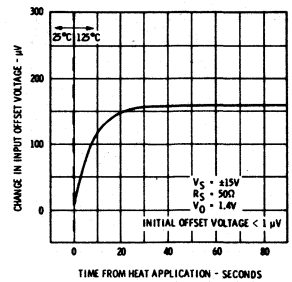
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



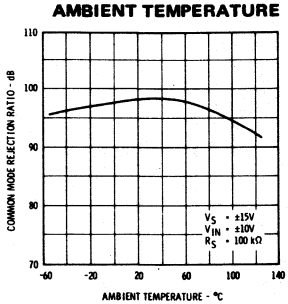
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



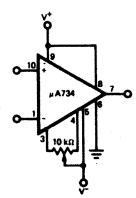
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



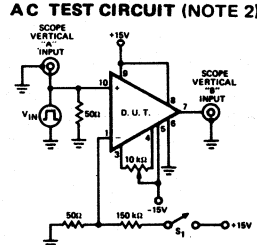
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



OFFSET NULL CIRCUIT (NOTE 2)



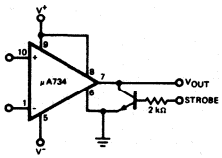
AC TEST CIRCUIT (NOTE 2)



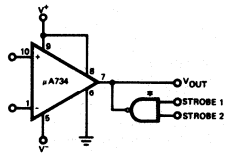
V_{IN} = -100 mV, 100 kHz

TYPICAL APPLICATIONS (Note 2)

STROBE CIRCUITRY

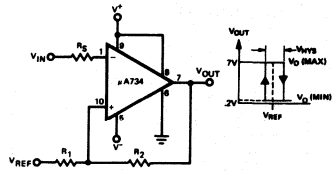


ALTERNATE STROBE CIRCUITRY



* 1/2 9944

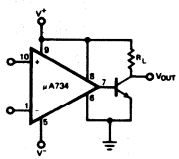
LEVEL DETECTOR WITH HYSTERESIS



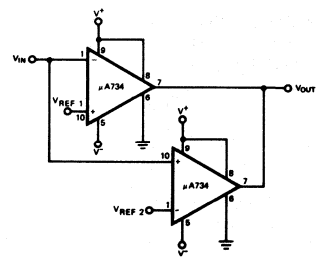
$$R_S = \frac{R_1 R_2}{R_1 + R_2} \text{ FOR MINIMUM OFFSET}$$

$$V_{HYS} = \frac{R_1 [V_{O\,MAX} - V_{O\,MIN}]}{R_1 + R_2}$$

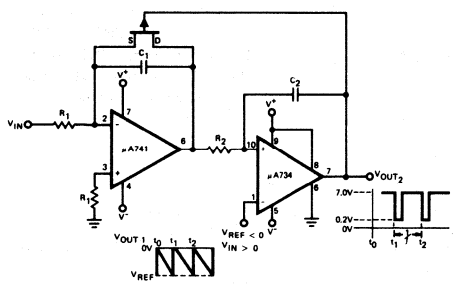
HIGH POWER OUTPUT CIRCUITS



PRECISION DUAL LIMIT GO-NO GO TESTER

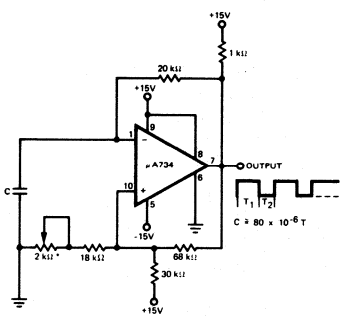


VOLTAGE CONTROLLED OSCILLATOR



$$f = \frac{V_{IN}}{|V_{REF}| R_1 C_1} \qquad R_2 C_2 > \frac{|V_{REF}| C_1}{I_{DSS}}$$

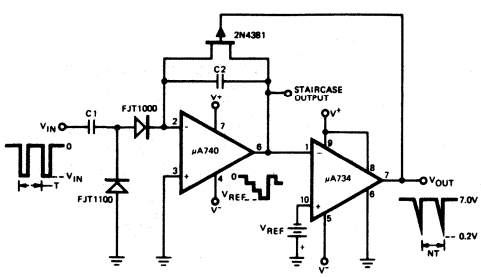
FREE RUNNING OSCILLATOR



$C \approx 80 \times 10^{-6} T$

* Adjusts $\frac{T_1}{T_2}$

FREQUENCY DIVIDER & STAIRCASE GENERATOR

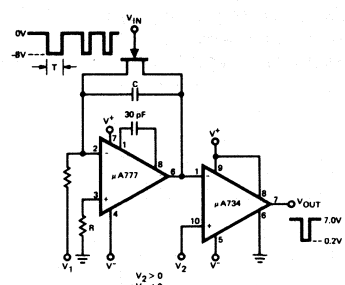


$$|V_{REF}| = 2V_D + N\left[3.5T + 2V_D - \frac{C_1 V_{IN}}{C_2}\right]$$

T In Seconds

V_D for FJT 1000 ≈ 0.31V

PULSE WIDTH DISCRIMINATOR

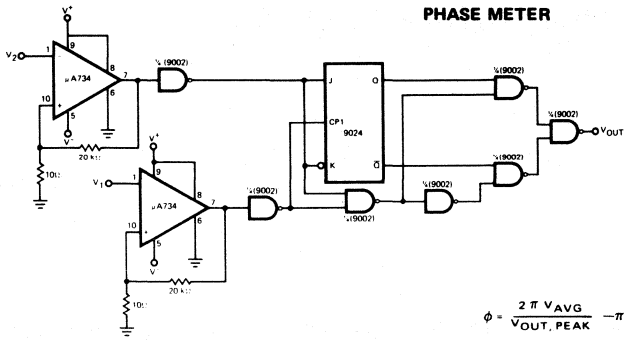


V_{OUT} Pulse Appears

Whenever $T > \frac{R C V_2}{|V_1|}$

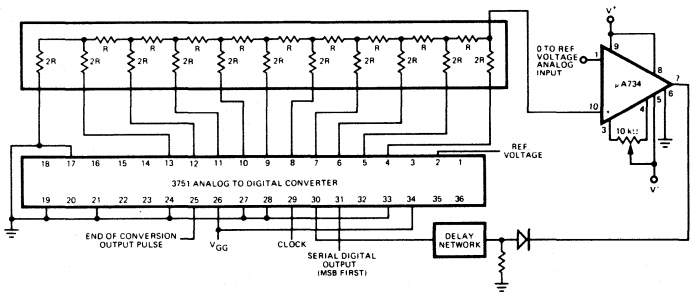
TYPICAL APPLICATIONS (Note 2)

PHASE METER



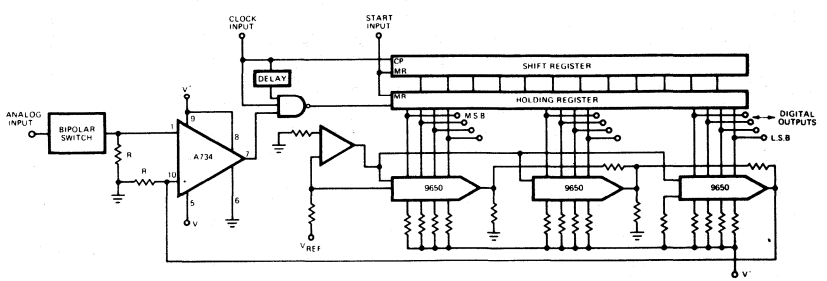
$$\phi = \frac{2\pi V_{AVG}}{V_{OUT,PEAK}} - \pi$$

12-BIT A/D CONVERTER



NO. OF BITS	R VALUE
8	12.5kΩ
9	25kΩ
10	50kΩ
12	200kΩ

12-BIT A/D CONVERTER



μA760
HIGH SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

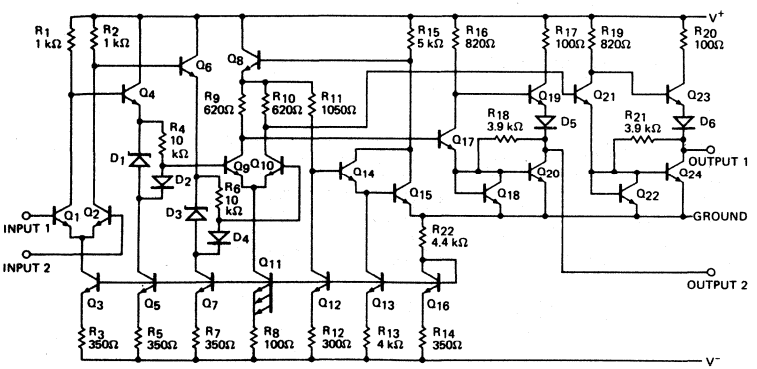
GENERAL DESCRIPTION – The μA760 is a Differential Voltage Comparator offering considerable speed improvement over the μA710 family and operation from symmetric supplies of from ±4.5 V to ±6.5 V. The μA760 can be used in high speed analog to digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The μA760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

- **GUARANTEED HIGH SPEED – 25 ns MAX**
- **GUARANTEED DELAY MATCHING ON BOTH OUTPUTS**
- **COMPLEMENTARY TTL COMPATIBLE OUTPUTS**
- **HIGH SENSITIVITY**
- **USES STANDARD SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

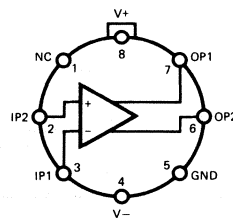
Positive Supply Voltage	+8 V
Negative Supply Voltage	-8 V
Peak Output Current	10 mA
Differential Input Voltage	±5 V
Input Voltage	$V+ \geq V_{IN} \geq V-$
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA760)	-55°C to 125°C
Commercial (μA760C)	0°C to 70°C
Storage Temperature Range	
Metal Can and DIP	-65°C to 150°C

EQUIVALENT CIRCUIT



Notes on following page.

CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

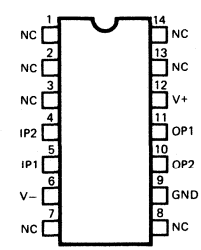


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA760	μA760HM
μA760C	μA760HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA760	μA760DM
μA760C	μA760DC

μA760

ELECTRICAL CHARACTERISTICS (V_S = ±4.5V to ±6.5V, T_A = −55°C to +125°C, T_A = 25°C for typical figures unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	Note 2, T_A = 25°C			7.5	ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			7.5	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = −55°C to T_A = +125°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +125°C		2.0		nA/°C
	T_A = 25°C to T_A = −55°C		7.0		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA				
	V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.4	3.0		V
Output LOW Voltage (either output)	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	32	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

9

μA760C

ELECTRICAL CHARACTERISTICS (V_S = ±4.5V to ±6.5V, T_A = 0°C to +70°C, T_A = 25°C for typical figures unless otherwise specified.)

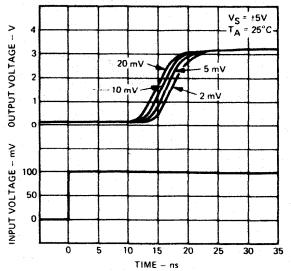
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	Note 2, T_A = 25°C			10	ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			10	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = 0°C to T_A = +70°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +70°C		5.0		nA/°C
	T_A = 25°C to T_A = 0°C		10		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA				
	V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.5	3.0		V
Output LOW Voltage (either output)	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	34	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

NOTES

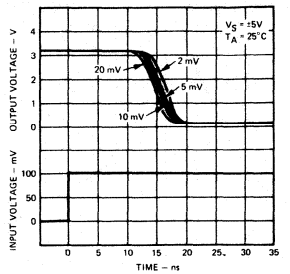
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and 8.3 mW/°C for the DIP.
2. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
3. Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
4. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

TYPICAL PERFORMANCE CURVES FOR μA760 AND μA760C

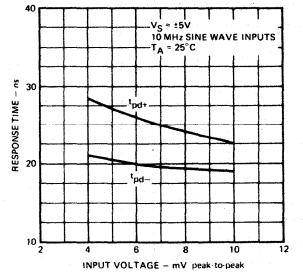
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



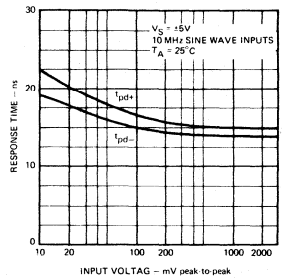
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



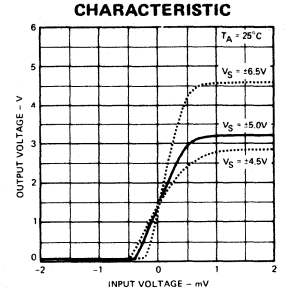
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



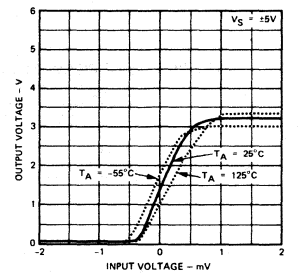
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



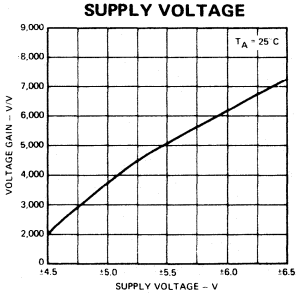
VOLTAGE TRANSFER CHARACTERISTIC



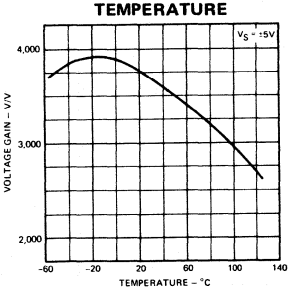
VOLTAGE TRANSFER CHARACTERISTIC



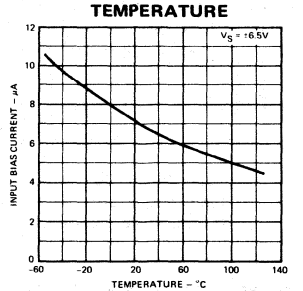
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



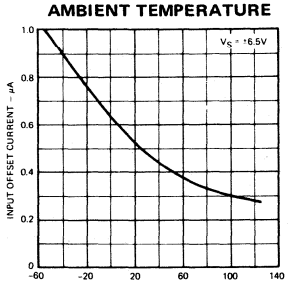
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



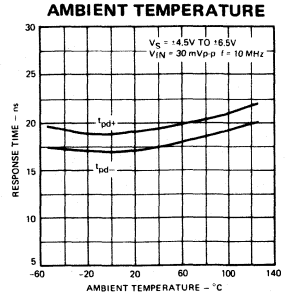
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



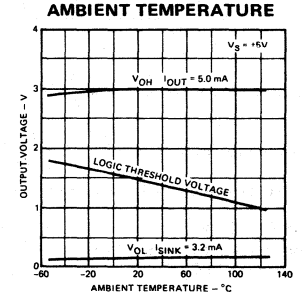
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



RESPONSE TIME AS A FUNCTION OF AMBIENT TEMPERATURE



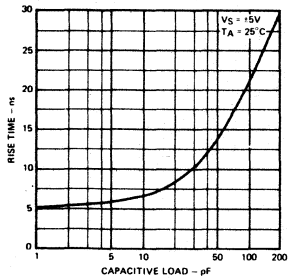
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



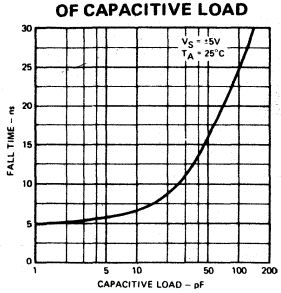
9

TYPICAL PERFORMANCE CURVES FOR μA760 AND μA760C (Cont'd)

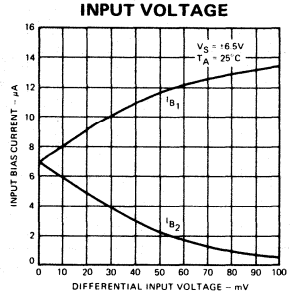
RISE TIME AS A FUNCTION OF CAPACITIVE LOAD



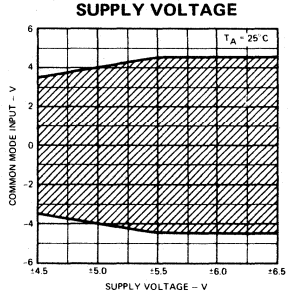
FALL TIME AS A FUNCTION OF CAPACITIVE LOAD



INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



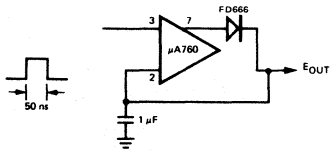
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



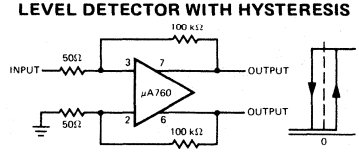
APPLICATIONS

Pin numbers shown are only for Metal Can

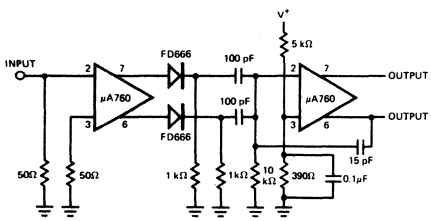
FAST POSITIVE PEAK DETECTOR



LEVEL DETECTOR WITH HYSTERESIS

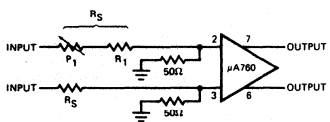


ZERO CROSSING DETECTOR



Total Delay = 30 ns
Input frequency = 300 Hz to 3 MHz
Minimum input voltage = 20 mVpk-pk

LINE RECEIVER WITH HIGH COMMON MODE RANGE



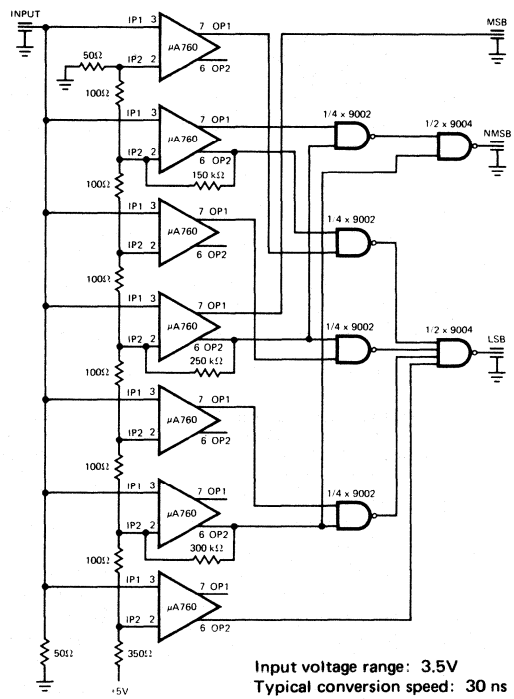
Common mode range = $\pm 4 \times \frac{RS}{50}$ V

Differential Input sensitivity = $5 \times \frac{RS}{50}$ mV

P_1 must be adjusted for optimum common mode rejection.

For $R_S = 200\Omega$
Common mode range = ±16V
Sensitivity = 20 mV

HIGH SPEED 3-BIT A/D CONVERTER



Input voltage range: 3.5V
Typical conversion speed: 30 ns

μA775

QUAD COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA775 Quad Comparator consists of four independent voltage comparators designed specifically to operate from a single power supply over a wide range of voltages. These comparators have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

Applications include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range V_{CO}; MOS clock timers; multivibrators and high voltage digital logic gates.

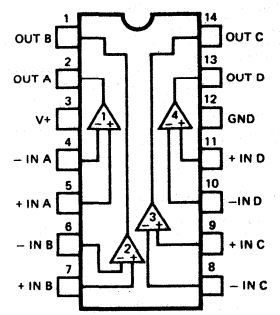
- **SINGLE SUPPLY OPERATION – +2.0 V TO +36 V**
- **DUAL SUPPLY OPERATION – ±1.0 V TO ±18 V**
- **ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL**
- **LOW CURRENT DRAIN – 800 μA TYP**
- **COMPATIBLE WITH ALL FORMS OF LOGIC**
- **LOW INPUT BIAS CURRENT – 25 nA TYP**
- **LOW INPUT OFFSET CURRENT – 25 nA MAX(μA775), 50 nA MAX(μA775C)**
- **LOW OFFSET VOLTAGE – 5 mV MAX**
- **INPUT COMMON MODE RANGE INCLUDES GROUND**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	36 V or ±18 V
Differential Input Voltage	$\pm V_S$
Common Mode Input Voltage Range (Note 1)	−0.3 V to $+V_S$
Output Short Circuit Duration to GND (Note 2)	Indefinite
Internal Power Dissipation (Note 3)	670 mW
Storage Temperature Range	
Molded DIP – 9A	−55°C to +125°C
Hermetic DIP – 6A	−65°C to +150°C
Operating Temperature Range	
μA775 (Miltary	−55°C to +125°C
μA775C (Commercial)	0°C to 70°C
Lead Temperature (Soldering)	
Molded DIP – 9A (10 s)	260°C
Hermetic DIP – 6A (60 s)	300°C

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

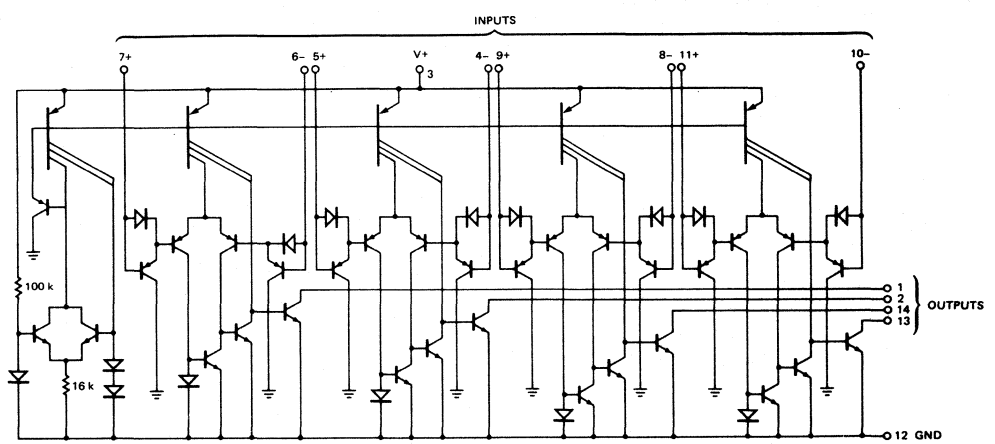
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA775	μA775DM
μA775C	μA775DC
μA775C	μA775PC

EQUIVALENT CIRCUIT



μA775

ELECTRICAL CHARACTERISTICS (V_S = +5 V, T_A = 25°C unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OUT} = +1.4 V, R_S = 50 Ω		2.0	5.0	mV
Average Input Offset Voltage Temperature Coefficient			10		μV/°C
Input Bias Current (Note 4)			25	100	nA
Input Offset Current			±3.0	±25	nA
Input Common Mode Range		0		$(V_{S+}) - 1.5$	V
Input Resistance		0.4	2.0		MΩ
Transconductance			13		mhos
Voltage Gain	$R_L \geq 15$ kΩ		200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 5 V, R_L = 5.1 kΩ		300		ns
Response Time	100 mV Input Step, R_L = 5.1 kΩ, 5 mV Overdrive, V_{RL} = 5 V		1.3		μs
Output Leakage Current	$V_{IN(+)} \geq +1.0$ V, $V_{IN(-)}$ = 0, V_{OUT} = 5 V		0.1		nA
Low Output Voltage (V_{OL})	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4.0$ mA		250	400	mV
Output Sink Current	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $V_{OUT} \leq 1.5$ V	6.0	16		mA
Supply Current			0.8	2.0	mA
Channel Separation			110		dB
The following specifications apply for $-55°C \leq T_A \leq 125°C$					
Input Offset Voltage	V_{OUT} = +1.4 V, R_S = 50 Ω			9.0	mV
Input Bias Current (Note 4)				300	nA
Input Offset Current				100	nA
Input Common Mode Range		0		$(V_{S+}) - 2$	V
Differential Input Voltage Range		$\pm V_S$			V
Common Mode Rejection Ratio		70			dB
Output Leakage Current	$V_{IN(+)} \geq +1.0$ V, $V_{IN(-)}$ = 0, V_{OUT} = 30 V			1.0	μA
Low Output Voltage (V_{OL})	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4.0$ mA			600	mV
Output Sink Current	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $V_{OUT} \leq 1.5$ V	4.5			mA
Supply Current				3.0	mA
Power Supply Rejection Ratio		70			dB

NOTES:
1. If either (+) or (−) input of any comparator goes more than several tenths of a volt below ground, a parasitic transistor turns on causing high input current and possible faulty outputs.
2. Output short circuit to V+ may cause damage to device. The maximum output current is approximately 20 mA independent of the magnitude of V+.
3. Rating applies to ambient temperature up to 70°C, above 70°C derate linearly at 8.3 mW/°C.
4. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

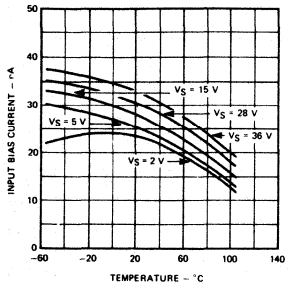
μA775C

ELECTRICAL CHARACTERISTICS (V_S = +5 V, T_A = 25°C unless otherwise specified)

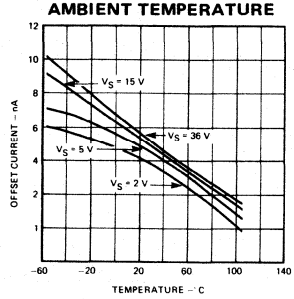
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OUT} = +1.4 V, R_S = 50 Ω		2.0	5.0	mV
Average Input Offset Voltage Temperature Coefficient			10		μV/°C
Input Bias Current (Note 4)			25	250	nA
Input Offset Current			±5.0	±50	nA
Input Common Mode Range		0		$(V_{S+}) - 1.5$	V
Input Resistance		0.15	2.0		MΩ
Transconductance			13		mhos
Voltage Gain	$R_L \geq 15$ kΩ		200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 5 V, R_L = 5.1 kΩ		300		ns
Response Time	100 mV Input Step, R_L = 5.1 kΩ, 5 mV Overdrive, V_{RL} = 5 V		1.3		μs
Output Leakage Current	$V_{IN(+)} \geq +1.0$ V, $V_{IN(-)}$ = 0, V_{OUT} = 5 V		0.1		nA
Low Output Voltage (V_{OL})	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4.0$ mA		250	400	mV
Output Sink Current	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $V_{OUT} \leq 1.5$ V	6.0	16		mA
Supply Current			0.8	2.0	mA
Channel Separation			110		dB
The following specifications apply for $0°C \leq T_A \leq 70°C$					
Input Offset Voltage	V_{OUT} = +1.4 V, R_S = 50 Ω			9.0	mV
Input Bias Current (Note 4)				400	nA
Input Offset Current				150	nA
Input Common Mode Range		0		$(V_{S+}) - 2$	V
Differential Input Voltage Range		$\pm V_S$			V
Common Mode Rejection Ratio		70			dB
Output Leakage Current	$V_{IN(+)} \geq +1.0$ V, $V_{IN(-)}$ = 0, V_{OUT} = 30 V			1.0	μA
Low Output Voltage (V_{OL})	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4.0$ mA			500	mV
Output Sink Current	$V_{IN(-)} \geq +1.0$ V, $V_{IN(+)}$ = 0, $V_{OUT} \leq 1.5$ V	4.5			mA
Supply Current				2.5	mA
Power Supply Rejection Ratio		70			dB

TYPICAL PERFORMANCE CURVES

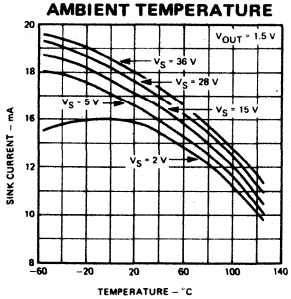
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



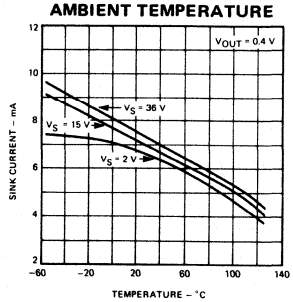
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



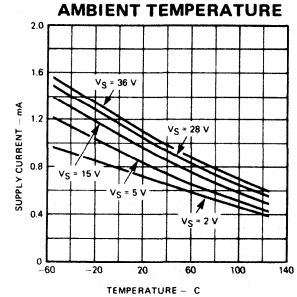
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



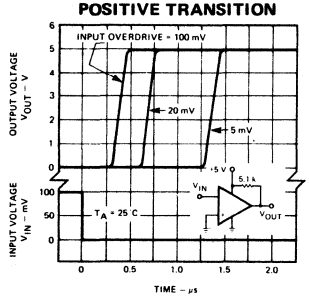
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



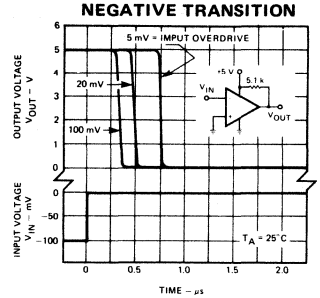
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



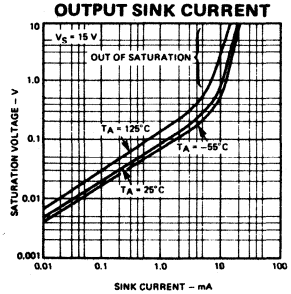
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES POSITIVE TRANSITION



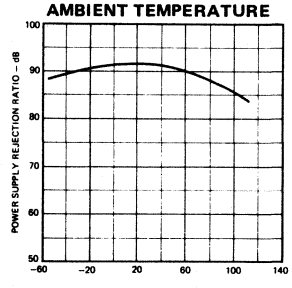
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES NEGATIVE TRANSITION



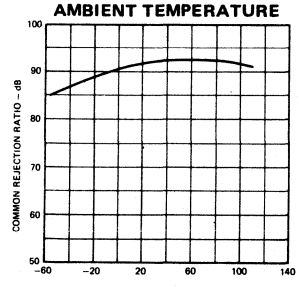
OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



POWER SUPPLY REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

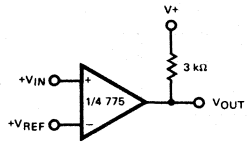


COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

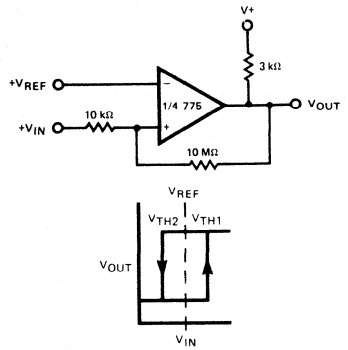


TYPICAL APPLICATIONS

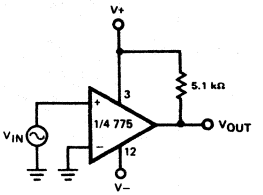
BASIC COMPARATOR



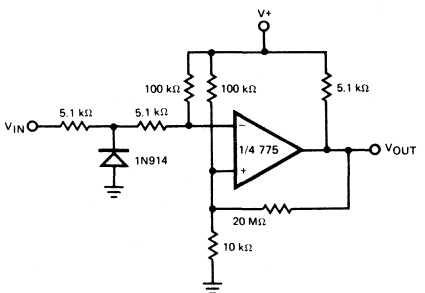
NON-INVERTING COMPARATOR WITH HYSTERESIS



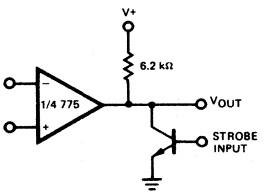
ZERO CROSSING DETECTOR (DUAL SUPPLY)



ZERO CROSSING DETECTOR (SINGLE POWER SUPPLY)

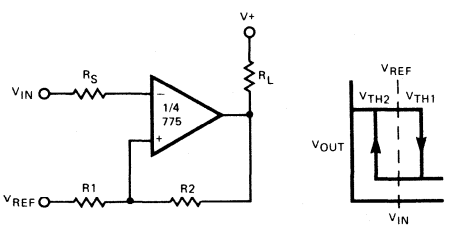


OUTPUT STROBING



*OR open-collector logic gate

COMPARATOR WITH HYSTERESIS

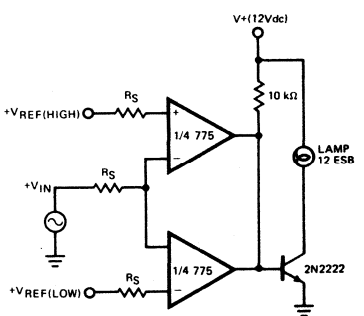


$$R_S = R1 \parallel R2$$

$$V_{TH1} = V_{REF} + \frac{(V_S - V_{REF})\,R1}{R1 + R2 + R_L}$$

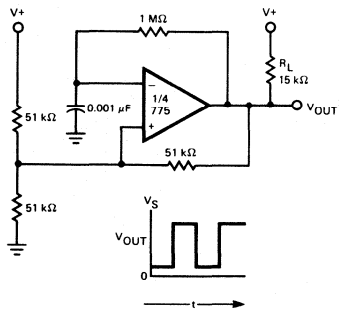
$$V_{TH2} = V_{REF} - \frac{(V_{REF} - V_{OUT\ LOW})\,R1}{R1 + R2 + R_L}$$

LIMIT COMPARATOR

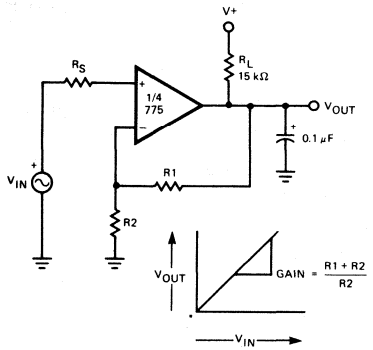


TYPICAL APPLICATIONS(Cont'd)

FREE RUNNING SQUARE WAVE OSCILLATOR

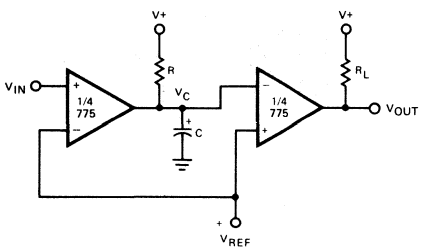


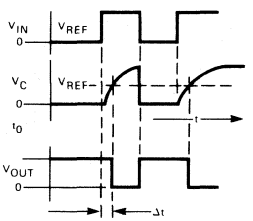
THE COMPARATOR AS AN OPERATIONAL AMPLIFIER (NON-INVERTING MODE)



*Input common mode voltage range includes ground (0 V) and V_{OUT} can go to approximately 0 V.

TIME DELAY GENERATOR





"ON" for $t \geq t_0 + \Delta t$
where:
$$\Delta t = RC \ln\left(\frac{V_{REF}}{V_{CC}}\right)$$

μA3302

QUAD COMPARATOR

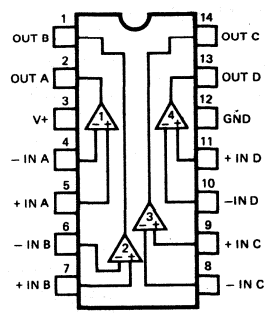
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3302 Quad Comparator consists of four independent voltage comparators designed specifically to operate from a single power supply over a wide range of voltages. These comparators have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

Applications include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range V_{CO}; MOS clock timers; multivibrators and high voltage digital logic gates.

- **SINGLE SUPPLY OPERATION – +2.0 TO +28 Vdc**
- **DIFFERENTIAL INPUT VOLTAGE – $\pm V_S$**
- **COMPARES VOLTAGES AT GROUND POTENTIAL**
- **LOW CURRENT DRAIN – 700 μA TYPICAL @ V_S +5.0 TO +28 Vdc.**
- **COMPATIBLE WITH ALL FORMS OF LOGIC**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



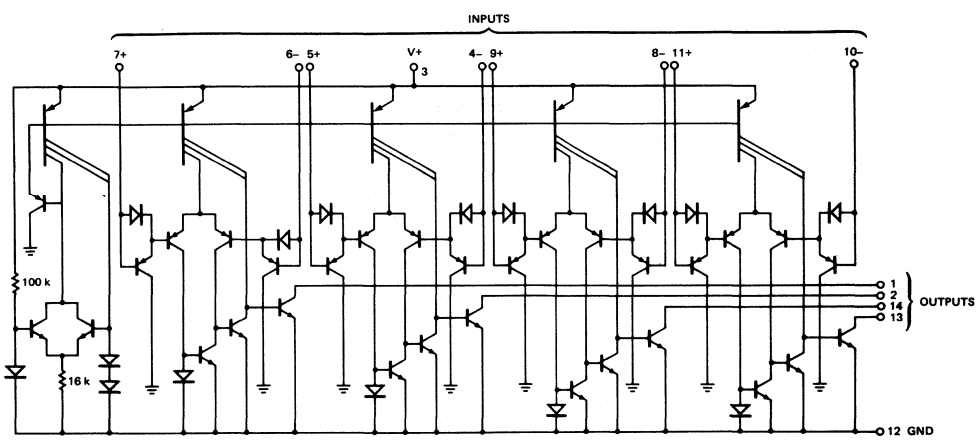
ORDER INFORMATION

TYPE	PART NO.
μA3302	μA3302P

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	+2.0 to +28 V
Output Sink Current (Note 1)	20 mA
Differential Input Voltage	$\pm V_S$
Common Mode Input Voltage Range (Note 2)	–0.3 to +V_S
Internal Power Dissipation (Note 3)	670 mW
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_S = +15 Vdc, T_A = 25°C, each comparator unless otherwise noted.)

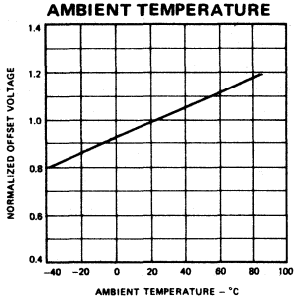
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{REF} = 1.2 V		3.0	20	mV
Input Offset Current			3.0		nA
Input Bias Current			30	500	nA
Voltage Gain	R_L = 15 kΩ	2000	30,000		V/V
Transconductance			2.0		mhos
Differential Input Voltage Range		±V_S			V
Output Leakage Current	Output Voltage HIGH			1.0	μA
Negative Output Voltage	I_S = 2.0 mA, V_S = +5.0 to 28 V		150	400	mV
Output Sink Current	V_S = +5.0 V, V_{OL} = 400 mV		6.0		mA
Input Common Mode Range	V_S = +28 V	0-26			V
Common Mode Rejection Ratio			80		dB
Propagation Delay Time for Positive and Negative Going Pulse	R_L = 5 kΩ		2.0		μs
Slew Rate					
Negative	R_L = 15 kΩ		200		V/μs
Positive	R_L = 15 kΩ		50		V/μs
Supply Current (Total of Four Comparators)	I_S = 0, V_S = +5.0 to +28 V		0.7	1.5	mA
The following specifications apply for −40°C ≤ T_A ≤ 85°C.					
Input Offset Voltage	V_{REF} = 1.2 V			40	mV
Input Bias Current				1000	nA
Output Sink Current	V_{OL} = 800 mV	2.0			mA

NOTES:
1. Requires an external resistor, R_L, to limit current below maximum rating.
2. If either (+) or (−) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns ON causing high input current and possible faulty outputs.
3. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C.

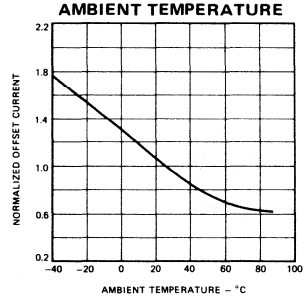
TYPICAL PERFORMANCE CURVES

(V_S = +15 V, T_A = +25°C, each comparator , unless otherwise noted)

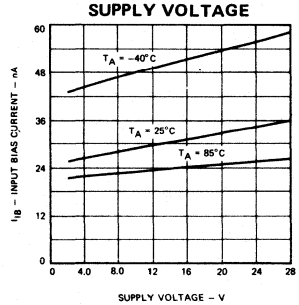
NORMALIZED OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



NORMALIZED OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

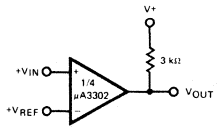


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

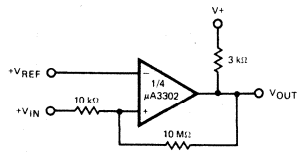


TYPICAL APPLICATIONS

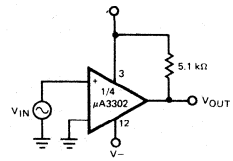
BASIC COMPARATOR



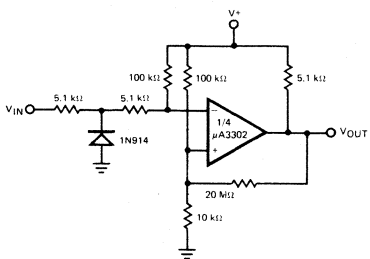
NON-INVERTING COMPARATOR WITH HYSTERESIS



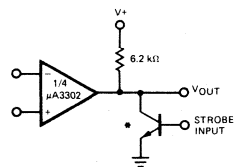
ZERO CROSSING DETECTOR



ZERO CROSSING DETECTOR(SINGLE POWER SUPPLY)

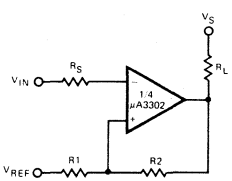


OUTPUT STROBING



*OR open-collector logic gate

COMPARATOR WITH HYSTERESIS

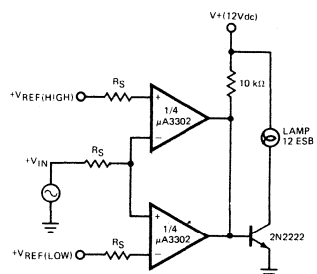


$$R_S = R1 \parallel R2$$

$$V_{th1} = V_{REF} + \frac{(V_S - V_{REF})\,R1}{R1 + R2 + R_L}$$

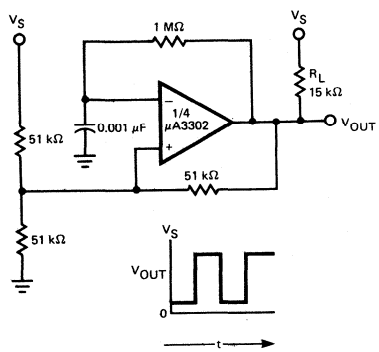
$$V_{th2} = V_{REF} - \frac{(V_{REF} - V_{OUT\ LOW})\,R1}{R1 + R2 + R_L}$$

LIMIT COMPARATOR

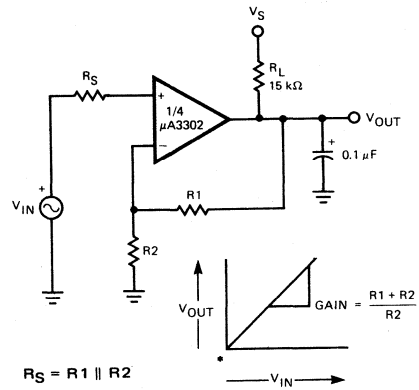


TYPICAL APPLICATIONS(Cont'd)

FREE RUNNING SQUARE WAVE OSCILLATOR



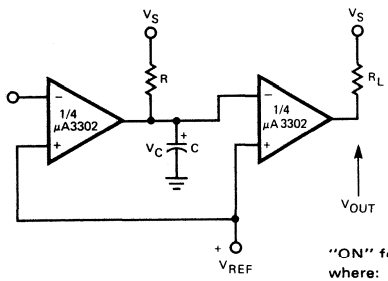
THE COMPARATOR AS AN OPERATIONAL AMPLIFIER



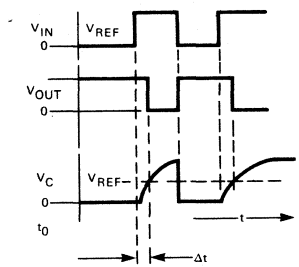
$R_S = R1 \parallel R2$

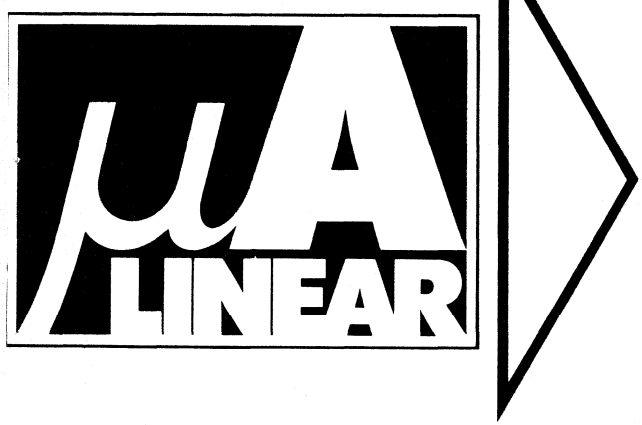
*Input common mode voltage range includes ground (0 V) and V_{OUT} can go to approximately 0 V.

TIME DELAY GENERATOR



"ON" for $t \geq t_0 + \Delta t$
where: $\Delta t = RC \ln \frac{V_{REF}}{V_{CC}}$





INDEX

TELEVISION RECEIVER AND VIDEO TAPE RECORDER

AUDIO – AM/FM RECEIVER

AUTOMOTIVE, APPLIANCE AND CALCULATOR

(See Section 11 – Interface, Section 14 – Voltage Regulators and Section 13 – Special Functions)

*Trademark CBS Inc.

μA703

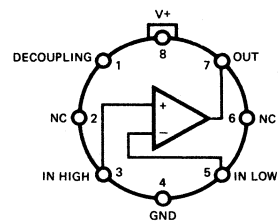
RF-IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA703 is a monolithic RF-IF Amplifier constructed using the Fairchild Planar* epitaxial process and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

- **29 mmho MINIMUM FORWARD TRANSADMITTANCE**
- **1.0 mmho/0.05 mmho MAXIMUM INPUT/OUTPUT CONDUCTANCE**
- **18 pF/4.0 pF MAXIMUM INPUT/OUTPUT CAPACITANCE**

CONNECTION DIAGRAM
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5C
PACKAGE CODE H



NOTE: Pin 4 connected to case.

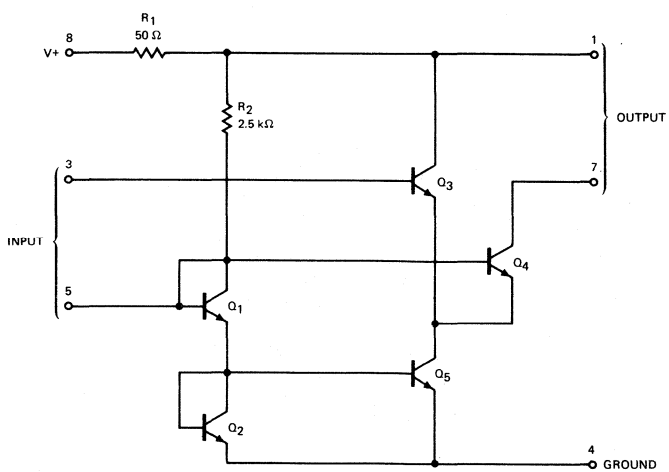
ORDER INFORMATION

TYPE	PART NO.
μA703C	μA703HC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

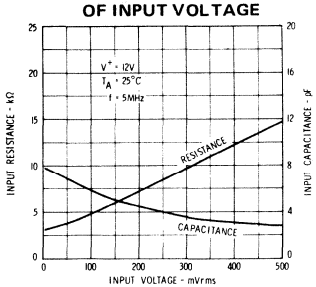
μA703C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_+ = 12 V unless otherwise specified)

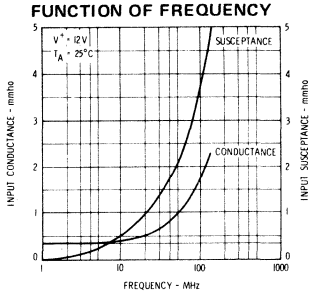
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	e_{IN} = 0		9.0	14	mA
Power Consumption	e_{IN} = 0		110	170	mW
Quiescent Output Current	e_{IN} = 0	1.5	2.5	3.3	mA
Peak-to-Peak Output Current	e_{IN} = 400 mV_{rms}, f = 1 kHz	3.0			mA
Output Saturation Voltage	I_7 = 2.5 mA			1.7	V
Forward Transadmittance	e_{IN} = 10 mV_{rms}, f = 1 kHz	29	33		mmho
Input Conductance	e_{IN} < 10 mV_{rms}, f = 10.7 MHz		0.35	1.0	mmho
Input Capacitance	e_{IN} < 10 mV_{rms}, f = 10.7 MHz		9.0	18	pF
Output Conductance	e_{OUT} = 100 mV_{rms}, f = 10.7 MHz		0.03	0.05	mmho
Output Capacitance	e_{OUT} = 100 mV_{rms}, f = 10.7 MHz		2.0	4.0	pF
Noise Figure	f = 10.7 MHz, R_S = 500 Ω		6.0		dB
	f = 100 MHz, R_S = 500 Ω		8.0		dB

TYPICAL PERFORMANCE CURVES FOR μA703C

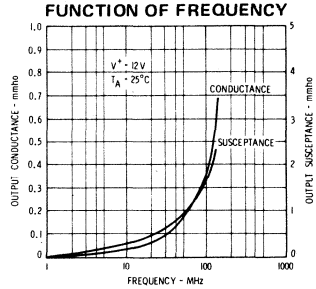
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



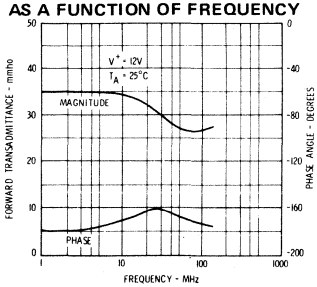
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



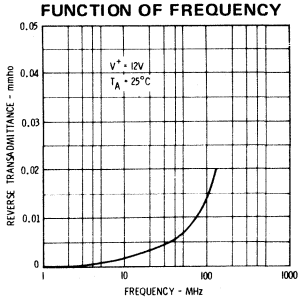
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



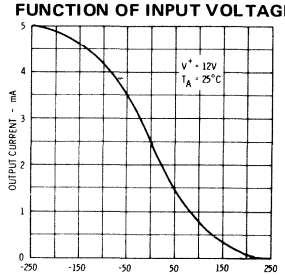
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



μA706

5 WATT AUDIO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

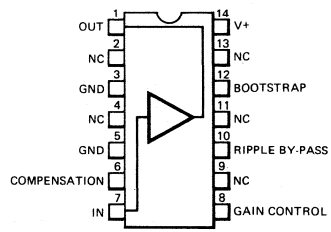
GENERAL DESCRIPTION – The μA706 monolithic 5.0 W Audio Amplifier is constructed using the Fairchild Planar* epitaxial process. It is ideally suited as an audio amplifier in automobile radios. Provided with adequate heat sinking, the circuit is optimized to provide 5.5 W (continuous output) into a 4.0 Ω speaker using a single 14 V supply. The circuit operates over the full automobile battery range of 6.0 V to 16 V. The μA706 incorporates such special features as self-centering bias, direct coupling to the input, low quiescent current, high input impedance and low distortion. Operation as a 5.0 W audio amplifier is achieved with minimal external components.

Other applications for the μA706 are home audio equipment, TV receivers and many industrial applications.

- **OUTPUT POWER 5.5 W (14 V – 4 Ω)**
- **LOW DISTORTION**
- **LOW QUIESCENT CURRENT**
- **SELF CENTERING BIAS**
- **HIGH INPUT IMPEDANCE**
- **HIGH PEAK OUTPUT CURRENT**
- **HIGH IMMUNITY TO DAMAGE FROM SHORT-CIRCUITED LOAD†**
- **PIN-FOR-PIN REPLACEMENT FOR TBA641B**

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)

PACKAGE OUTLINES 9H 9J
PACAKGE CODES AP BP

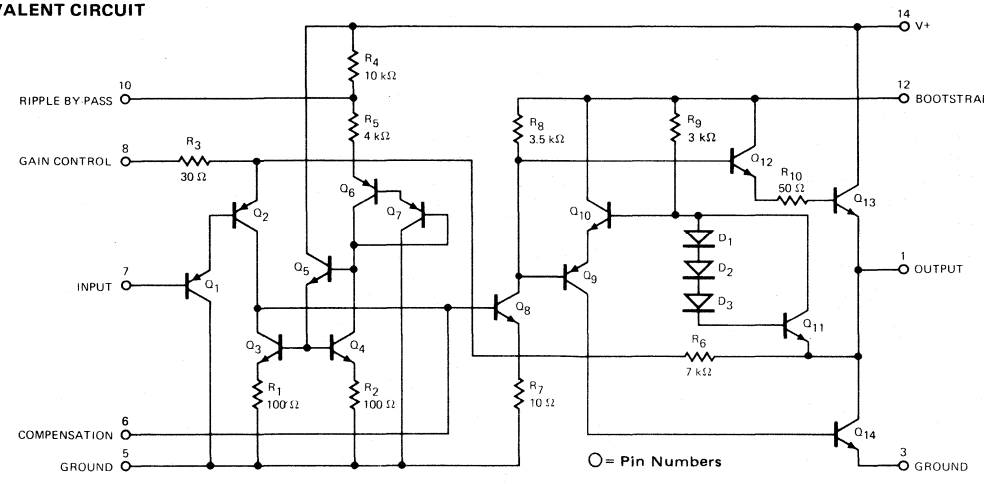


ORDER INFORMATION

TYPE	PART NO.
μA706AC	μA706APC
μA706BC	μA706BPC

†The device will withstand repetitive short circuits across the speaker load if the absolute maximum junction temperature is not exceeded.

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (No Signal)	25 V
Supply Voltage	16 V
Input Voltage	−0.5 V to V^+
Peak Output Current	2.5 A
Operating Temperature Range	−30°C to +85°C
Storage Temperature	−55°C to +125°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_C \leq 85°C$)	5 W
Power Dissipation ($T_A \leq 25°C$)	
Package Type AP	1.7 W
Package Type BP	2.3 W
Power Dissipation ($T_A \leq 85°C$)	
Package Type AP	0.9 W
Package Type BP	1.2 W

PACKAGE THERMAL RESISTANCE

Thermal Resistance, Junction to Ambient	
Package Type AP	73°C/W
Package Type BP	55°C/W
Thermal Resistance, Junction to Case	
Package Type AP	11°C/W
Package Type BP	12°C/W

μA706C

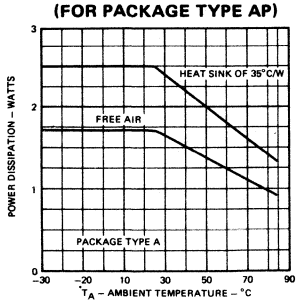
ELECTRICAL CHARACTERISTICS (V_+ = 14 V, R_L = 4 Ω, T_A = 25°C, θ_{C-A} = 13°C/W, Test Circuit 1, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Total Supply Current	P_{OUT} = 0	10	18	30	mA
Quiescent Current in Output Transistors	P_{OUT} = 0	7	15	27	mA
Input Bias Current			200	950	nA
DC Output Level	R_S = 22 kΩ	6.55	7.0	7.45	V
Voltage Gain, A_V	R_B = 0 Ω	43	46	49	dB
Output Power, P_{OUT}	THD = 10%, f = 1 kHz, A_V = 46 dB	4.5	5.5		W
Total Harmonic Distortion	f = 1 kHz, A_V = 46 dB				
	P_{OUT} = 50 mW		0.3		%
	P_{OUT} = 2.0 W		0.5		%
	P_{OUT} = 4.5 W		3.0		%
Equivalent Input Noise Voltage	R_S = 22 kΩ, B.W. = 10 kHz		3.5		μV
Total Supply Current	P_{OUT} = 4.5 W		510		mA
Input Impedance	A_V = 46 dB, f = 1 kHz		3.0		MΩ

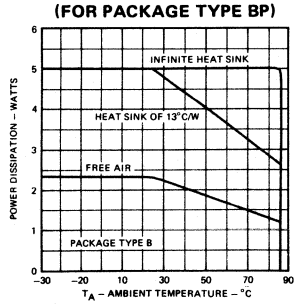
TYPICAL PERFORMANCE CURVES FOR μA706C

(T_A = 25°C, θ_{C-A} = 13°C/W, Test Circuit 1, A_V = 46 dB)

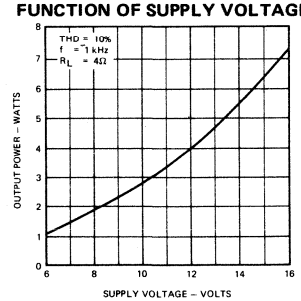
MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE AP)



MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE BP)

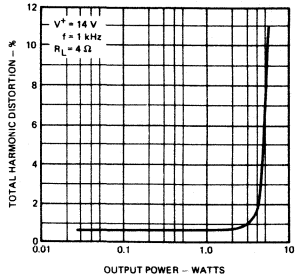


OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

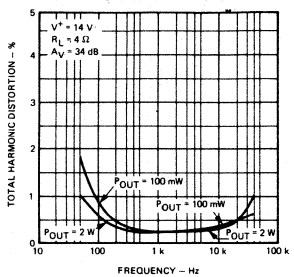


TYPICAL PERFORMANCE CURVES FOR μA706C (Cont'd)

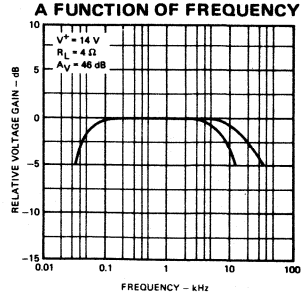
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



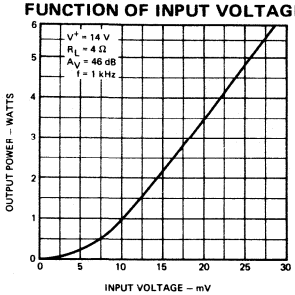
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



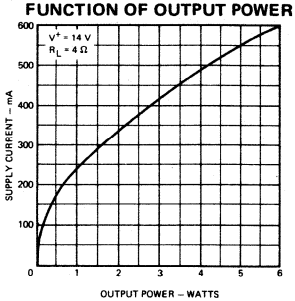
RELATIVE VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



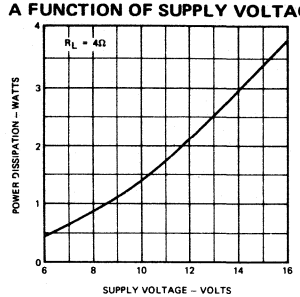
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



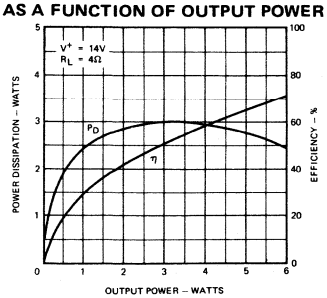
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



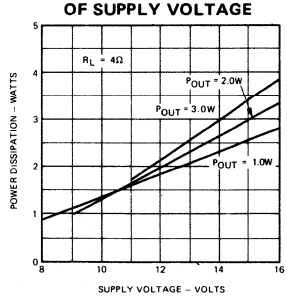
MAXIMUM POWER DISSIPATION BY THE INTEGRATED CIRCUIT AS A FUNCTION OF SUPPLY VOLTAGE



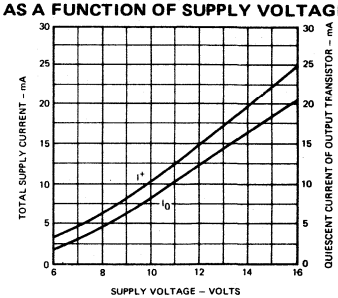
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



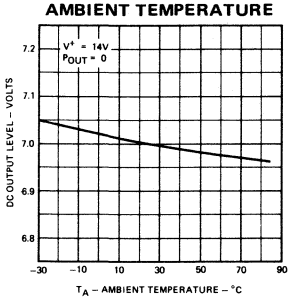
POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



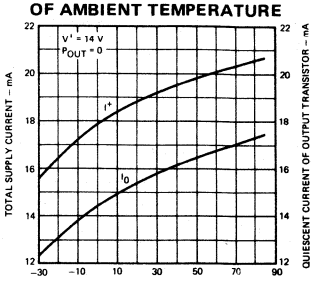
TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF SUPPLY VOLTAGE



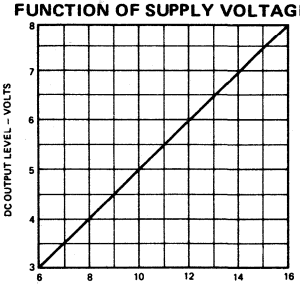
DC OUTPUT LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE



DC OUTPUT LEVEL AS A FUNCTION OF SUPPLY VOLTAGE



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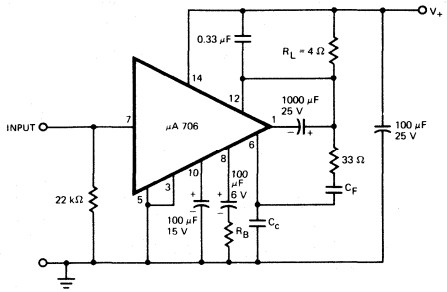
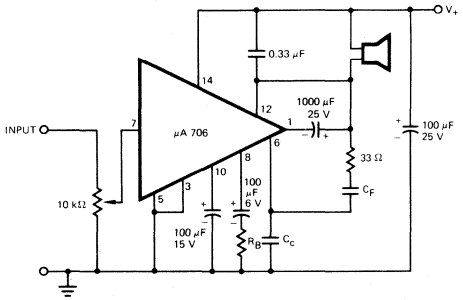
TEST CIRCUIT 1 (A_V = 46 dB, R_B = 0 Ω, C_c = 1.5 nF, C_F = 150 pF)



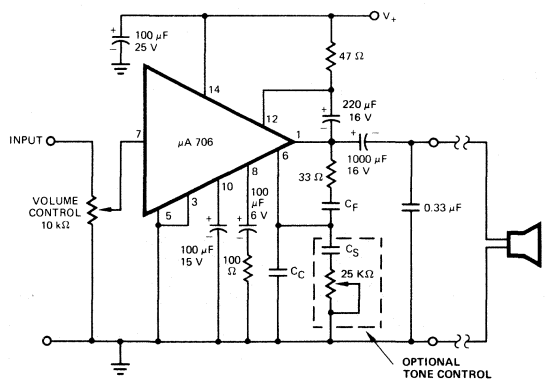
TYPICAL AUDIO APPLICATIONS

5 WATT AUDIO AMPLIFIER WITH MINIMUM COMPONENT COUNT



A_V	34 dB		46 dB	
BW	10 kHz	20 kHz	10 kHz	20 kHz
R_B	100 Ω	100 Ω	0 Ω	0 Ω
C_c	10 nF	6.8 nF	2.7 nF	1.5 nF
C_F	1 nF	470 pF	330 pF	150 pF

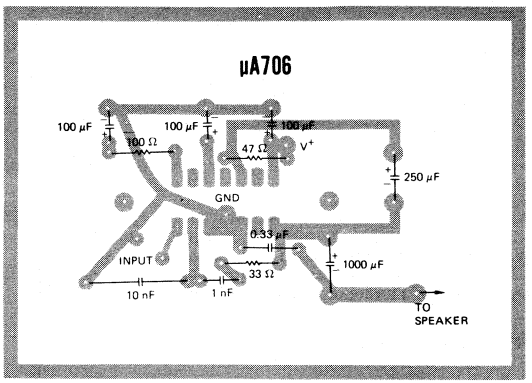
5 WATT AUDIO AMPLIFIER WITH LOAD CONNECTED TO GROUND



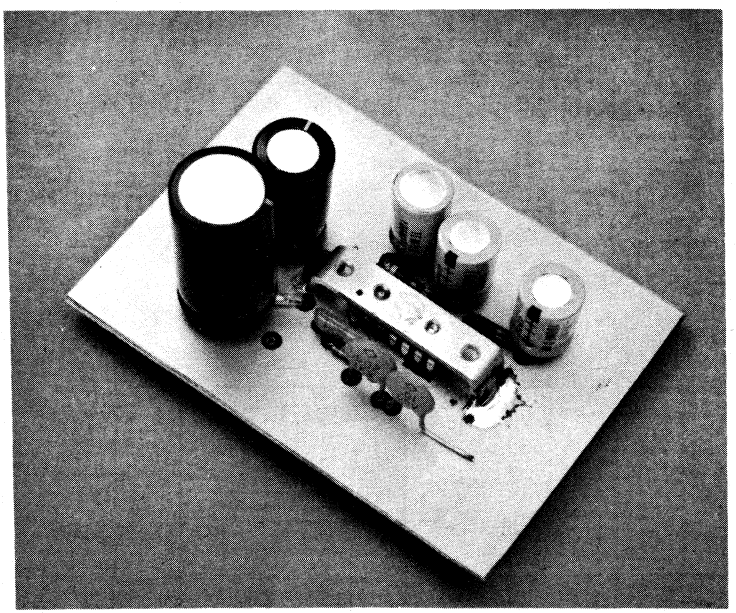
A_V	34 dB	46 dB
C_S	27 nF	5.6 nF

Note: C_S selected for 3 dB at 4 kHz.

A PC BOARD LAYOUT FOR THE 5 WATT AUDIO AMPLIFIER



PHOTOGRAPH OF THE μA706 IN A TYPICAL APPLICATION



μA720
AM RADIO SYSTEM
FAIRCHILD LINEAR INTEGRATED CIRCUIT

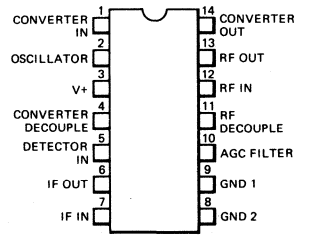
GENERAL DESCRIPTION – The μA720 is a monolithic AM Radio Receiver System made with the patented Fairchild Planar* epitaxial process. The device contains two amplifiers, a mixer-oscillator, an AGC detector and a voltage regulator. It is intended for superheterodyne AM receiver applications. Since all parts of the circuit are accessible separately, the μA720 can be used in a variety of other applications. The voltage regulator is protected against short term overvoltage transients.

- **AM-RF OSCILLATOR-CONVERTER, IF AMPLIFIER ON ONE CHIP**
- **REGULATED SUPPLY**
- **OVERVOLTAGE PROTECTION**
- **AMPLIFIERS SEPARATELY ACCESSIBLE**
- **AGC FOR RF STAGE**

ABSOLUTE MAXIMUM RATINGS

Operating Voltage	16V
Current into Supply Terminal (Pin 3)	40mA
Power Dissipation (Note 1)	670mW
Current into RF Output Terminal (Pin 13)	20mA
Current into RF Input Terminal (Pin 12)	10mA
Current into IF Input Terminal (Pin 7)	10mA
Current into or out of Detector Input Terminal (Pin 5)	±10mA
Current into AGC Filter Terminal (Pin 10)	10mA
Negative Voltage on RF Input, IF Input, and Detector Input Terminals	−5V
Negative Voltage on Converter Input Terminal	0V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperatures	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C

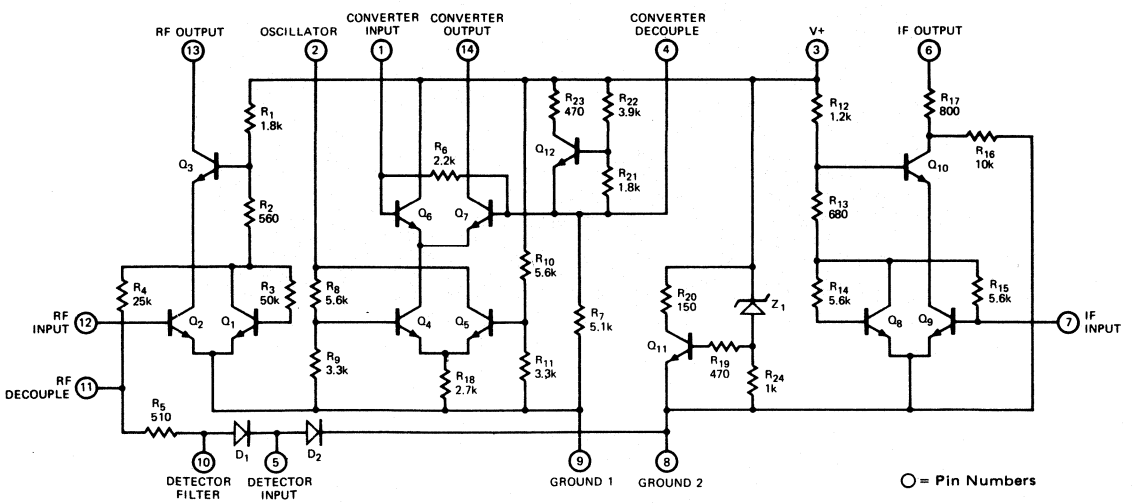
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA720C	μA720DC
μA720C	μA720PC

EQUIVALENT CIRCUIT



See notes on following page.

*Planar is a patented Fairchild process.

μA720C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_+ = 12 V, Test Circuit 1, unless otherwise indicated)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (Oscillator OFF, S_1 in Pos 2, S_3 in Pos 2, unless otherwise indicated)					
Voltage on Supply Terminal (V_3)	$I_2 + I_3$ = 15 mA	6.6	7.0	7.5	V
Voltage on Supply Terminal (V_3)	$I_2 + I_3 + I_{13} + I_{14}$ = 22 mA, S_3 in Pos 1	6.6	7.0	7.5	V
Current into Oscillator and Supply Terminal ($I_2 + I_3$)	V_3 = 5 V, S_1 in Pos 1	4.0	6.0	8.0	mA
Current into Oscillator, Supply, RF Out, and Conv. Out Terminals ($I_2 + I_3 + I_{13} + I_{14}$)	V_3 = 5 V, S_1 in Pos 1, S_3 in Pos 1	6.0	9.0	12	mA
Oscillator Current (I_2)	$I_2 + I_3$ = 15 mA		1.2		mA
RF Output Current (I_{13})	$I_2 + I_3$ = 15 mA		4.0		mA
IF Output Current (I_6)	$I_2 + I_3$ = 15 mA		4.0		mA
Voltage on Converter Input (V_1)	$I_2 + I_3$ = 15 mA		5.8		V
Voltage on IF Input (V_7)	$I_2 + I_3$ = 15 mA		0.75		V
Voltage on RF Input (V_{12})	$I_2 + I_3$ = 15 mA		0.67		V
Internal Power Dissipation	$I_2 + I_3 + I_{13} + I_{14}$ = 22 mA, S_3 in Pos 1		200		mW
AC CHARACTERISTICS (Signals are measured at the device pins)					
RF Transconductance ($gm_{RF} = i_{13}/e_{12}$)	f_{12} = 1 MHz, e_{12} = 100 μV_{RMS}, e_5 = 0 Oscillator OFF	80	120	180	mmhos
RF Input Resistance (R_{IN12})	f_{12} = 1 MHz, e_{12} = 100 μV_{RMS}, S_2 in Pos 2	500	1000		Ω
RF Input Capacitance (C_{IN12})	f_{12} = 1 MHz, e_{12} = 100 μV_{RMS}, S_2 in Pos 2		50		pF
RF Output Resistance (R_{OUT13})	f_{13} = 1 MHz		50		kΩ
RF Output Capacitance (C_{OUT13})	f_{13} = 1 MHz		10		pF
RF Noise Voltage, $\sqrt{en^2}$	Referred to Input, R_S = 50 Ω, f_{13} = 1 MHz		3.0		$nV/\sqrt{Hz}$
Detector Input Voltage (e_5)	RF Stage Gain Reduction				
	Δgm_{RF} = 3 dB, f_{13} = 1 MHz, f_5 = 260 kHz	140	180	250	mV_{RMS}
	Δgm_{RF} = 40 dB, f_{13} = 1 MHz, f_5 = 260 kHz	220	270	330	mV_{RMS}
IF Tranconductance ($gm_{IF} = i_e/e_7$)	f_7 = 260 kHz, e_7 = 1 mV_{RMS}	50	90	130	mmhos
IF Input Resistance (R_{IN7})	f_7 = 260 kHz	600	1000		Ω
IF Input Capacitance (C_{IN7})	f_7 = 260 kHz		70		pF
IF Output Resistance (R_{OUT6})	f_6 = 260 kHz		10		kΩ
IF Output Capacitance (C_{OUT6})	f_6 = 260 kHz		8		pF
Converter Transconductance ($gm_{CON} = i_{14}/e_1$)	f_1 = 1 MHz, e_1 = 1 mV_{RMS}, $f_{14} = f_{oscillator} - f_1$	1.5	2.5	3.4	mmhos
Converter Input Resistance (R_{IN1})	f_1 = 1 MHz	1000	1400		Ω
Converter Input Capacitance (C_{IN1})	f_1 = 1 MHz		8		pF
Converter Output Resistance (R_{OUT14})	f_{14} = 260 kHz		50		kΩ
Converter Output Capacitance (C_{OUT14})	f_{14} = 260 kHz		10		pF
Oscillator Output Voltage (e_2)			1.2		V_{RMS}

Note 1. Rating applies for ambient temperatures to +70°C. Derate at 8.3 mW/°C between +70°C and +85°C.

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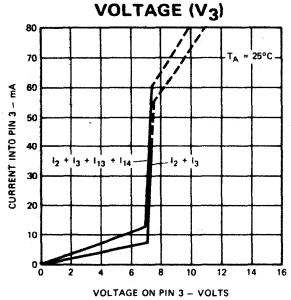
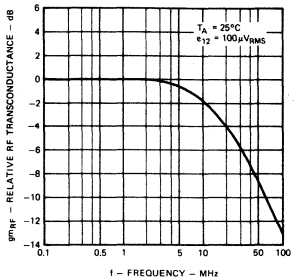
TYPICAL PERFORMANCE CURVES FOR μA720C

TEST CIRCUIT 1, unless otherwise specified.

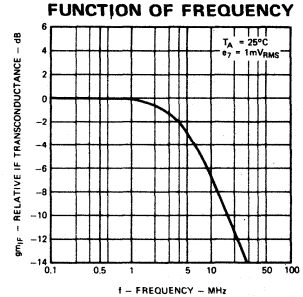
CURRENTS AS A FUNCTION OF VOLTAGE (V_3)



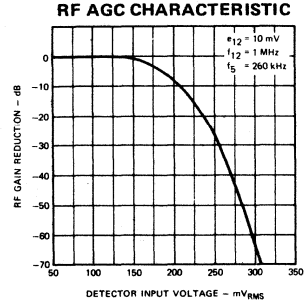
RF TRANSCONDUCTANCE AS A FUNCTION OF FREQUENCY



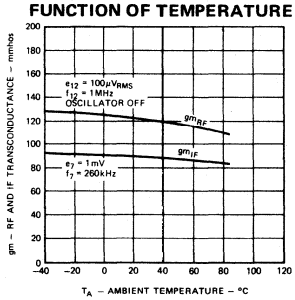
IF TRANSCONDUCTANCE AS A FUNCTION OF FREQUENCY



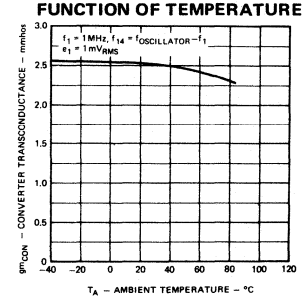
RF AGC CHARACTERISTIC



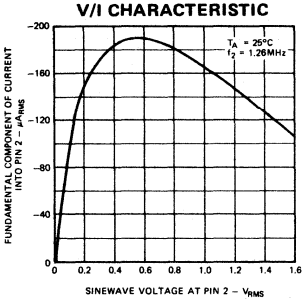
RF AND IF TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE



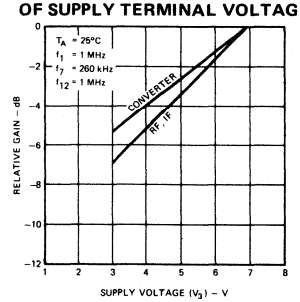
CONVERTER TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE



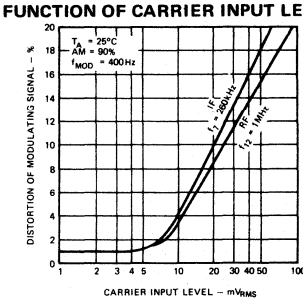
OSCILLATOR TERMINAL (PIN 2) V/I CHARACTERISTIC



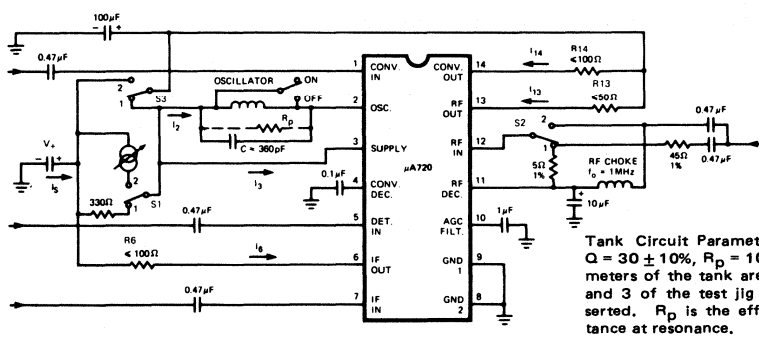
RELATIVE GAIN AS A FUNCTION OF SUPPLY TERMINAL VOLTAGE



TOTAL HARMONIC DISTORTION OF THE MODULATING SIGNAL AS A FUNCTION OF CARRIER INPUT LEVEL

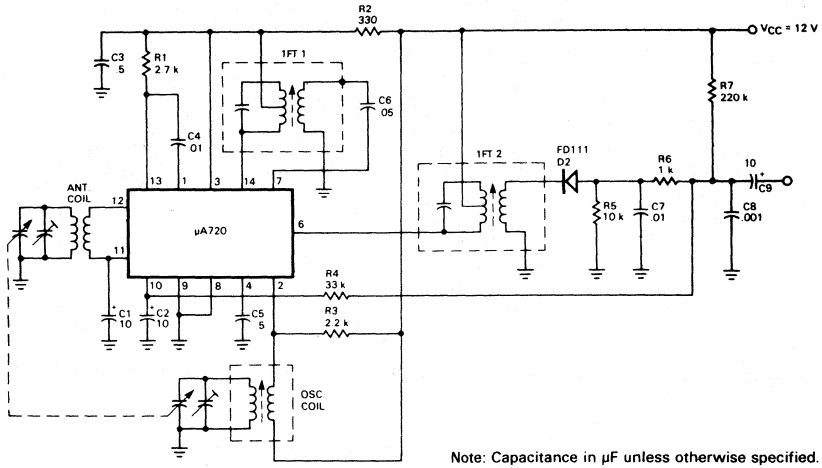


TEST CIRCUIT 1



Tank Circuit Parameters: f_o = 1.26MHz, Q = 30 ± 10%, R_p = 10kΩ ± 5%. The parameters of the tank are measured at pins 2 and 3 of the test jig without a device inserted. R_p is the effective parallel resistance at resonance.

HOME RADIO APPLICATION (Capacitor Tuned)

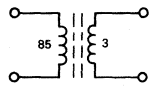


Note: Capacitance in μF unless otherwise specified.

PARTS LIST

Ferrite Antenna Bar: Q2BAR 1080/TDK Electronics
Lenght: 80mm
Diameter: 10mm

Antenna Coil:

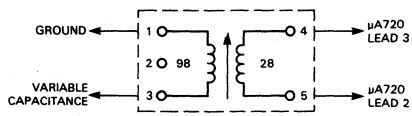


Variable Capacitance: PVC — LX20T/MITSUMI ELECTRIC
Antenna: 5–140 pF
Oscillator: 4.5–82 pF

OSCILLATOR COIL (BOTTOM VIEW)

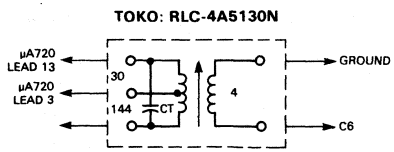
$L_{(1-3)}$ = 360 μH
Q_U = 140
f = 796 kHz

TOKO: RBO-6A5105BM



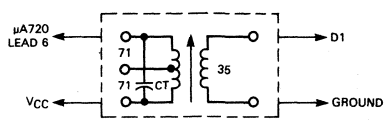
1FT 1 (BOTTOM VIEW)

TOKO: RLC-4A5130N

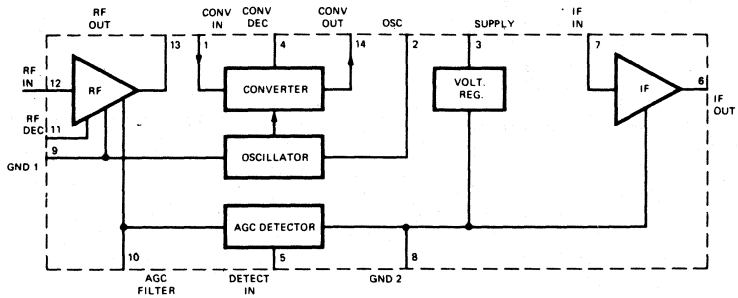


1FT 2 (BOTTOM VIEW)

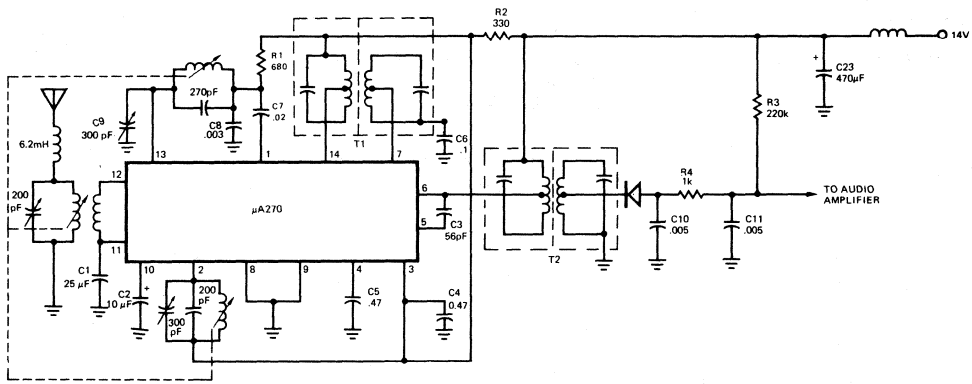
TOKO: RHC-1A5022N



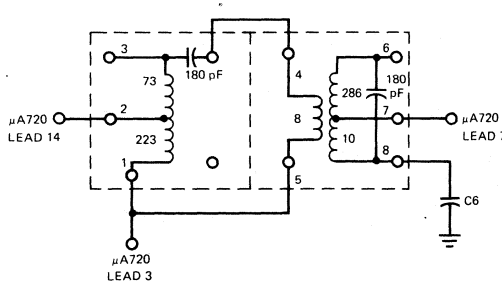
BLOCK DIAGRAM AND TYPICAL APPLICATIONS



AM CAR RADIO APPLICATION (SLUG TUNED)

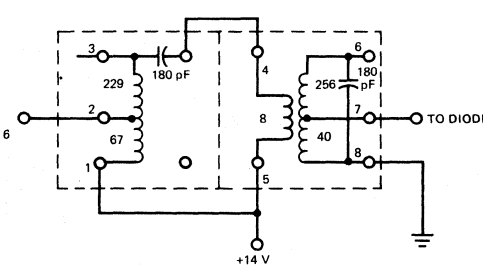


TRANSFORMER (T1)



Q_o = 60, f = 262.5 kHz
TOKO: WYOC–60021QAN
WYOC–60022SDG

TRANSFORMER (T2)



Q_o = 60, f = 262.5 kHz
TOKO: WYOC–600 23QAN
WYOC–600 24SDG

μA732
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

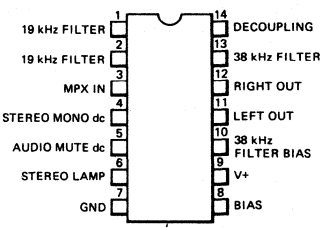
GENERAL DESCRIPTION – The μA732 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This integrated circuit demodulates a stereo multiplex signal into the right and left audio channels while inherently suppressing SCA frequency components. Internal provision is made for interstation audio muting, stereo/mono mode switching and driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement make the μA732 suitable for all line-operated and automotive FM stereo multiplex applications. See Note 1.

- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**
- **INTERNAL STEREO SWITCHING AND AUDIO MUTING FUNCTIONS**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver (Note 3)	100 mA
Internal Power Dissipation	
Molded DIP	340 mW
Hermetic DIP	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
Molded DIP	−55°C to +125°C
Hermetic DIP	−65°C to +150°C
Lead Temperature	
Molded DIP (Soldering, 10 s)	+260°C
Hermetic DIP (Soldering, 60 s)	+300°C

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACAKGE CODES D P

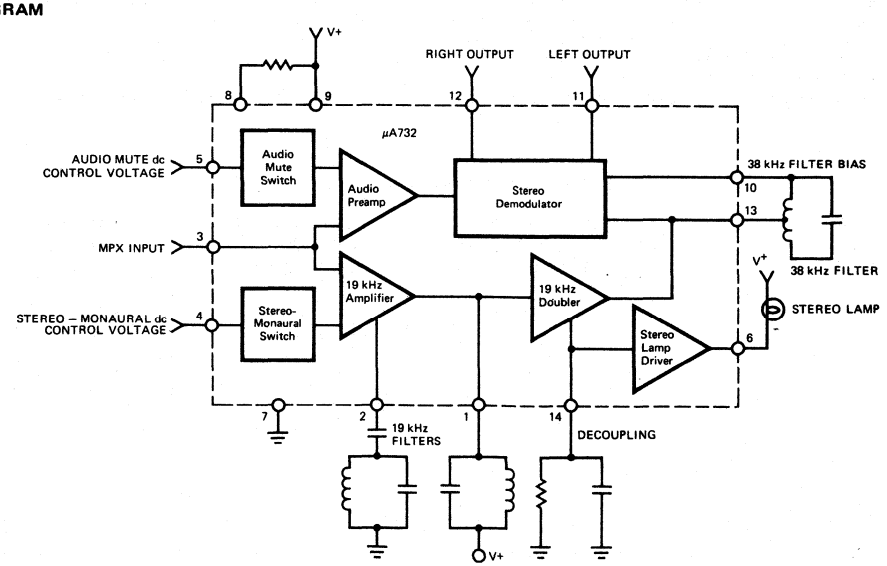


ORDER INFORMATION

TYPE	PART NO.
μA732C	μA732DC
μA732C	μA732PC

10

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

μA732C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+= +12 V, 200 mV_{RMS} standard stereo multiplex signal applied to input, unless otherwise specified (Note 3). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN	TYP	MAX	UNITS
Supply Current		11	18	mA
Input Resistance	12	20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/ V
67 kHz Storecast Rejection (Note 4)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV_{RMS}
Stereo Indicator Lamp off	4.0	8.0		mV_{RMS}
DC Voltage Required at Pin 4 for Stereo-Monaural Switching				
Stereo on	1.0	1.25	1.5	V dc
Stereo off	0.6	0.85	1.0	V dc
DC Voltage Required at Pin 5 for Audio Mute Switching				
Audio on	1.0	1.20	1.5	V dc
Audio off	0.6	0.85	1.0	V dc
Mute Attenuation of Audio	45	55		dB
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) Power supply transients up to 22 V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15 V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

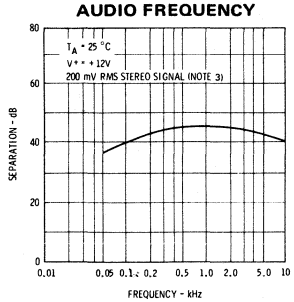
(2) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(3) "Standard Stereo Multiplex Signal" here refers to a 200 mV RMS (0.56 V p-p) composite stereo signal including 10% pilot with L = 1 and R = 1 as described in the FCC Rules on FM Broadcasting.

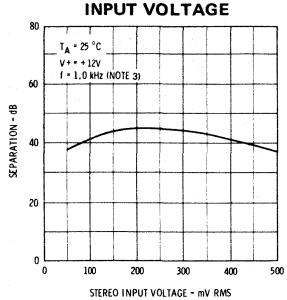
(4) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

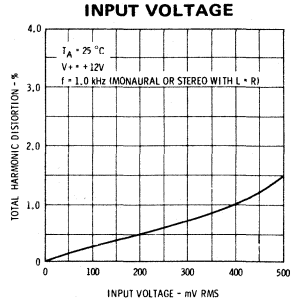
SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



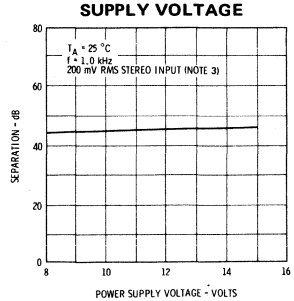
1kHz SEPARATION AS A FUNCTION OF COMPOSITE INPUT VOLTAGE



1kHz DISTORTION AS A FUNCTION OF INPUT VOLTAGE



1kHz SEPARATION AS A FUNCTION OF POWER SUPPLY VOLTAGE



FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

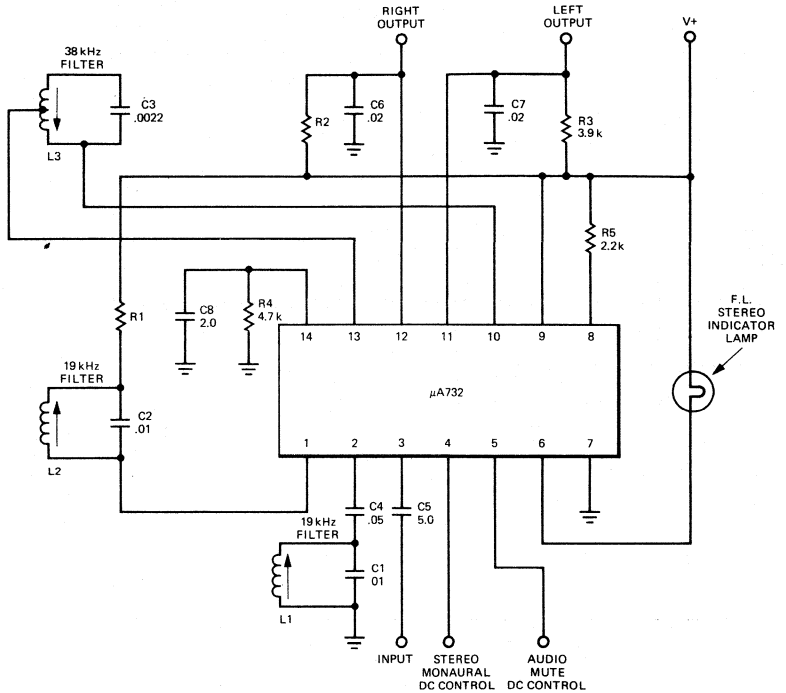


Fig. 1

NOTES:

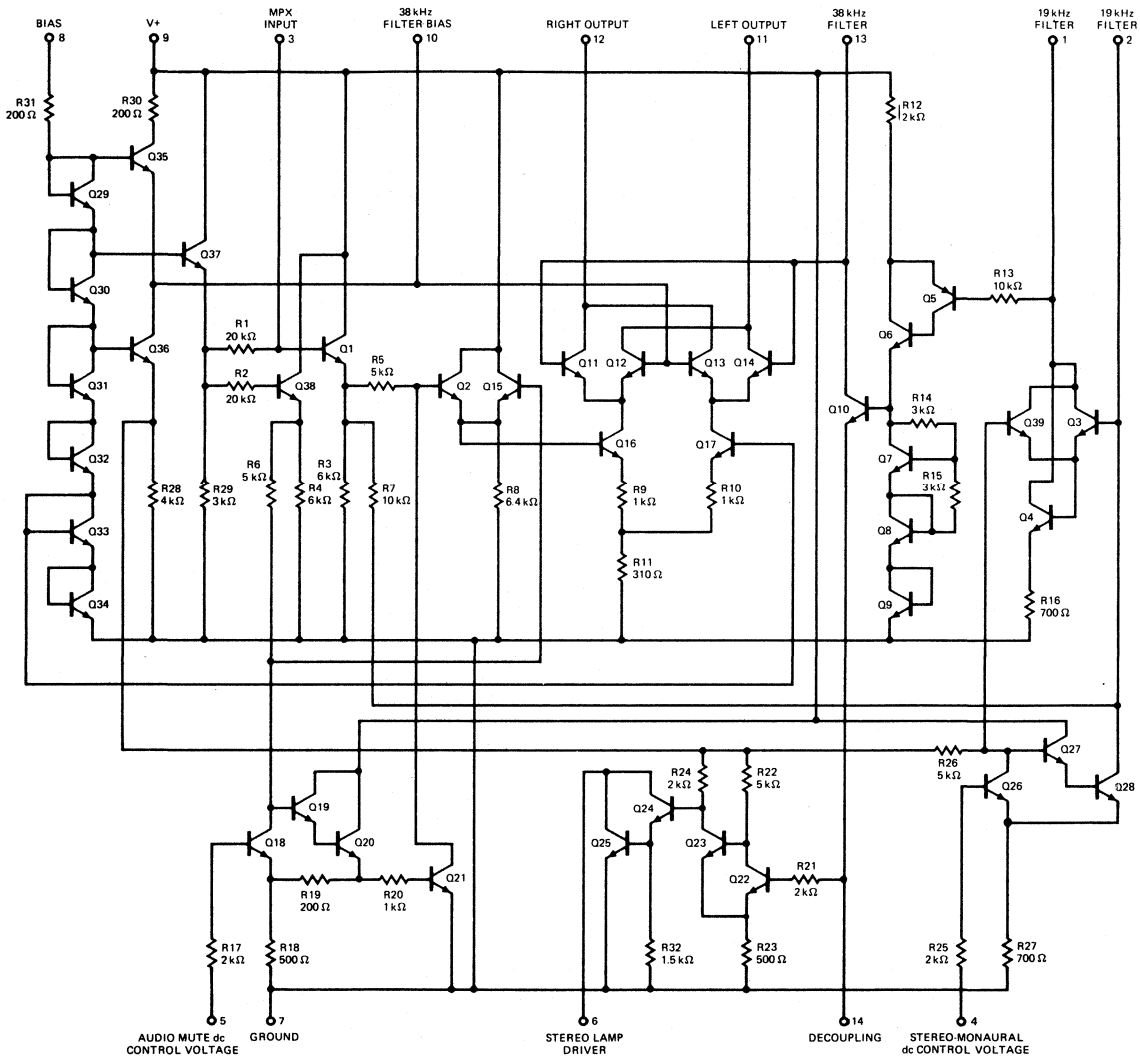
(1) Capacitors C1, C2 and C3 should be polystyrene or mylar.

(2) Coils L1 and L2 are 7.0 mH nominal with Q = 60 (Miller #1361 or equivalent).

(3) Coil L3 is 8.0 mH nominal with Q = 80, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).

(4) Resistor R1 can be increased (or decreased) in value to increase (or decrease) the 19 kHz sensitivity.

FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA739

DUAL LOW NOISE AUDIO PREAMPLIFIER/OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

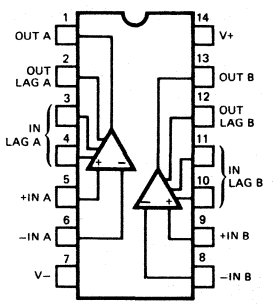
GENERAL DESCRIPTION – The μA739 consists of two identical monolithic Operational Amplifiers using the Fairchild Planar* epitaxial process. These low noise, high gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltages and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	670 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA739C	μA739DC
μA739C	μA739PC

10

FOR FULL DATA SHEET SEE OPERATIONAL AMPLIFIER SECTION

μA746

CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

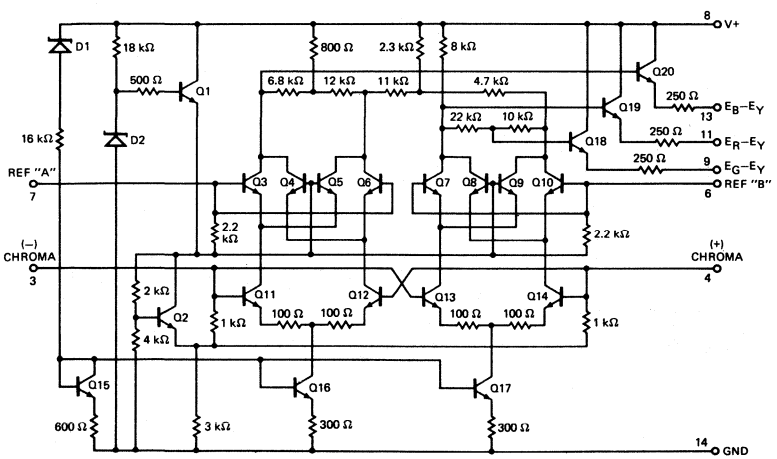
GENERAL DESCRIPTION — The μA746 is a monolithic Chroma Demodulator constructed using the Fairchild Planar* epitaxial process. This device demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs. The low voltage drift of the dc output insures excellent performance in direct-coupled chrominance output circuitry.

- **LOW OUTPUT VOLTAGE DRIFT WITH TEMPERATURE**
- **DOUBLY BALANCED DEMODULATION**
- **INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV**
- **10 VOLT PEAK-TO-PEAK E_B-E_Y OUTPUT**

ABSOLUTE MAXIMUM RATINGS

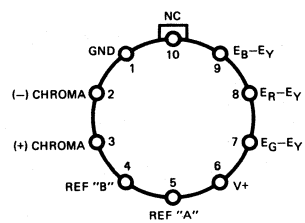
Supply Voltage	+28V
Minimum Load Resistance	3kΩ
Peak-to-Peak Reference Input Voltage	5.0V
Peak-to-Peak Chroma Input Voltage	5.0V
Internal Power Dissipation	
Metal Can	500mW
DIP	670mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
Molded DIP	−55°C to +125°C
Metal Can and Hermetic DIP	−65°C to +150°C
Lead Temperature	
Metal Can and Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C

EQUIVALENT CIRCUIT



Pin numbers shown for Dual In-line Package.

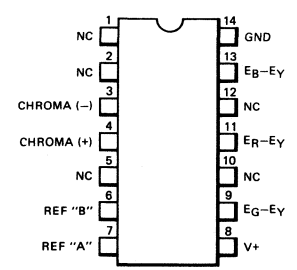
CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA746C	μA746HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA746C	μA746DC
μA746C	μA746PC

*Planar is a patented Fairchild process.

μA746C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 24V, Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	e_C = 0, R_L = 1MΩ	5.5	9.0	12.5	mA
	e_C = 0, R_L = 1MΩ, T_A = 70°C		9.0	13.0	mA
	e_C = 0	16.5	22	25.5	mA
	e_C = 0, T_A = 70°C		22		mA
Internal Power Dissipation	e_C = 0		340	430	mW
	e_C = 0, T_A = 70°C		340	445	mW
DC Voltage at any Output Terminal	e_C = 0	13.2	14.5	15.8	V
	e_C = 0, T_A = 70°C	13.0	14.5	16.0	V
Temperature Coefficient of DC Voltage at any Output Terminal	e_C = 0	−5.0	−0.3	+5.0	mV/°C
Absolute Value of DC Difference Voltage between any Two Outputs	e_C = 0		0.15	0.6	V
DC Voltage at either Reference Terminal	$e_A = e_B = e_C$ = 0		5.8		V
DC Voltage at either Chroma Terminal	e_C = 0		3.2		V
Reference Input Resistance	e_C = 0		1.7		kΩ
Reference Input Capacitance	e_C = 0		6.0		pF
Chroma Input Resistance			0.8		kΩ
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y$ = 5Vp-p		0.4	0.7	V
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y$ = 5Vp-p	3.5	3.8	4.2	V
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y$ = 5Vp-p	0.75	1.0	1.25	V
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	e_C = 1.5Vp-p	8.0	10		V
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y$ = 5Vp-p		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y$ = 5Vp-p		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y$ = 5Vp-p		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y$ = 5Vp-p	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y$ = 5Vp-p	96	104	112	Degrees
Highest AC Unbalance Voltage at any Output Terminal	e_C = 0		0.3	0.8	V_{p-p}

DEFINITIONS

Color-Difference Demodulation Angle — A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

(+) Chroma Input — A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(−) Chroma Input — A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (−) Chroma input.

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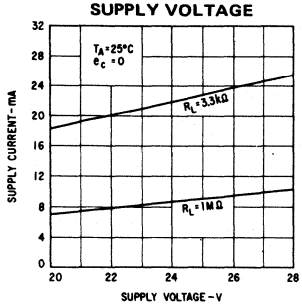
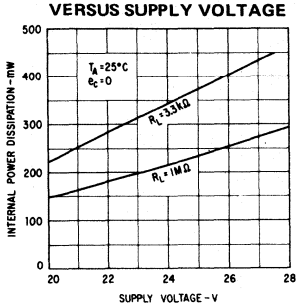
TYPICAL PERFORMANCE CURVES FOR μA746C

(Test Circuit 1 Unless Otherwise Specified)

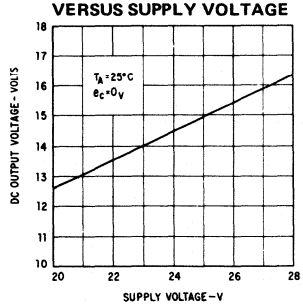
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



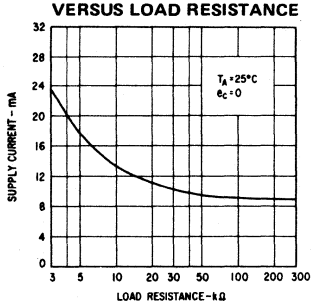
INTERNAL POWER DISSIPATION VERSUS SUPPLY VOLTAGE



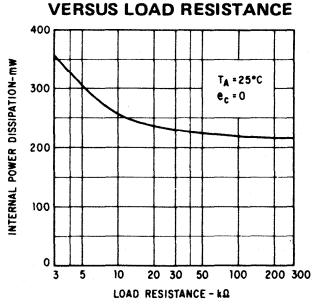
DC VOLTAGE AT ANY OUTPUT VERSUS SUPPLY VOLTAGE



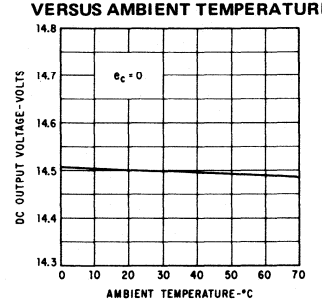
SUPPLY CURRENT VERSUS LOAD RESISTANCE



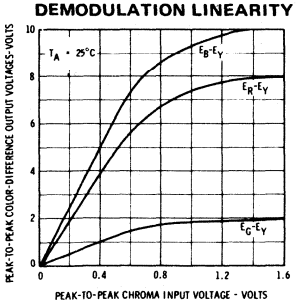
INTERNAL POWER DISSIPATION VERSUS LOAD RESISTANCE



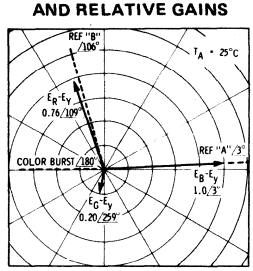
DC VOLTAGE AT ANY OUTPUT VERSUS AMBIENT TEMPERATURE



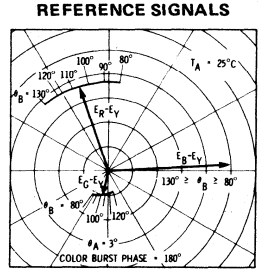
DEMODULATION LINEARITY



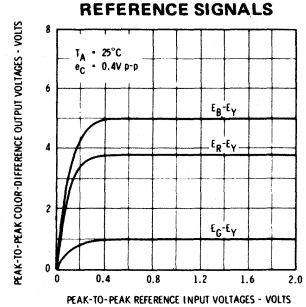
DEMODULATION ANGLES AND RELATIVE GAINS



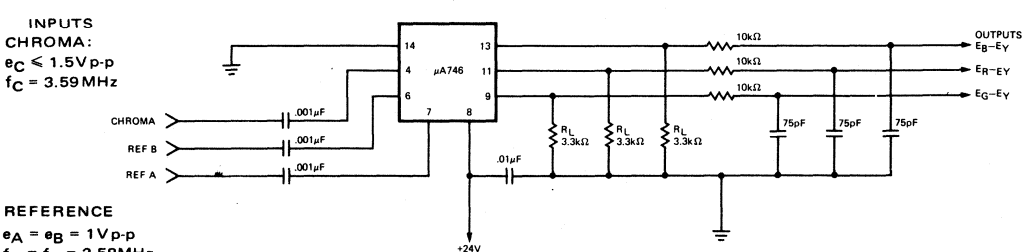
DEMODULATION SENSITIVITY TO RELATIVE PHASING OF REFERENCE SIGNALS



DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS



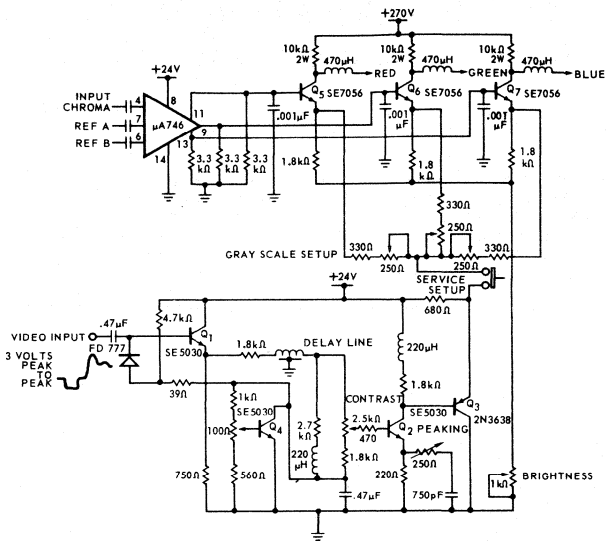
TEST CIRCUIT 1



Pin numbers shown for Dual In-line Package only.

TYPICAL APPLICATION

COMPLETE R-G-B VIDEO OUTPUT STAGE

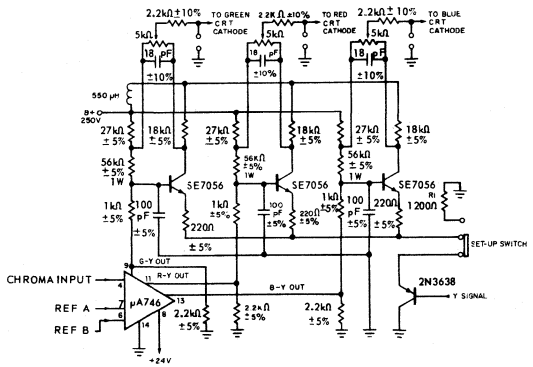


Pin numbers shown for Dual In-line Package only.

Fully dc coupled circuit exhibits negligible drift with temperature, eliminates interaction between contrast and brightness controls, and minimizes gray-scale set-up time.

10

ALTERNATIVE R-G-B VIDEO OUTPUT STAGE



Pin numbers shown for Dual In-line Package only.

From:

"A Semiconductor Video Output Amplifier for a Red Blue Green Large Screen Color Television Receiver", by D. Poppy. IEEE Transactions on Broadcast and Television Receivers, BTR-15, #2, pp. 167-70, July 1969.

μA749

DUAL AUDIO OPERATIONAL AMPLIFIER/AUDIO PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA749 consists of Two Identical High Gain Operational Amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These three-stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from dc to 10 MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired-OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers and peak detectors.

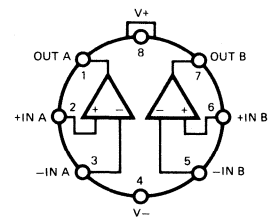
- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 25,000 V/V**
- **LARGE COMMON MODE RANGE, +11 V, −13 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (μA749 and μA749C)	±18 V
(μA749D)	±12 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	650 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2) (μA749 and μA749C)	±15 V
(μA749D)	±12 V
Storage Temperature Range	
Metal Can, Hermetic DIP	−65°C to +150°C
Molded DIP (μA749PC)	−55°C to +125°C
Operating Temperature Range	
Military (μA749)	−55°C to +125°C
Commercial (μA749C and μA749D)	0°C to +70°C
Lead Temperature	
Metal Can, Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

FOR FULL DATA SHEET
SEE OPERATIONAL AMPLIFIER SECTION

CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

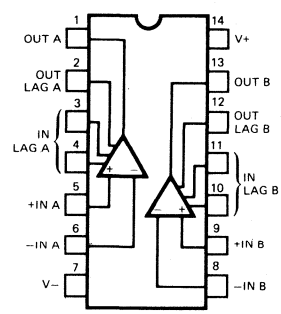


Note: Pin 4 is connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA749D	μA749DHC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA749	μA749DM
μA749C	μA749DC
μA749C	μA749PC

*Planar is a patented Fairchild process.

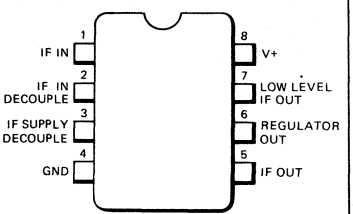
μA753
FM GAIN BLOCK
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA753 is a high performance monolithic FM Gain Block using the Fairchild Planar* epitaxial process. The FM gain block consists of a three stage direct coupled amplifier with 330Ω input and output terminations and the 7 pF shunting capacitance required for a 10.7 MHz FM IF strip utilizing commercially available ceramic filters. Included on the chip is a 7.8 V active regulator providing up to 10 mA of current to an external load such as an FM tuner.

The μA753 features full temperature compensation for the IF amplifier and the 7.8 V regulator. Excellent power supply rejection eliminates the need for an external regulated supply. An output from the second stage of the IF amplifier provides a means of external gain control without affecting the input or output terminations. The device is packaged in an 8-lead mini DIP.

- **50 dB VOLTAGE GAIN AT 10.7 MHz**
- **330Ω INPUT AND OUTPUT TERMINATIONS**
- **OPTIMIZED GAIN VS TEMPERATURE CHARACTERISTICS**
- **TEMPERATURE COMPENSATED 7.8 V ACTIVE REGULATOR PROVIDING UP TO 10 mA OF CURRENT**
- **SHORT CIRCUIT PROTECTION FOR ALL EXTERNAL CONNECTIONS**

CONNECTION DIAGRAM
8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage at any terminal must not exceed V^+

Supply Voltage (V^+)	18 V
Power Dissipation (P_D) (Note 1)	430 mW
Input Voltage (Pins 1 and 3)	±3 V
Regulator Output Current (I_{REG})	10 mA
Regulator Short Circuit Duration	Indefinite
Operating Temperature Range (T_A)	-40°C to +85°C
Storage Temperature Range (T_{STG})	-55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	260°C

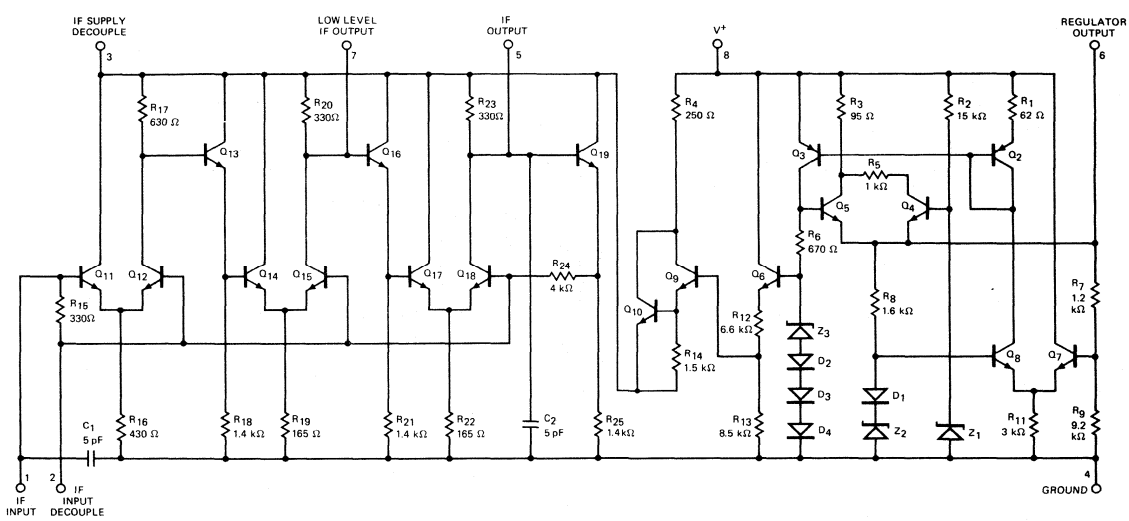
Notes: 1. Rating applies for ambient temperatures to 70°C. Above 70°C derate linearly at 6.3 mW/°C

ORDER INFORMATION

TYPE	PART NO.
μA753C	μA753TC

10

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA753C

ELECTRICAL CHARACTERISTICS: (T_A = 25°C, V_+ = +12 V unless otherwise specified)

PARAMETER	CONDITION	TEST CIRCUIT FIG. NO.	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage Operating Range		3	10		16	V
Supply Current	R_L = ∞	3	11	16	19	mA
Power Dissipation	R_L = ∞	3		190	230	mW
	I_L = 5 mA	3		210	255	mW
Terminal Voltages	I_L = 5 mA	3				
Pin 1, 2				1.4		V
3				2.6		V
5				2.0		V
6			7.2	7.8	8.3	V
7				2.0		V
AC CHARACTERISTICS IF AMPLIFIER (f_o = 10.7 MHz)						
−3 dB Limiting Threshold		1		900		μV
Output Voltage Swing	V_{IN} = 100 mV, R_L = ∞	1	1.1	1.4		V_{p-p}
Voltage Gain	V_{OUT} = 100 mV	1	40	50	56	dB
Voltage Gain Change	−40°C ≤ T_A ≤ +25°C	1		6.0		dB
	+25°C ≤ T_A ≤ 85°C	1		1.0		dB
Input Impedance:	Pin 1 to Pin 2					
Parallel Input Resistance			230	330	440	Ω
Parallel Input Capacitance				5.0	9.0	14	pF
Output Impedance:	Pin 5 to ground					
Parallel Output Resistance			230	330	440	Ω
Parallel Output Capacitance				5.0	9.0	14	pF
Output Noise Voltage		2		5.0		mV_{RMS}
AC CHARACTERISTICS REGULATOR SECTION						
Line Regulation (V_6)	I_L = 5 mA, V^+ = 10 V to 16 V	3		3.0	30	mV
Load Regulation (V_6)	I_L = 0 to 5 mA	3		−10		mV
Temperature Coefficient (V_6)	I_L = 5 mA, −40°C ≤ T_A ≤ +85°C	3		−0.15		mV/°C

TEST CIRCUIT FOR DYNAMIC CHARACTERISTICS

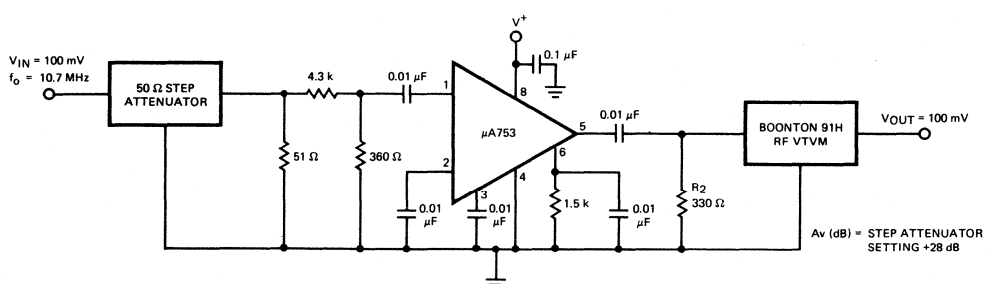


Fig. 1

NOISE MEASUREMENT TEST CIRCUIT

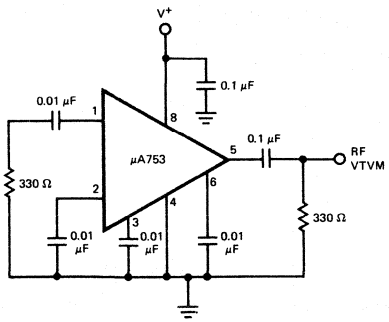


Fig. 2

TEST CIRCUIT STATIC CHARACTERISTICS

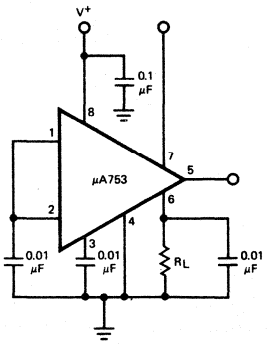
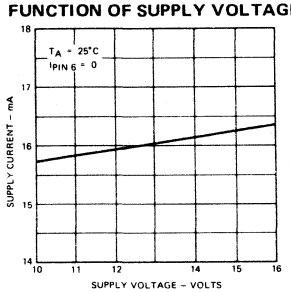


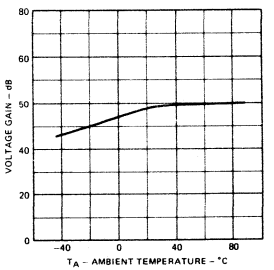
Fig. 3

TYPICAL PERFORMANCE CURVES

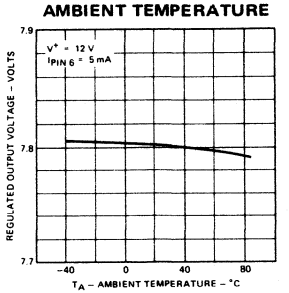
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



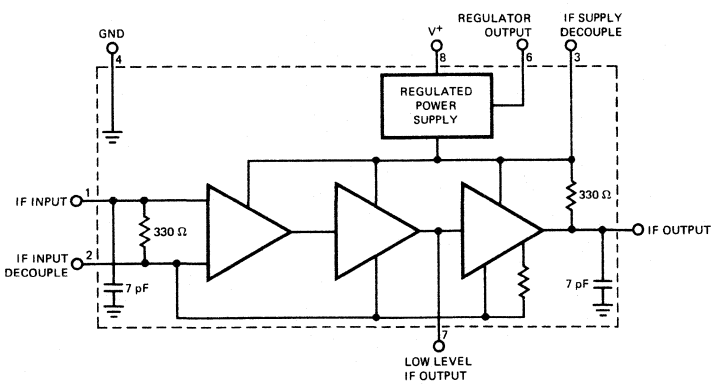
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



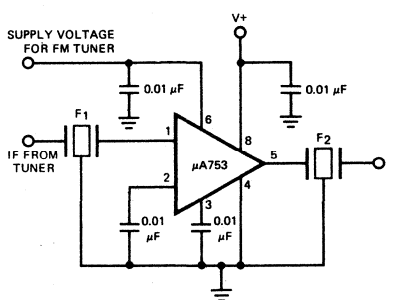
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



BLOCK DIAGRAM



TYPICAL APPLICATION



F1 AND F2: VERNITRON FM4 OR EQUIVALENT
10.7 MHz CERAMIC FILTER

10

μA758

PHASE LOCKED LOOP
FM STEREO MULTIPLEX DECODER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

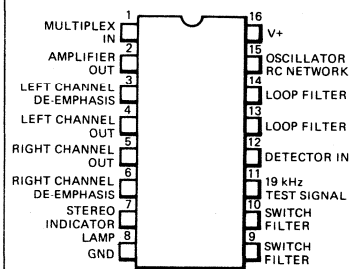
GENERAL DESCRIPTION – The μA758 is a monolithic Phase Locked Loop FM Stereo Multiplex decoder using the Fairchild Planar* epitaxial process. This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust: a potentiometer to set oscillator frequency. No external coils are required. The μA758 is suitable for all line-operated and automotive FM Stereo Receivers.

- **45 dB CHANNEL SEPARATION**
- **AUTOMATIC STEREO/MONO SWITCHING**
- **STEREO INDICATOR LAMP DRIVER WITH CURRENT LIMITING**
- **HIGH IMPEDANCE INPUT – LOW IMPEDANCE OUTPUTS**
- **70 dB SCA REJECTION**
- **ONE ADJUSTMENT FOR COMPLETE ALIGNMENT**
- **LOW NUMBER OF EXTERNAL PARTS – NO COILS**
- **10 V TO 16 V SUPPLY VOLTAGE RANGE**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)

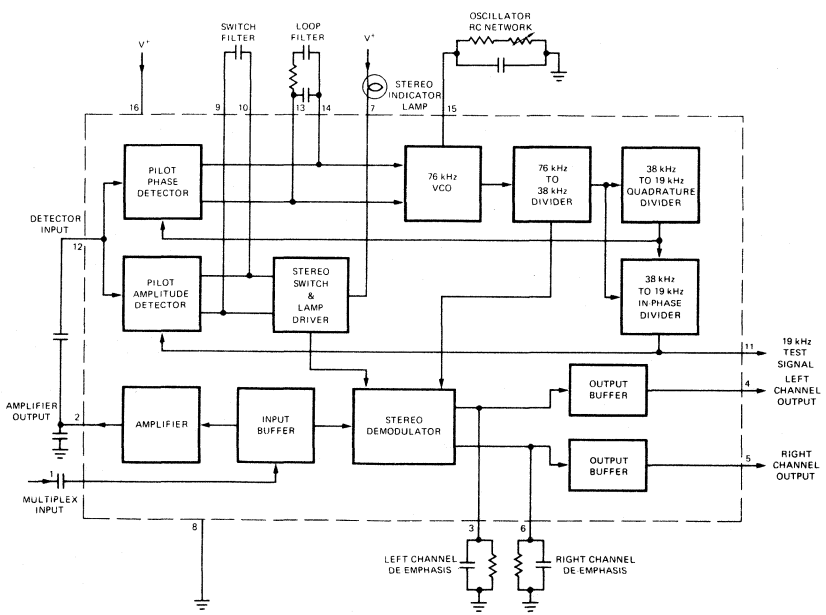
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA758C	μA758DC
μA758C	μA758PC

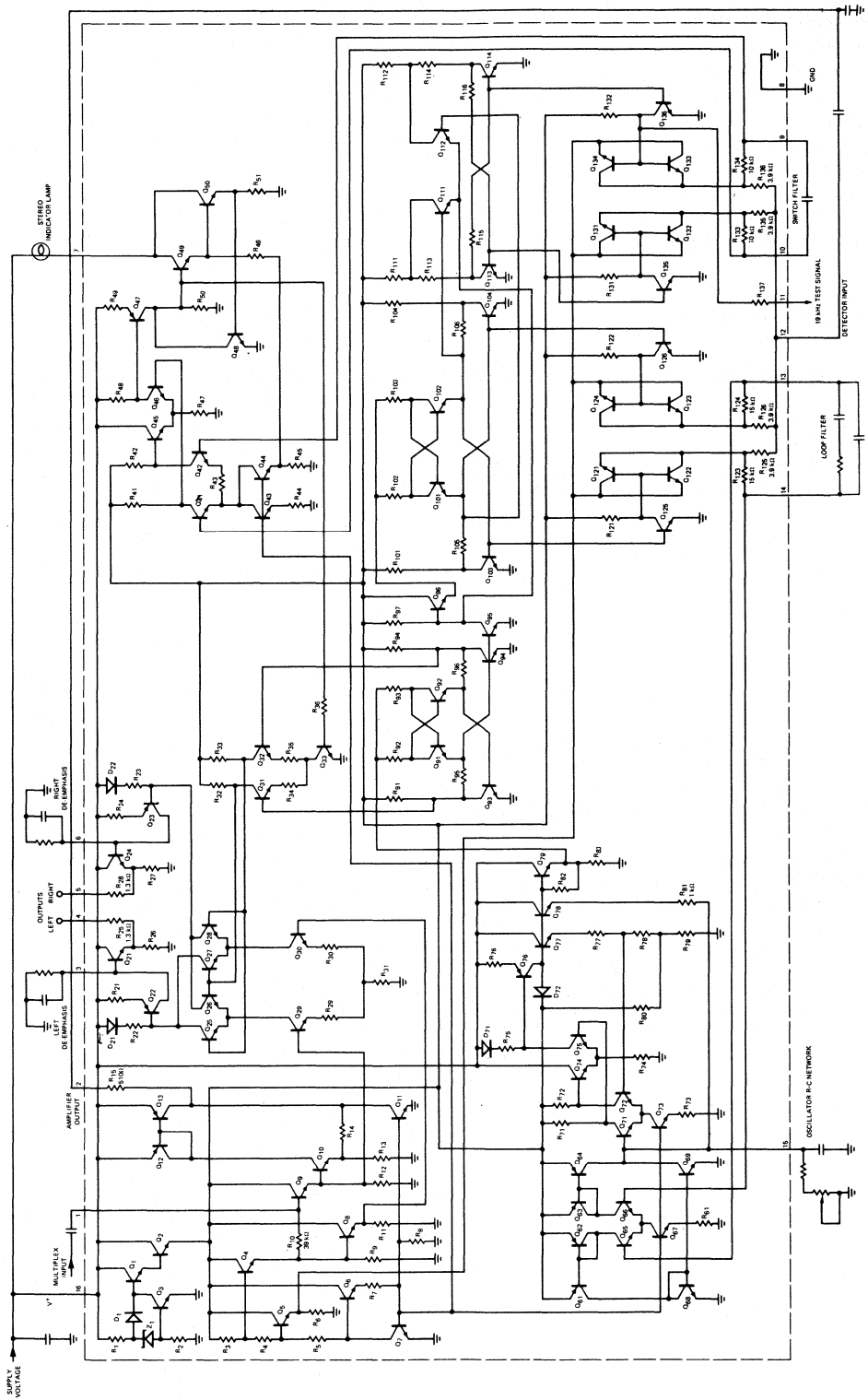
BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



All resistance values are in ohms
All capacitance values are in picofarads

10

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Supply Voltage (≤ 15 Seconds)	+22 V
Voltage at Lamp Driver Terminal (Lamp OFF)	+22 V
Internal Power Dissipation (Note 1)	730 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C

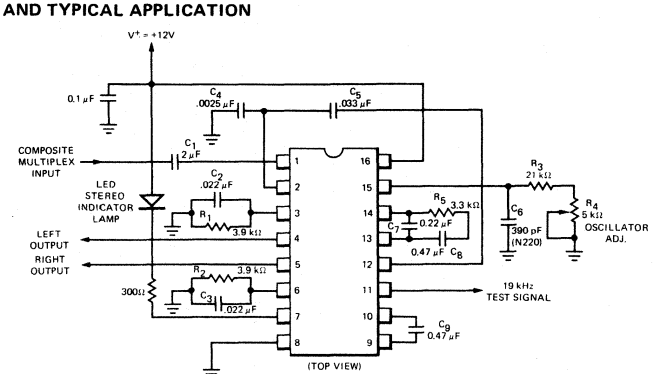
μA758C

ELECTRICAL CHARACTERISTICS [T_A = 25°C, V^+ = +12 V, 19 kHz pilot level = 30 mV_{RMS}, Multiplex Signal (L = R, pilot OFF) = 300 mV_{RMS}, Modulation Frequency = 400 Hz or 1 kHz, Test Circuit 1, unless otherwise specified]

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Supply Current	Lamp OFF		26	35	mA
Maximum Available Lamp Current		75	150		mA
Voltage at Lamp Driver Terminal	I_{LAMP} = 50 mA		1.3	1.8	V
DC Voltage Shift at Either Output Terminal	Stereo to Mono Operation		30	150	mV
Power Supply Ripple Rejection	200 Hz, 200 mV_{RMS}	35	45		dB
Input Resistance		20	35		kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation	100 Hz		40		dB
	400 Hz	30	45		dB
	10 kHz		45		dB
Channel Balance			0.3	1.5	dB
Voltage Gain	1 KHz	0.5	0.9	1.4	V/V
Pilot Input Level	Lamp Turn-On		15	20	mV_{RMS}
	Lamp Turn-Off	2.0	7.0		mV_{RMS}
Pilot Input Level Hysteresis	Lamp Turn-Off to Turn-On	3.0	7.0		dB
Capture Range		2.0	4.0	6.0	%
Total Harmonic Distortion	Multiplex Level = 600 mV_{RMS} Pilot OFF		0.4	1.0	%
19 kHz Rejection		25	35		dB
38 kHz Rejection		25	45		dB
SCA Rejection (Note 2)			70		dB
VCO Tuning Resistance (Note 3)		21.0	23.3	25.5	kΩ
VCO Frequency Drift	0°C ≤ T_A ≤ 25°C		+0.1	±2	%
	25° ≤ T_A ≤ +70°C		−0.4	±2	%

NOTES:
(1) Rating applied for ambient temperatures to 70°C. Derate at 9.1 mW/°C from 70°C to 85°C.
(2) Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
(3) Total resistance from pin 15 to ground, in test circuit 1, required to set reference frequency at pin 11 to 19 kHz ±10 Hz.

TEST CIRCUIT 1 AND TYPICAL APPLICATION

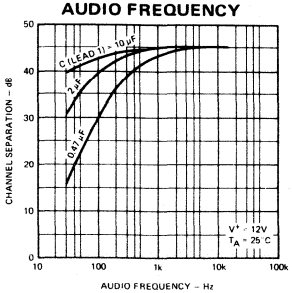


NOTE:
Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.
C_1 Tolerance = +100%, −20%
C_6 Tolerance = ±1% in test circuit and ±5% in typical application
R_3 Tolerance = ±1%
R_4 Tolerance = ±10%
R_1 and R_2 Tolerances = ±1% in test circuit and ±5% in typical application.

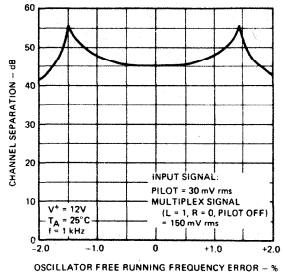
TYPICAL PERFORMANCE CURVES FOR μA758C

(Test Circuit 1 unless Otherwise Specified)

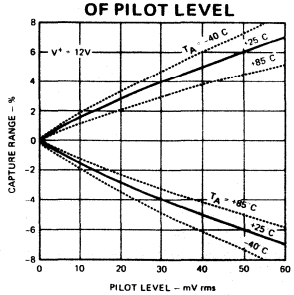
CHANNEL SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



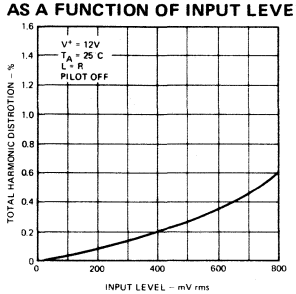
CHANNEL SEPARATION AS A FUNCTION OF OSCILLATOR FREE RUNNING FREQUENCY ERROR



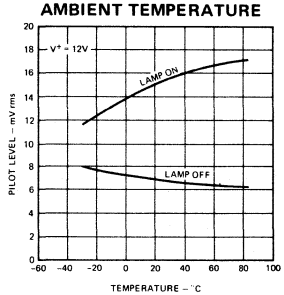
CAPTURE RANGE AS A FUNCTION OF PILOT LEVEL



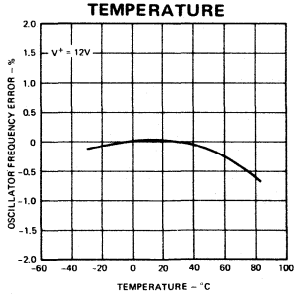
TOTAL HARMONIC DISTORTION AS A FUNCTION OF INPUT LEVEL



LAMP TURN ON AND TURN OFF SENSITIVITY AS A FUNCTION OF AMBIENT TEMPERATURE



OSCILLATOR FREE RUNNING FREQUENCY ERROR AS A FUNCTION OF AMBIENT TEMPERATURE



10

μA767

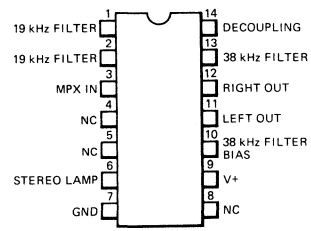
FM STEREO MULTIPLEX DECODER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA767 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This integrated circuit demodulates a stereo multiplex signal into the right and left audio channels while inherently suppressing SCA frequency components. Internal provision is made for driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement make the μA767 suitable for all line-operated and automotive FM stereo multiplex applications. For stereo decoding including interstation audio muting and stereo/mode switching, see the μA732 data sheet.

- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



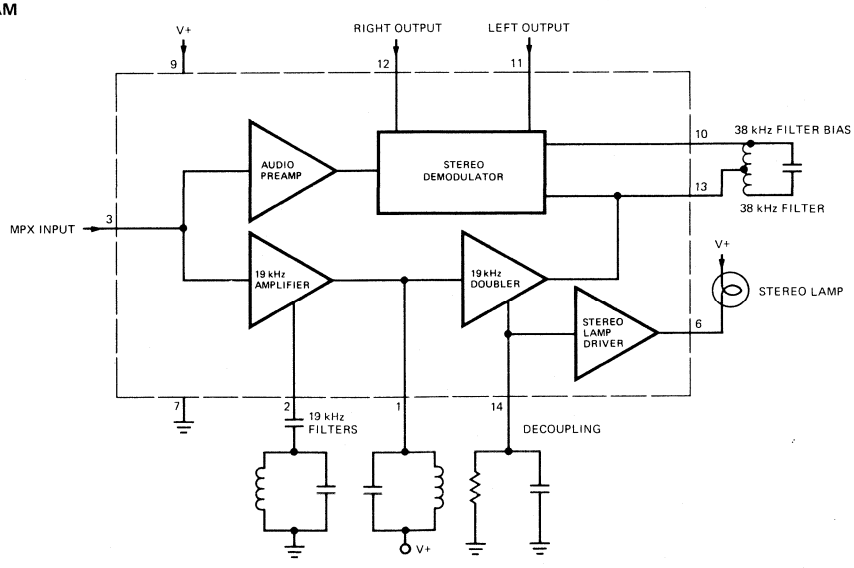
ORDER INFORMATION

TYPE	PART NO.
μA767C	μA767PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver Terminal (Note 2)	100 mA
Internal Power Dissipation	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 s)	+300°C
Molded DIP (Soldering, 10 s)	+260°C

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = + 12 V, 200 mV $_{RMS}$ standard stereo multiplex signal applied to input, unless otherwise specified (Note 3). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN	TYP	MAX	UNITS
Supply Current		12	18	mA
Input Resistance	12	20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 4)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV $_{RMS}$
Stereo Indicator Lamp off	4.0	8.0		mV $_{RMS}$
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

(2) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

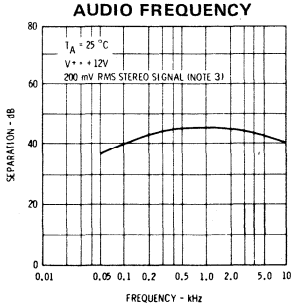
(3) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L=1 and R = 1 as described in the FCC Rules on FM Broadcasting.

(4) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

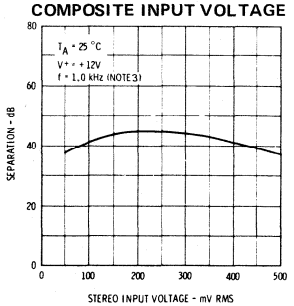
10

TYPICAL PERFORMANCE CURVES

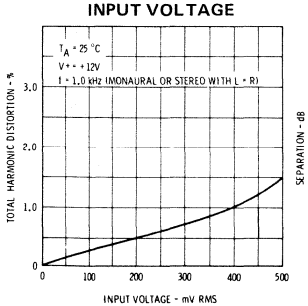
SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



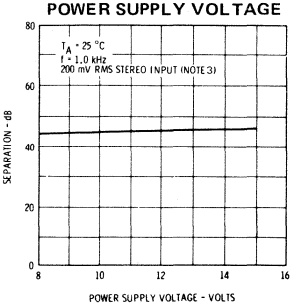
1 kHz SEPARATION AS A FUNCTION OF COMPOSITE INPUT VOLTAGE



1 kHz DISTORTION AS A FUNCTION OF INPUT VOLTAGE



1 kHz SEPARATION AS A FUNCTION OF POWER SUPPLY VOLTAGE



μA767 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

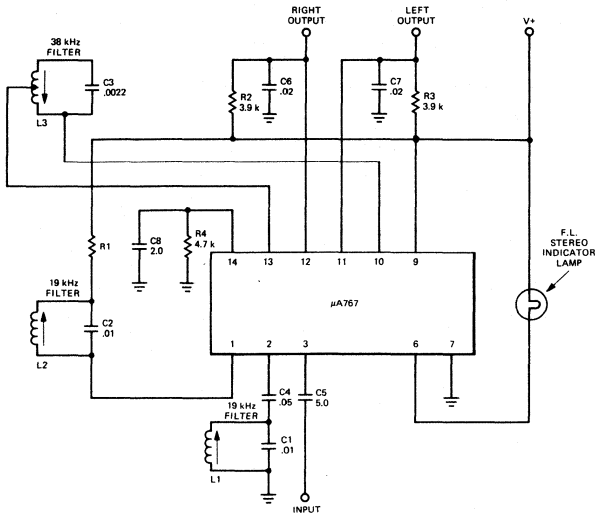
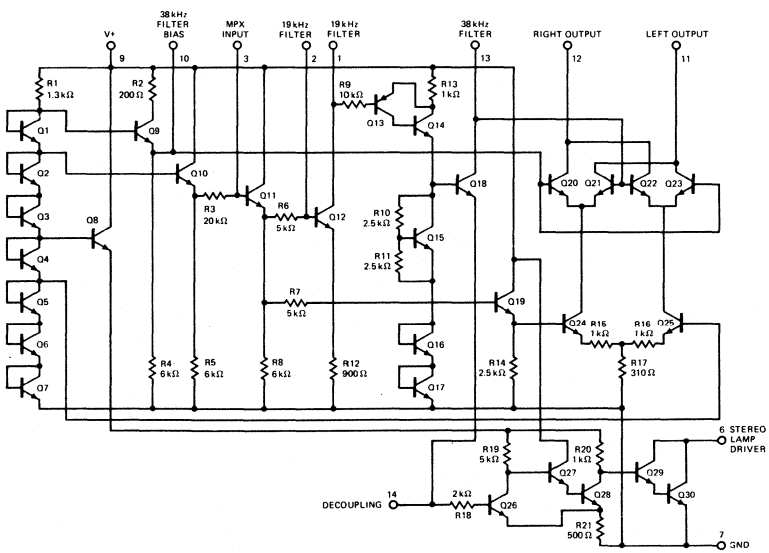


Fig. 1

NOTES:
(1) Capacitors C_1, C_2, and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with Q_{UL} = 60 (Miller #1361 or equivalent).
(3) Coil L_3 is 8.0 mH nominal with Q_{UL} = 80, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA767 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA780

CHROMA SUBCARRIER REGENERATOR (PHASE LOCKED LOOP)

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA780 is a monolithic Phase Locked Loop designed for use as a color TV subcarrier regenerator and is constructed using the Fairchild Planar* epitaxial process. This integrated circuit, which uses an automatic phase control (APC) loop, accepts the composite NTSC color video signal, extracts the color subcarrier reference and generates a CW signal suitable for use as a chroma demodulation reference. Other features include control of the CW phase (tint) by a dc voltage, blanking of the CW output during burst time and synchronous generation of an automatic color control (ACC) voltage.

The μA780 in combination with the μA781 Chroma IF Amplifier and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

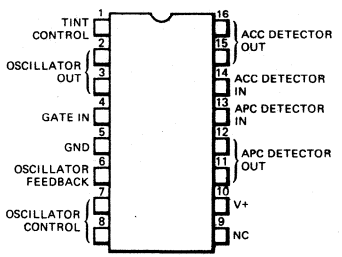
The μA780 is also useful as a communications phase locked loop system to select, amplify and demodulate AM, FM, FSK and SSB signals.

- **COMPLETE COLOR TV SUBCARRIER REGENERATOR**
- **AUTOMATIC PHASE CONTROL LOOP**
- **DC TINT CONTROL**
- **SYNCHRONOUS ACC/KILLER DETECTOR**
- **COLOR BURST GATING AND BLANKING**
- **INTERNALLY REGULATED SUPPLY**

ABSOLUTE MAXIMUM RATINGS

Supply Current	40 mA
Current into Gate Input Terminal	5 mA
Peak-to-Peak Voltage at either APC or ACC Detector Input Terminals	5 V
Internal Power Dissipation	730 mW
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Molded DIP (Soldering, 10 seconds)	260°C

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B
PACKAGE CODE P

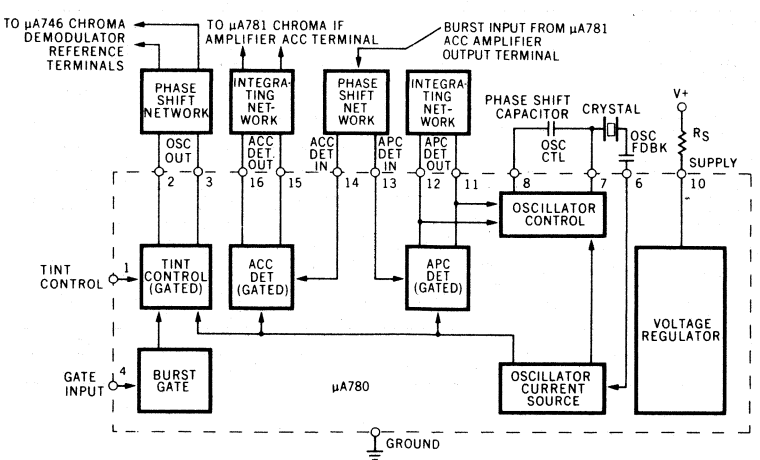


ORDER INFORMATION

TYPE	PART NO.
μA780C	μA780PC

10

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

μA780C

DC CHARACTERISTICS (T_A = 25°C, Gate "ON", Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			26		mA
Voltage at Supply Terminal		11.3	12.0	12.6	V
Supply Regulation (ΔV_{10})	V_+ = 22 V to V_+ = 27 V		40	200	mV
Total Current into Oscillator Output Terminals	Gate "OFF", 50 kΩ resistor connected between Pin 10 and Pin 6, Pin 2 shorted to Pin 3	4.2	5.8	7.6	mA
Current into Either APC Detector Output Terminal	12 kΩ resistor connected between Pin 6 and Ground		12	40	μA
Offset Voltage between ACC Detector Output Terminals ($V_{15} - V_{16}$)	50 kΩ resistor connected between Pin 10 and Pin 6	−330	−70	+330	mV
Offset Voltage between APC Detector Output Terminals ($V_{11} - V_{12}$)	50 kΩ resistor connected between Pin 10 and Pin 6	−375	−50	+375	mV
Offset Voltage between Oscillator Control Terminals ($V_7 - V_8$)	12 kΩ resistor connected between Pin 6 and Ground, $V_{11} = V_{12}$ = 9.5 V	−330	−20	+330	mV
Offset Voltage between Oscillator Output Terminals ($V_2 - V_3$)	Gate "OFF"	−200	+300	+800	mV
Voltage at Oscillator Feedback Terminal			2.8		V
Voltage at ACC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at APC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at Tint Control Terminal			200	300	mV
Voltage at Tint Control Terminal	Gate "OFF"	7.3	7.6	8.2	V
Internal Power Dissipation			310	400	mW

μA780C

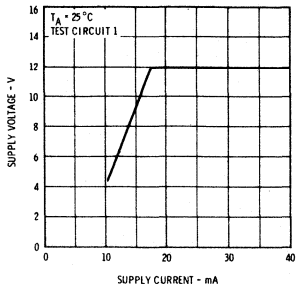
AC CHARACTERISTICS (T_A = 25°C, peak-to-peak burst level at APC Detector Input Terminal = 200 mV. Standard NTSC Signal, f_o = 3.579545 MHz, Test Circuit 2 unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Pull-in Range	$f_{free\ run} > f_o$ $f_{free\ run} < f_o$		400 −400		Hz Hz
Oscillator Static Phase Error	$f_{free\ run} = f_o$ +120 Hz $f_{free\ run} = f_o$ −120 Hz		+2.2 −2.2		Degree Degree
Oscillator Control Sensitivity			12		Hz/mV
Input Resistance at Oscillator Feedback Terminal			2.2		kΩ
Input Capacitance at Oscillator Feedback Terminal			4.5		pF
Peak-to-Peak Current at Oscillator Output Terminal (Pin 3)	Tint Control Wiper at Ground		6.8		mA
ACC Detector Input Resistance			2.2		kΩ
ACC Detector Input Capacitance			4.5		pF
ACC Detector Sensitivity	100 mV_{p-p} burst level at ACC Detector Input Terminal, Oscillator Locked		+2.2		$mVdc/mV_{p-p}$
APC Detector Input Resistance			2.2		kΩ
APC Detector Input Capacitance			4.5		pF
APC Detector Sensitivity			5.0		mV/Degree

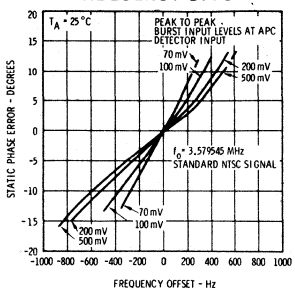
TYPICAL PERFORMANCE CURVES FOR μA780C

(Test Circuit 2 unless otherwise specified)

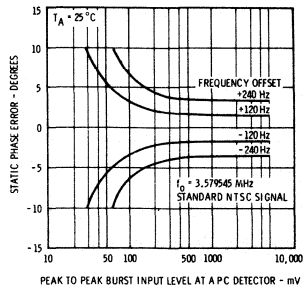
SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



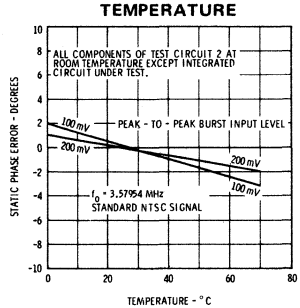
STATIC PHASE ERROR AS A FUNCTION OF FREQUENCY OFFSET



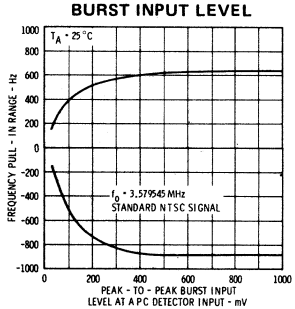
STATIC PHASE ERROR AS A FUNCTION OF BURST INPUT LEVEL



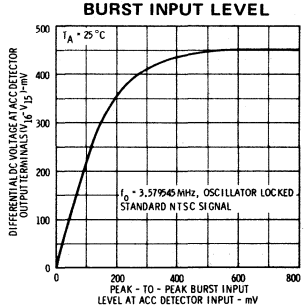
STATIC PHASE ERROR AS A FUNCTION OF TEMPERATURE



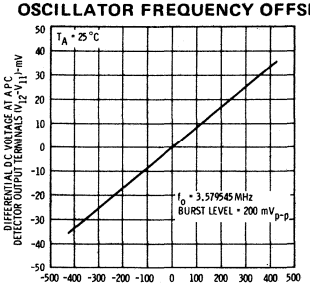
FREQUENCY PULL-IN RANGE AS A FUNCTION OF BURST INPUT LEVEL



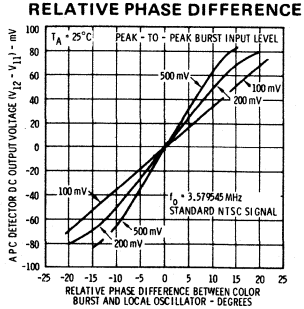
DIFFERENTIAL DC VOLTAGE AT ACC DETECTOR OUTPUT AS A FUNCTION OF BURST INPUT LEVEL



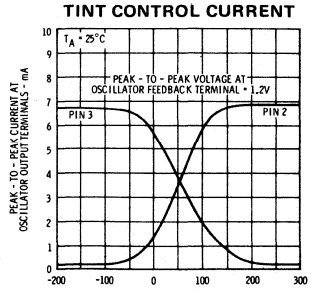
DIFFERENTIAL DC VOLTAGE AT APC DETECTOR OUTPUT TERMINALS AS A FUNCTION OF OSCILLATOR FREQUENCY OFFSET



APC DETECTOR OUTPUT AS A FUNCTION OF RELATIVE PHASE DIFFERENCE

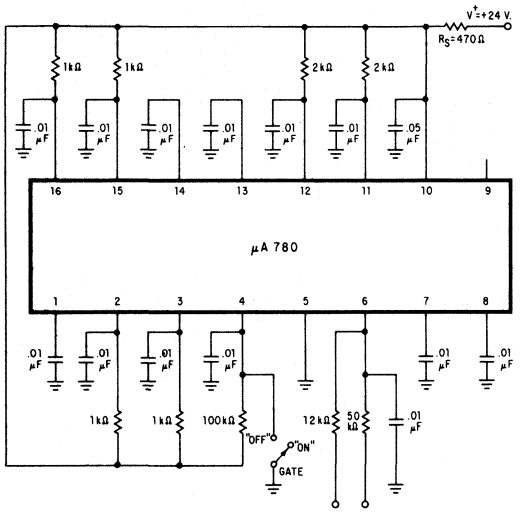


OSCILLATOR OUTPUT AS A FUNCTION OF TINT CONTROL CURRENT

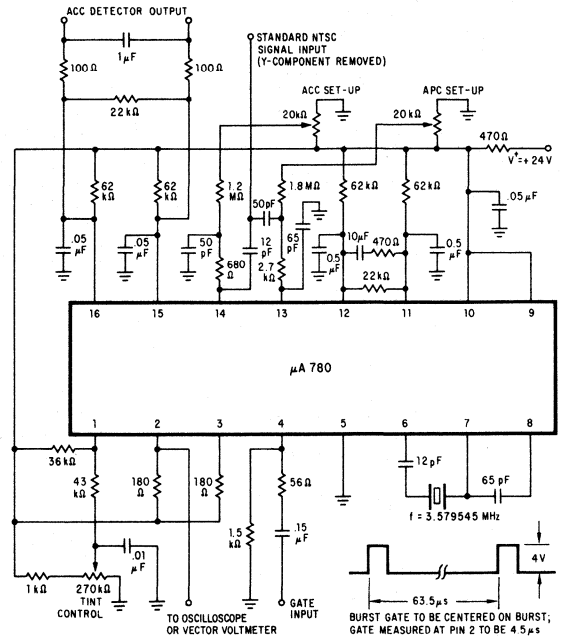


10

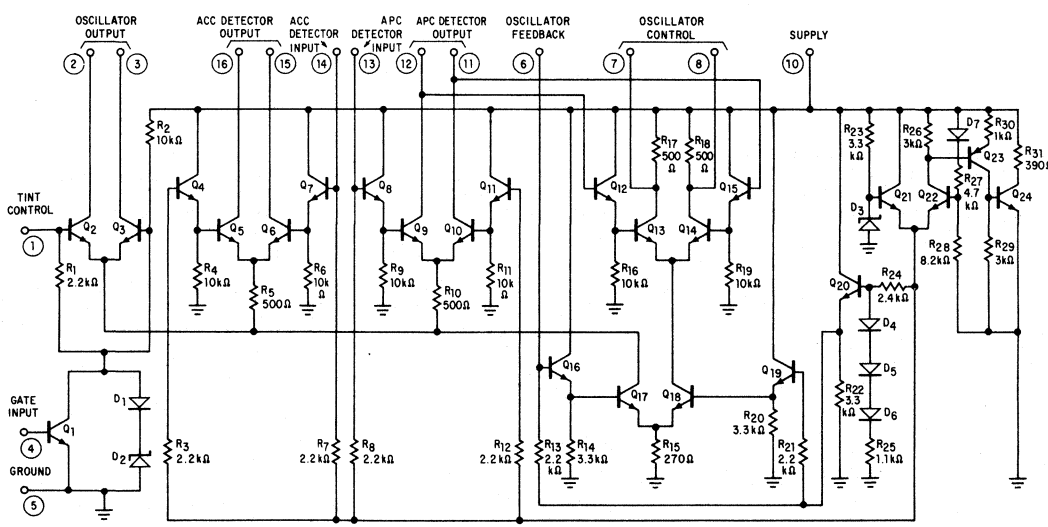
TEST CIRCUIT 1



TEST CIRCUIT 2

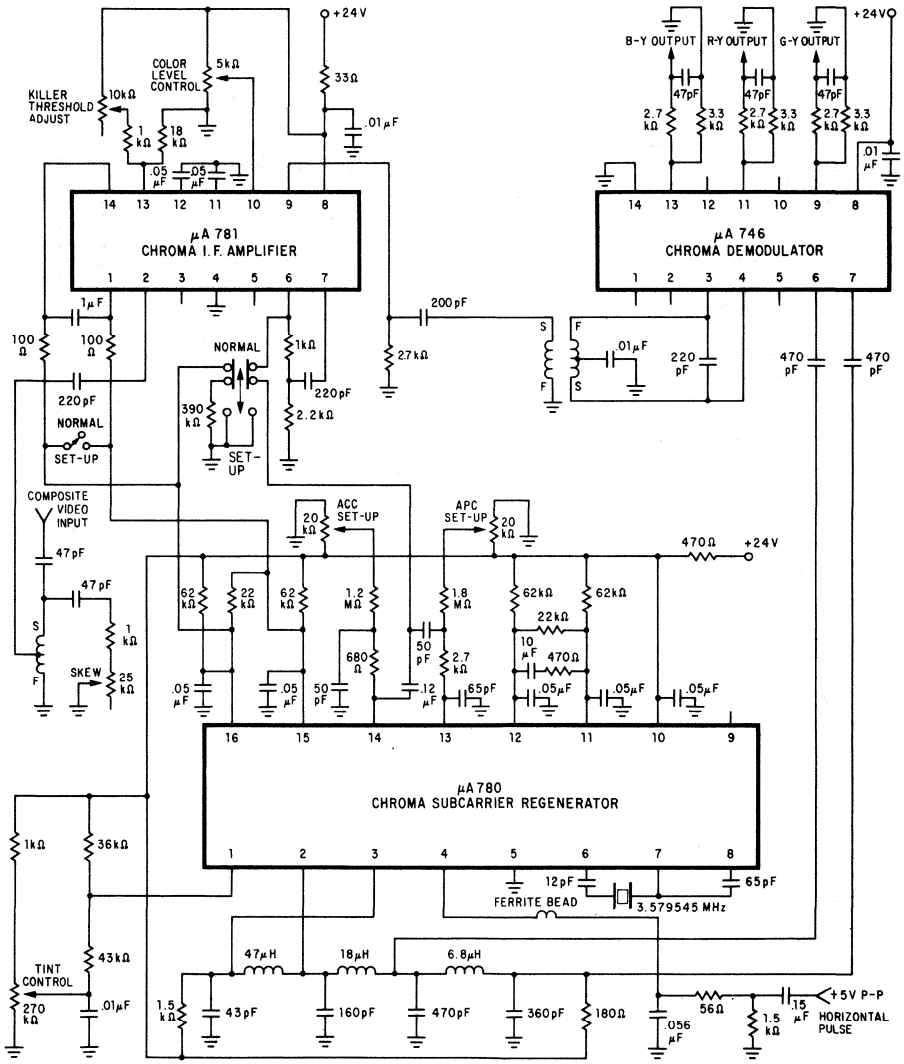


EQUIVALENT CIRCUIT

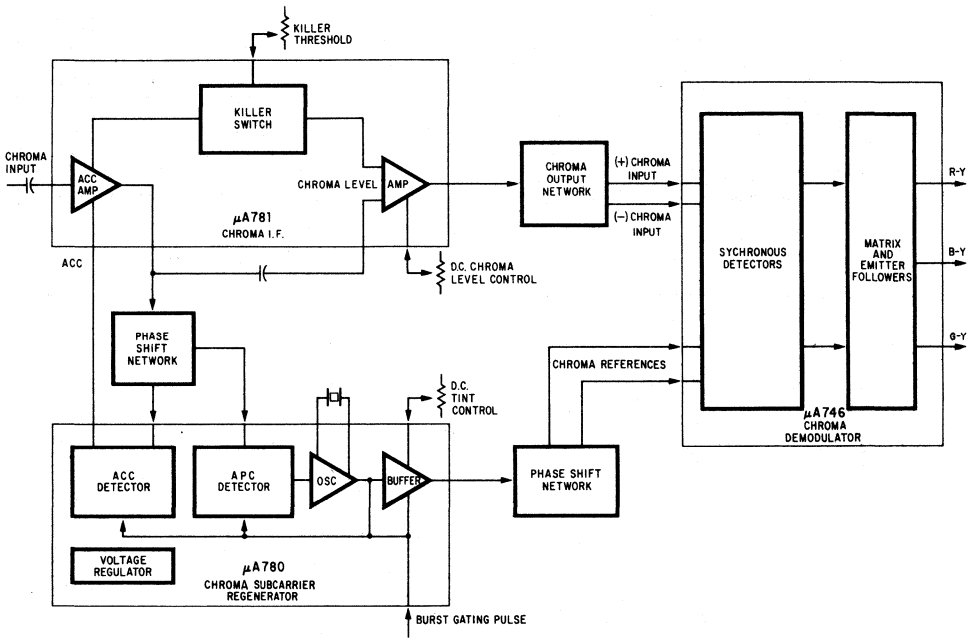


○ = Pin Numbers

INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM
(COMPLETE SCHEMATIC)



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM
(BLOCK DIAGRAM)



μA781
GAIN CONTROLLED CHROMA AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA781 is a monolithic Gain Controlled IF Amplifier for color TV constructed using the Fairchild Planar* epitaxial process. The first section is a gain controlled chroma signal amplifier whose output is used to drive a subcarrier regenerator circuit. The gain of the second section is controlled by means of an external dc voltage to set chroma level. In addition, the second stage may be gated off to provide "color killing" action in the absence of a color signal with the trip point of the gate adjusted externally.

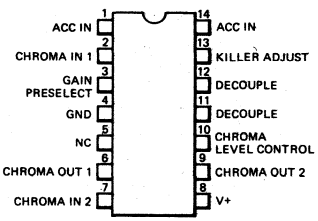
The μA781 in combination with the μA780 Phase Locked Loop Subcarrier Regenerator and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

- **COMPLETE COLOR TV CHROMA IF AMPLIFIER**
- **10 MHz BANDWIDTH**
- **AUTOMATIC COLOR CONTROL (ACC) AMPLIFIER**
- **DC CHROMA LEVEL CONTROL**
- **ADJUSTABLE COLOR KILLER**
- **OUTPUT SHORT CIRCUIT PROTECTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Internal Power Dissipation	670 mW
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C
Output Short Circuit Duration	30 seconds

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P

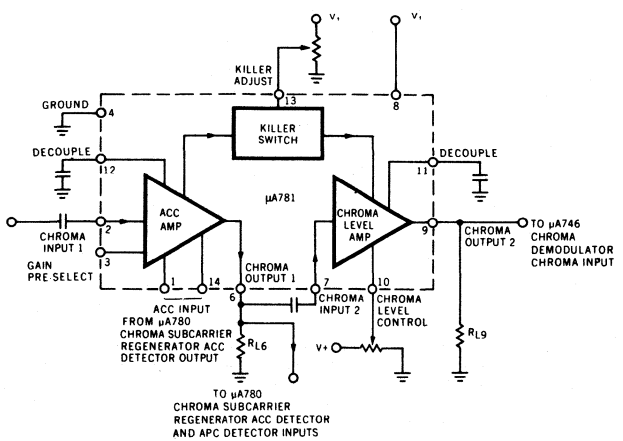


ORDER INFORMATION

TYPE	PART NO.
μA781C	μA781DC
μA781C	μA781PC

10

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

μA781C

ELECTRICAL CHARACTERISTICS (Note 1)

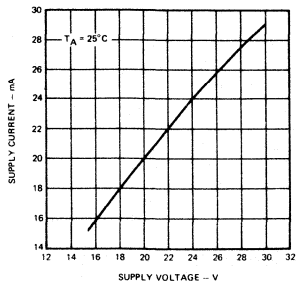
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Supply Current	$R_{L6} = R_{L9} = 1\ M\Omega$	8.0	13	18	mA
	(Note 1)	17	24	31	mA
Internal Power Dissipation			400	550	mW
Short Circuit Load Current, Chroma Output 1	$R_{L6} = 0\ \Omega$	20	42		mA
Short Circuit Load Current, Chroma Output 2	$R_{L9} = 0\ \Omega$	20	36		mA
DC Voltage at Chroma Output 1 Terminal		15.5	17.5	20	V
DC Voltage at Chroma Output 2 Terminal		17.5	18	18.5	V
Gain, ACC Amplifier Stage		14	17	19	dB
Output Voltage Sensitivity of ACC Amplifier to ACC Control Voltage	$V_{ACC} = V_1 - V_{14} = 0$ mV to $V_1 - V_{14} = -75$ mV	11	14	16	$mV_{p\text{-}p}/mVdc$
Maximum Gain, Chroma Level Amplifier Stage		12	15.8	17	dB
DC Voltage at Chroma Level Control Terminal for 90% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Set for 90% Maximum Output	3.0	5.0	5.5	V
DC Voltage at Chroma Level Control Terminal for 10% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Wiper set for 10% of Maximum Output	17	19.5	22	V
Killer "ON" Threshold (Pin 13)			16.6	17	V
Killer "OFF" Threshold (Pin 13)		16	16.3		V
DC Voltage at Decouple Terminal, Pin 11		15	15.5	16	V
DC Voltage at Decouple Terminal, Pin 12		14.5	15.3	16	V
DC Voltage at Gain Preselect Terminal		0.7	1.0	1.2	V
DC Voltage at Chroma Input 1 Terminal			1.7		V
DC Voltage at Chroma Input 2 Terminal			1.4		V
Gain Change with Temperature, Chroma Level Amplifier Stage	$T_A = 25°C$ to $T_A = 70°C$ Adjust Input Level at Chroma Input 2 for Output Level = 1.0 V RMS at Maximum Gain. Set Chroma Level Control Wiper for Output Level = 100 mV RMS		0.7		dB
Chroma Input 1 Resistance			2.4		kΩ
Chroma Input 1 Capacitance			6.2		pF
Chroma Input 2 Resistance			2.4		kΩ
Chroma Input 2 Capacitance			4.2		pF

NOTE (1)

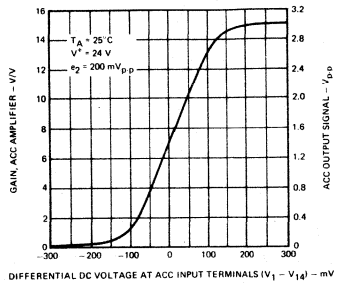
$T_A = 25°C$, $V^+ = 24$ V, $R_{L6} = 3.3\ k\Omega$, $R_{L9} = 2.7\ k\Omega$, Chroma Level Control Wiper at Ground, Voltage at ACC Input Terminals = 10 V, zero Differential Voltage between ACC Input Terminals, f = 3.58 MHz, Peak-to-Peak Input at Chroma Input 1 = 200 mV, Peak-to-Peak Input at Chroma Input 2 = 400 mV, unless otherwise specified. Refer to Test Circuit 1.

TYPICAL PERFORMANCE CURVES FOR μA781C

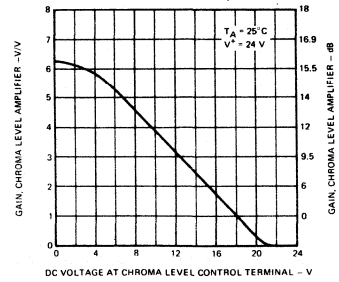
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



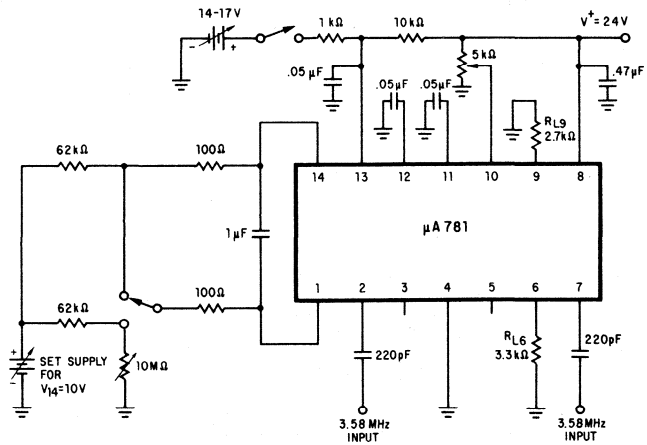
ACC AMPLIFIER GAIN AS A FUNCTION OF DIFFERENTIAL DC VOLTAGE AT ACC INPUT TERMINALS



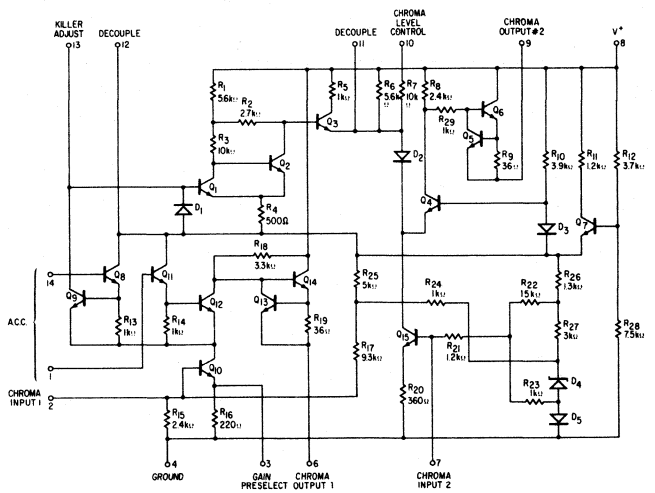
CHROMA LEVEL AMPLIFIER GAIN AS A FUNCTION OF DC VOLTAGE AT CHROMA LEVEL CONTROL TERMINAL



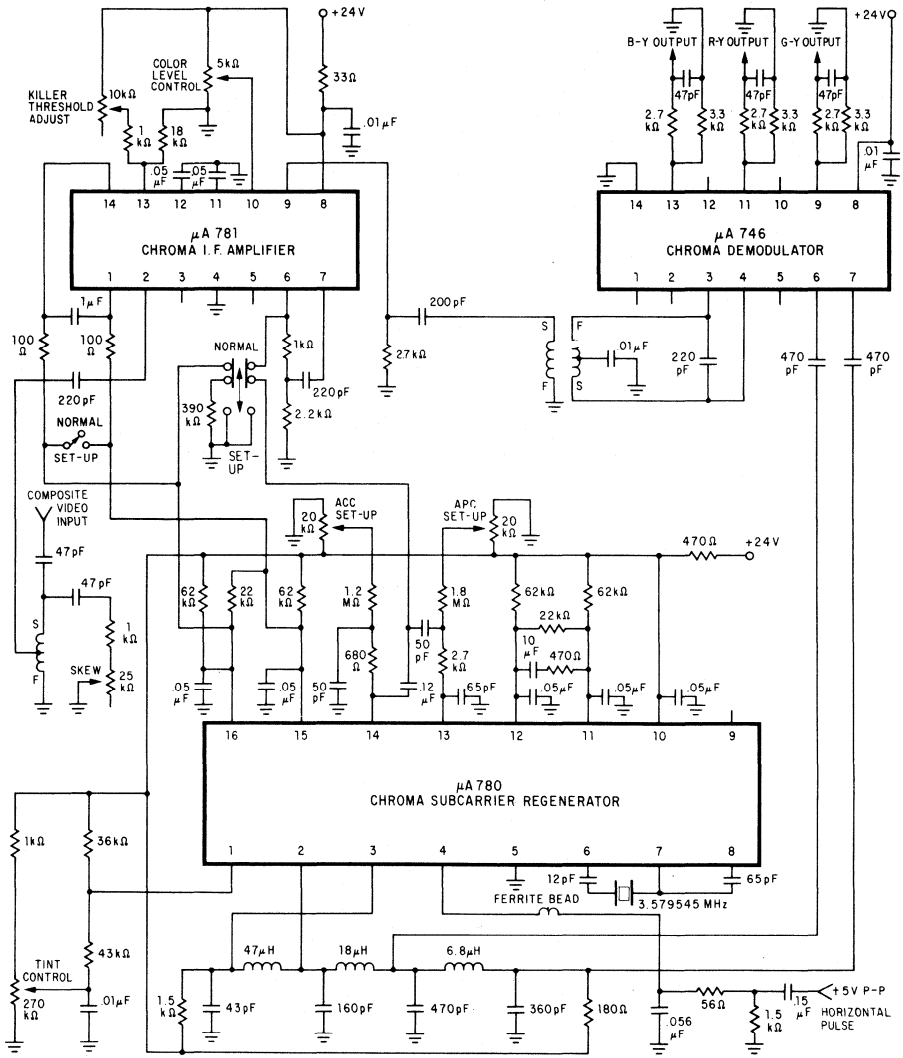
TEST CIRCUIT



EQUIVALENT CIRCUIT

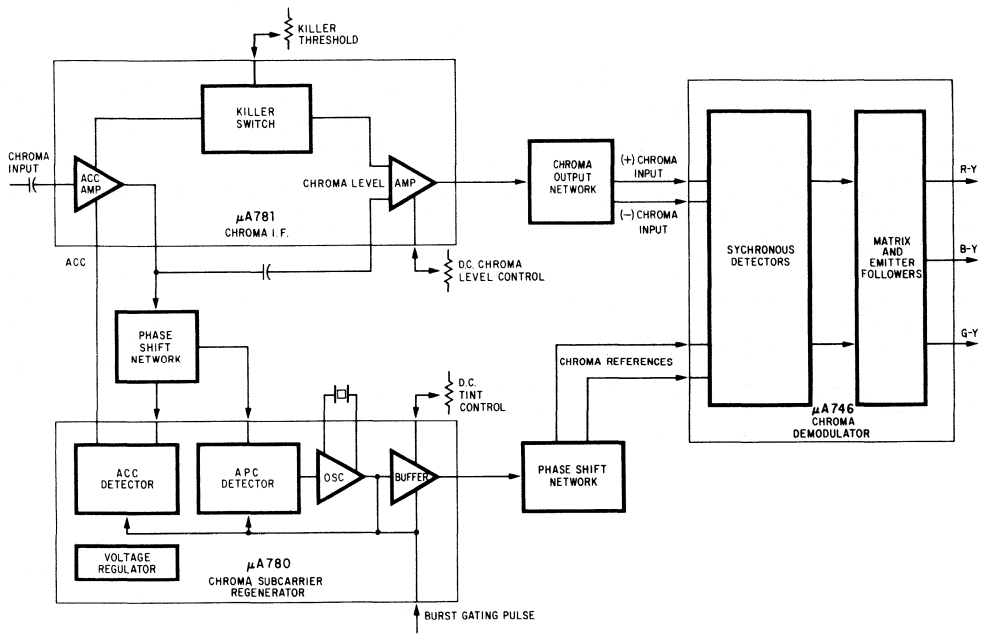


INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM

BLOCK DIAGRAM



10

μA787
CHROMA PROCESSOR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA787 is a monolithic color TV Chroma Processor circuit. It is constructed using the Fairchild Planar* epitaxial process. The device performs the entire chroma processing function in a color TV receiver. The μA787 interfaces with a variety of chroma demodulator circuits, e.g., μA746, 3067, and μA788. However, when teamed with the μA788 (chroma demodulator and dc tint control), it offers the most complete 2-chip chroma system, featuring reduced component count and minimum adjustments.

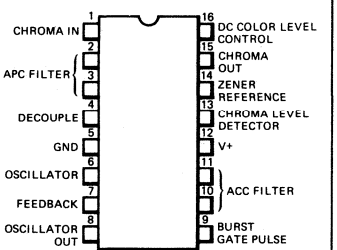
Automatic color level control, an additional feature of the μA787 controls the gain of the chroma bandpass amplifier by detection of the chroma level. ACC and ACL work in conjunction to give superior chroma performance under varying signal conditions.

- **GAIN CONTROLLED CHROMA BANDPASS AMPLIFICATION**
- **DC COLOR LEVEL CONTROL**
- **SYNCHRONOUS BURST LEVEL DETECTION (ACC)**
- **COLOR KILLER**
- **PHASE LOCKED CHROMA SUBCARRIER REGENERATION (APC)**
- **PEAK CHROMA LEVEL DETECTION (ACL)**
- **ACC AND COLOR KILLER ADJUSTMENTS NOT REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	14 V
Power Dissipation	730 mW
Current into Zener Reference Terminal	20 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 s)	260°C

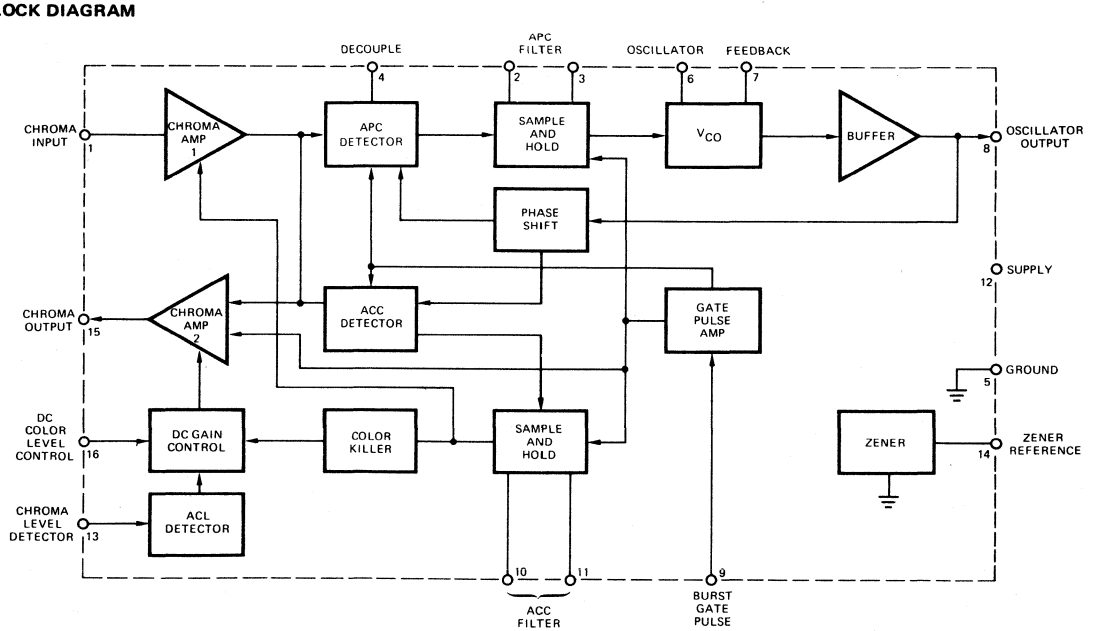
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B
PACAKGE CODE P



ORDER INFORMATION

TYPE	PART NO.
μA787	μA787PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

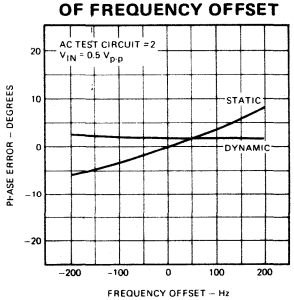
DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, S1 and S2 normally open, Test Circuit 1, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			26	36	mA
Zener Reference		11.1	11.9	12.7	V
Chroma Input			2.1		V
APC Filter			8.0		V
Decouple Bypass			7.5		V
Oscillator			8.0		V
Oscillator Feedback			2.0		V
Oscillator Output			7.6		V
Burst Gate Input	S2 Closed		1.7		V
ACC Filter			8.0		V
Chroma Level Detector			0.54		V
Chroma Output	S1, S2 Closed		6.2		V

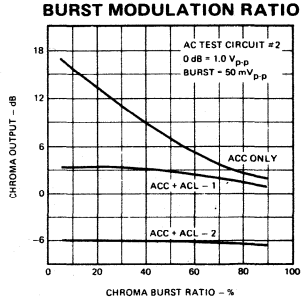
AC CHARACTERISTICS (V_{12} = 11.2 V, S3 normally open, Test Circuit 2, unless otherwise specified.)

Oscillator Output	V_{IN} = 0	0.6	1.1	1.8	V_{p-p}
Chroma Output	V_{IN} = 0.5 V_{p-p}	1.5	2.5	4.0	V_{p-p}
Oscillator Pull In Range	V_{IN} = 0.5 V_{p-p}	200	400		Hz
Chroma Output	S3 Closed		450		mV_{p-p}
Chroma Input Level for Color Killer Threshold		5.0	20	50	mV_{p-p}

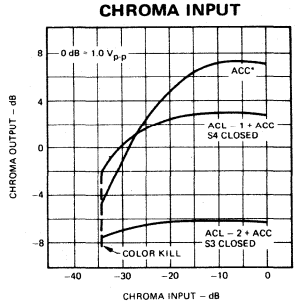
DYNAMIC AND STATIC PHASE ERROR AS A FUNCTION OF FREQUENCY OFFSET



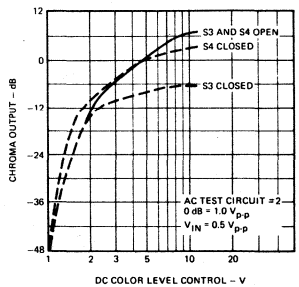
CHROMA OUTPUT AS A FUNCTION OF CHROMA BURST MODULATION RATIO



CHROMA OUTPUT AS A FUNCTION OF CHROMA INPUT

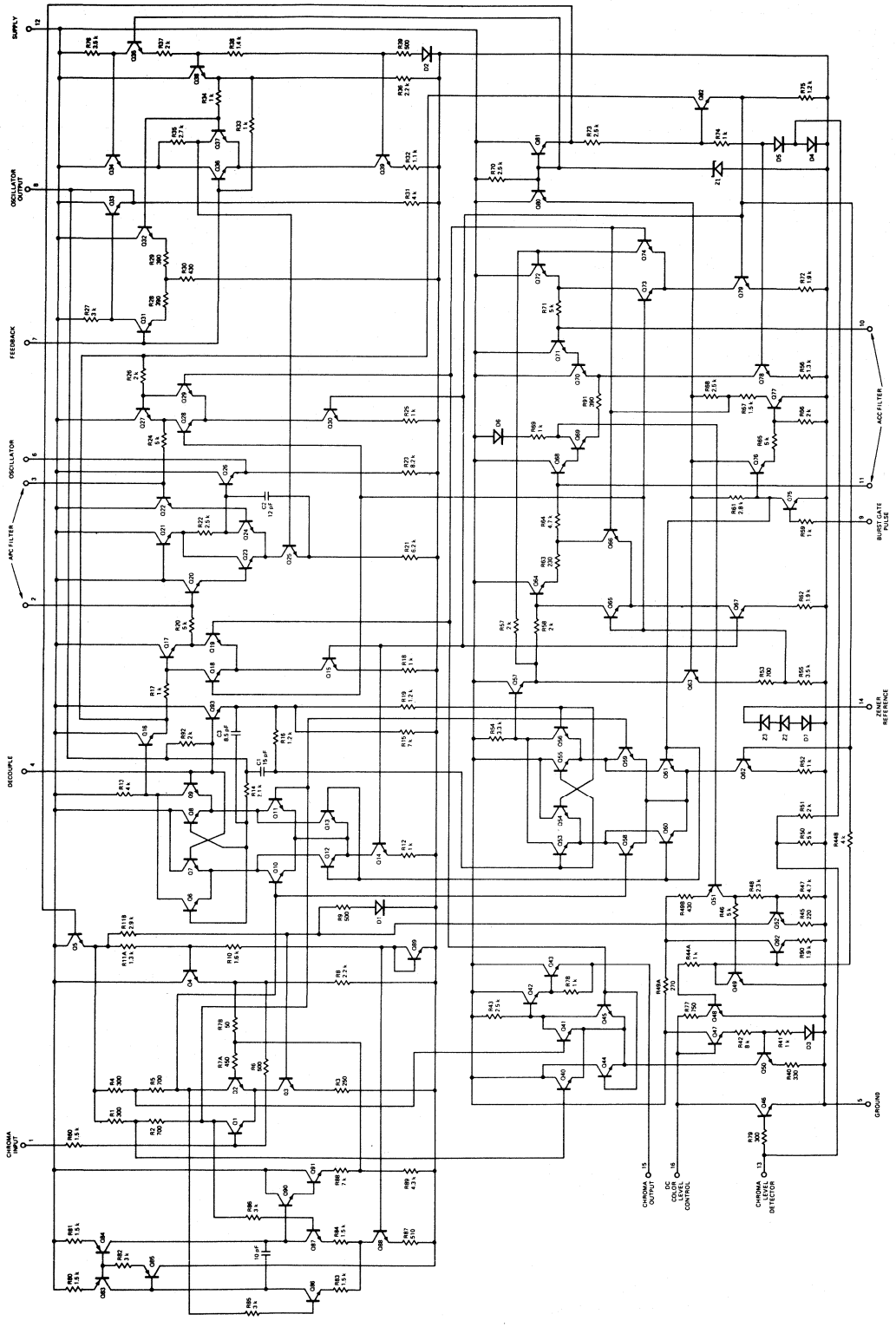


CHROMA OUTPUT AS A FUNCTION OF DC COLOR LEVEL CONTROL VOLTAGE

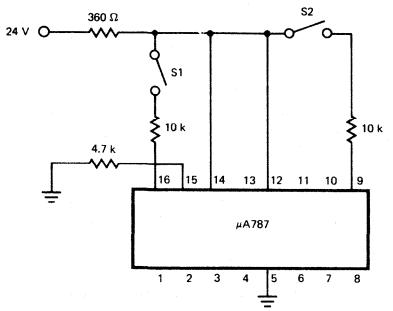


ACC — Output controlled by ACC only
ACL – 1 — Output partially controlled by ACL
ACL – 2 — Output fully controlled by ACL

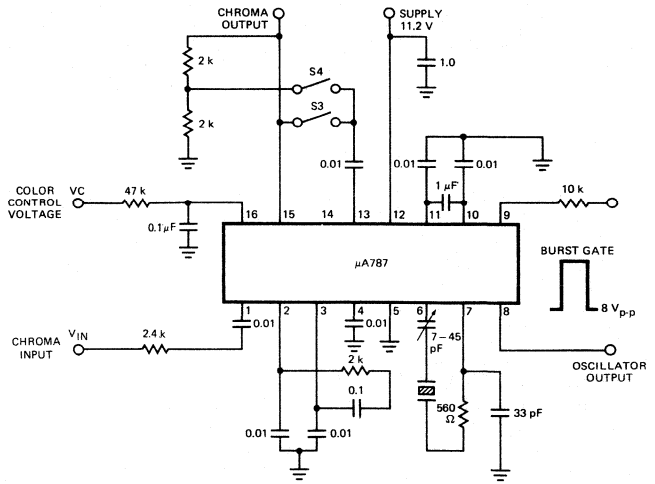
EQUIVALENT CIRCUIT



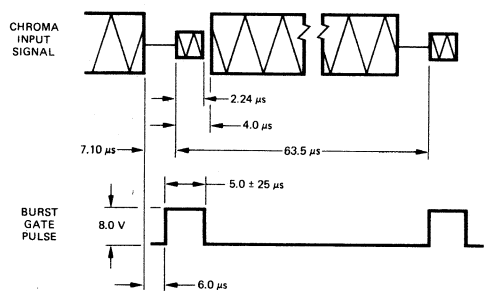
DC TEST CIRCUIT 1



AC TEST CIRCUIT 2



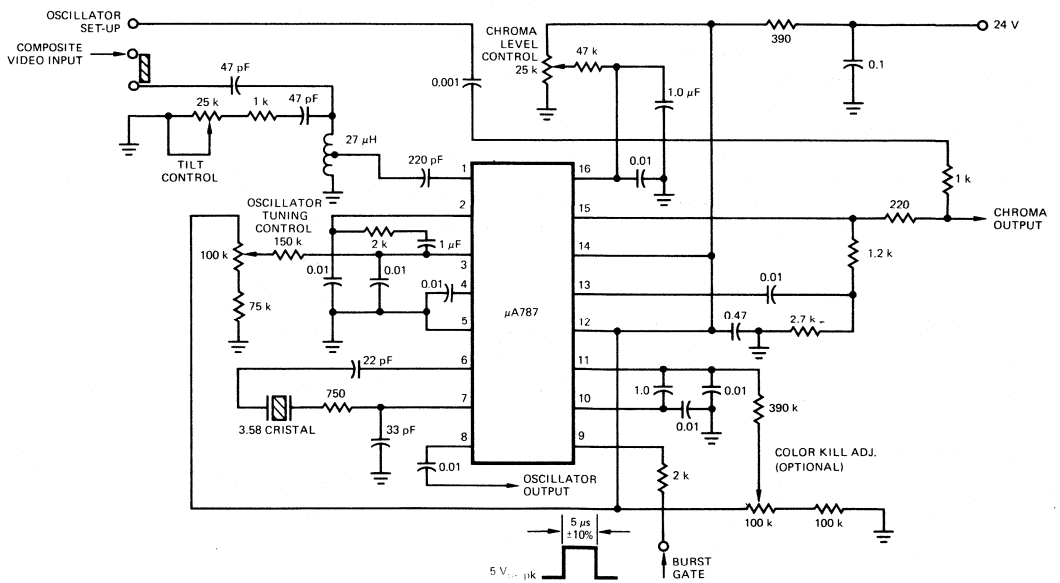
AC TEST SIGNAL (V_{IN})



Burst: 8 Cycles –3.58 MHz amplitude is 46.5% of chrominance with first and last cycle being at least 85% full amplitude. Amplitude of remaining cycles shall be within 5% of specification value. Chroma amplitude is 0.5 V Peak-to-Peak.

NOTES
1. Burst position during blanking interval may be altered if necessary.
2. Chrominance duration is 52 μs.
3. Burst gate pulse applied to test circuit is timed to coincide with burst.

TYPICAL APPLICATION



μA788

TV CHROMA DEMODULATOR AND DC TINT CONTROL

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA788 is a monolithic chroma demodulator with a dc tint control. It is constructed using the Fairchild Planar* epitaxial process. The device adds the luminance and color difference signals and provides direct coupled color signals to the video output drivers. The tint control section of the IC has a constant amplitude output with dc phase control.

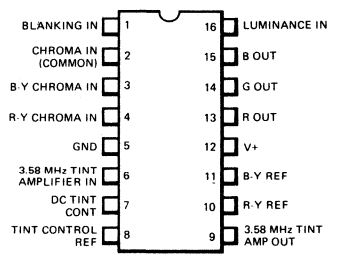
The μA788 will interface with several chroma processing systems, e.g., 3066 or μA780/μA781, but is intended to complement the μA787 chroma processing IC to form a 2-chip chroma system with optimum performance.

- **10 V PEAK-TO-PEAK BLUE OUTPUT**
- **INTERNAL SUBCARRIER FILTERING**
- **COLOR DIFFERENCE OR RGB SIGNALS AT THE OUTPUT**
- **LUMINANCE SIGNAL INPUT**
- **HORIZONTAL RETRACE BLANKING PULSE INPUT**
- **DC TINT CONTROL**
- **TINT RANGE ADJUSTABLE TO 150**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+)	28 V
Power Dissipation	730 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature Molded DIP (soldering, 10 s)	260°C
Luminance Input Voltage	Supply Voltage (V+)
Minimum Tint Control Reference Load Resistance (Pin 8)	8.0 kΩ
Minimum Output Load Resistance (Pins 9, 13, 14, 15)	3.0 kΩ
Peak-to-Peak Reference Voltage (Pins 10, 11)	5.0 V
Peak-to-Peak Chroma Voltage (Pins 2, 3, 4)	5.0 V
Blanking Input Voltage	−3.0 V to +7.0 V

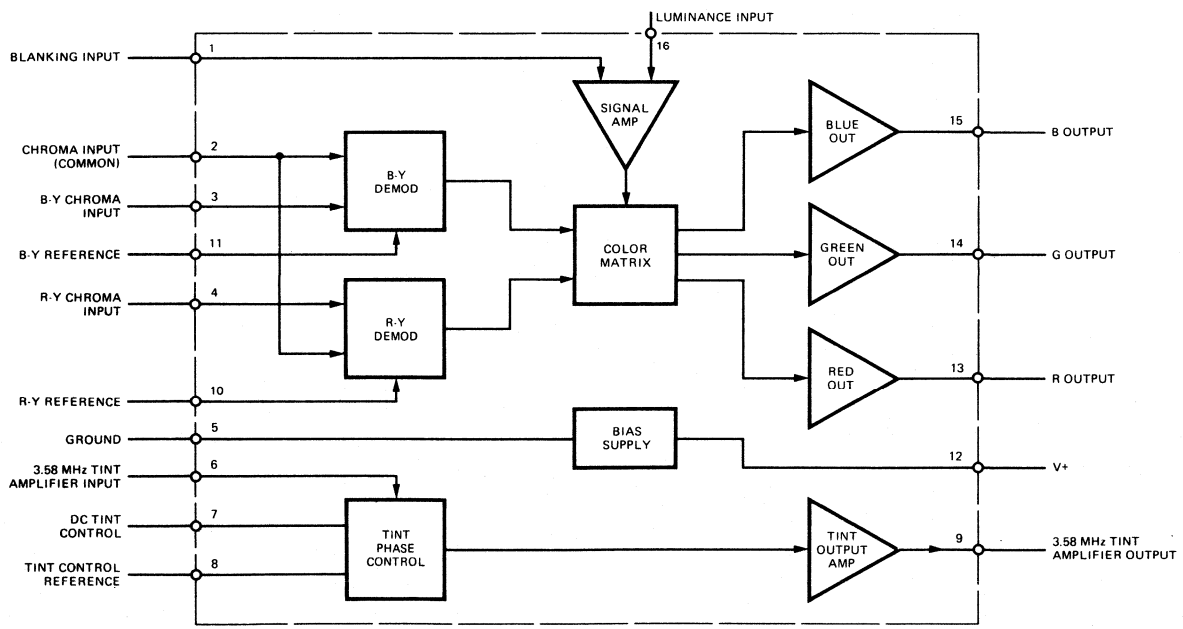
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B
PACKAGE CODE P



ORDER INFORMATION

TYPE	PART NO.
788	μA788PC

BLOCK DIAGRAM



DC CHARACTERISTICS (T_A = 25°C, V+ = 24 V, Test Circuit 1, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Bias Voltages					
Blanking Input (V1)	S1 Closed		1.2		V
Common Chroma Input (V2)			3.0		V
B-Y, R-Y Chroma Input (V3, V4)			3.0		V
3.58 MHz Tint Input (V6)			3.0		V
DC Tint Phase Control Input (V7)			5.6		V
Tint Phase Control Reference (V8)			11.2		V
3.58 MHz Tint Output (V9)			16		V
R-Y, B-Y Reference Input (V10, V11)			5.6		V
Demodulator Output (V13, V14, V15)		13	14.5	16	V
Luminance Input (V16)			23.8		V
Supply Current			25	33	mA
Blanking Input Current (I1)	V1 = 5.0 V		4.5		mA
Luminance Input Resistance (Pin 16)			100		kΩ
Chroma Input Resistance (Pins 2, 3, 4)			2.0		kΩ
Chroma Input Capacitance (Pins 2, 3, 4)			5.0		pF
Reference Input Resistance (Pins 10, 11)			2.0		kΩ
Reference Input Capacitance (Pins 10, 11)			6.0		pF
3.58 MHz Tint Amp Input Resistance (Pin 6)			2.0		kΩ
3.58 MHz Tint Amp Input Capacitance (Pin 6)			3.0		pF
3.58 MHz Tint Amp Output Resistance (Pin 9)			200		Ω
Demodulator Output Temperature Coefficient (V13, V14, V15)			−3.0		mV/°C

AC CHARACTERISTICS (T_A = 25°C, V+ = 24 V, Test Circuit 2, unless otherwise specified.)

Tint Amp Output Voltage (V9)		1.0	2.0		V_{p-p}
Maximum Available Tint Range			150		Degrees
Blue Output Voltage	Chroma Input V3 = V4 = 0.7 V_{p-p}	6.0	8.0		V_{p-p}
B-Y Demodulator Conversion Gain	Blue Output V15 = 5.0 V_{p-p}	10	16		V/V
Demodulator Output Gain Relative to B-Y Output (V15)	B-Y Output (V15) Normalized to 1.0				
R-Y Output (V13)		0.65	0.76	0.84	
G-Y Output (V14)		0.15	0.20	0.25	
Demodulator Output Phase Angle Relative to B-Y Output	B-Y Output Phase Normalized to 0°				
R-Y Output (V13)		101	106	111	Degrees
G-Y Output (V14)		248	256	264	Degrees
Differential Voltage Between Any Two Demodulator Outputs (V13, V14, V15)	Chroma Input = 0		0.3		V
Demodulator ac Unbalance Voltage (V13, V14, V15)	Chroma Input = 0		0.2		V_{p-p}
Gain From Luminance Input	S2 Closed				
(Lead 16) to Demodulator Outputs	f = 1.0 kHz		0.95		V/V
	f = 5.0 MHz		0.5		V/V

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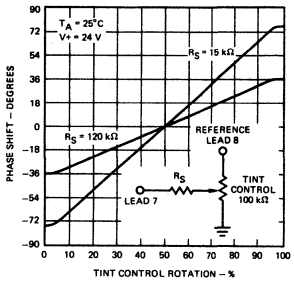
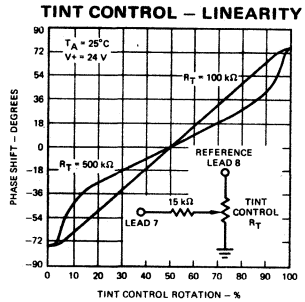
TYPICAL PERFORMANCE CURVES

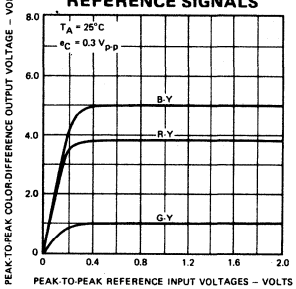
TINT CONTROL – RANGE



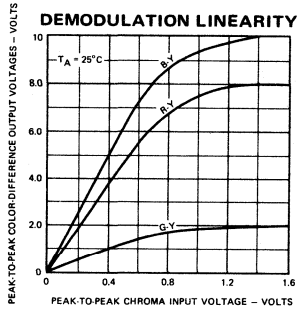
TINT CONTROL – LINEARITY



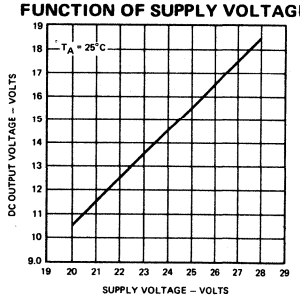
DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS



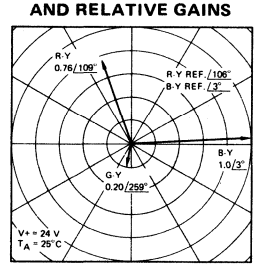
DEMODULATION LINEARITY



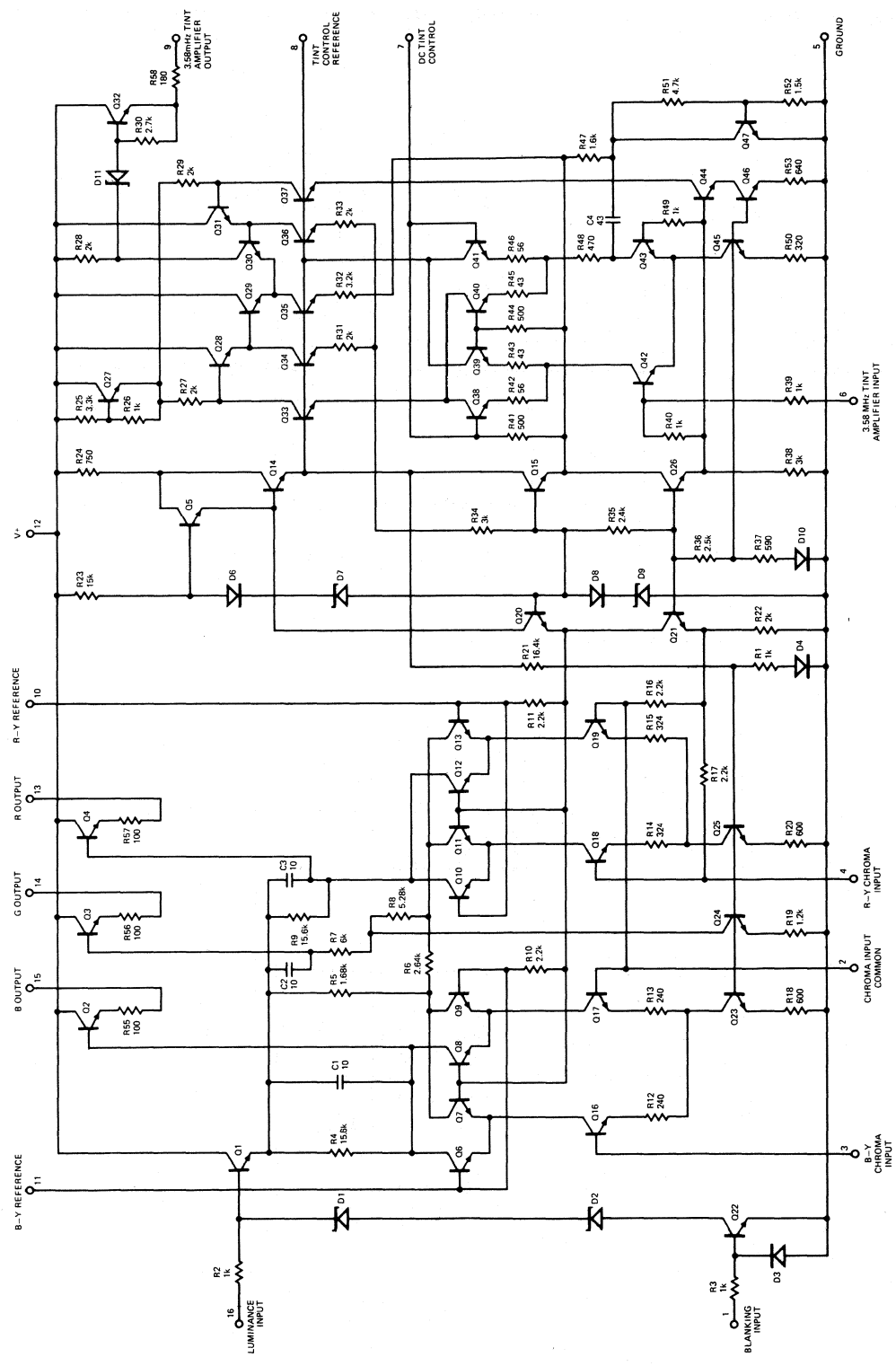
DC VOLTAGE AT ANY DEMODULATOR OUTPUT AS A FUNCTION OF SUPPLY VOLTAGE



DEMODULATION ANGLES AND RELATIVE GAINS



EQUIVALENT CIRCUIT



ALL RESISTOR VALUES ARE IN OHMS AND ALL CAPACITOR VALUES ARE IN PICO FARADS.

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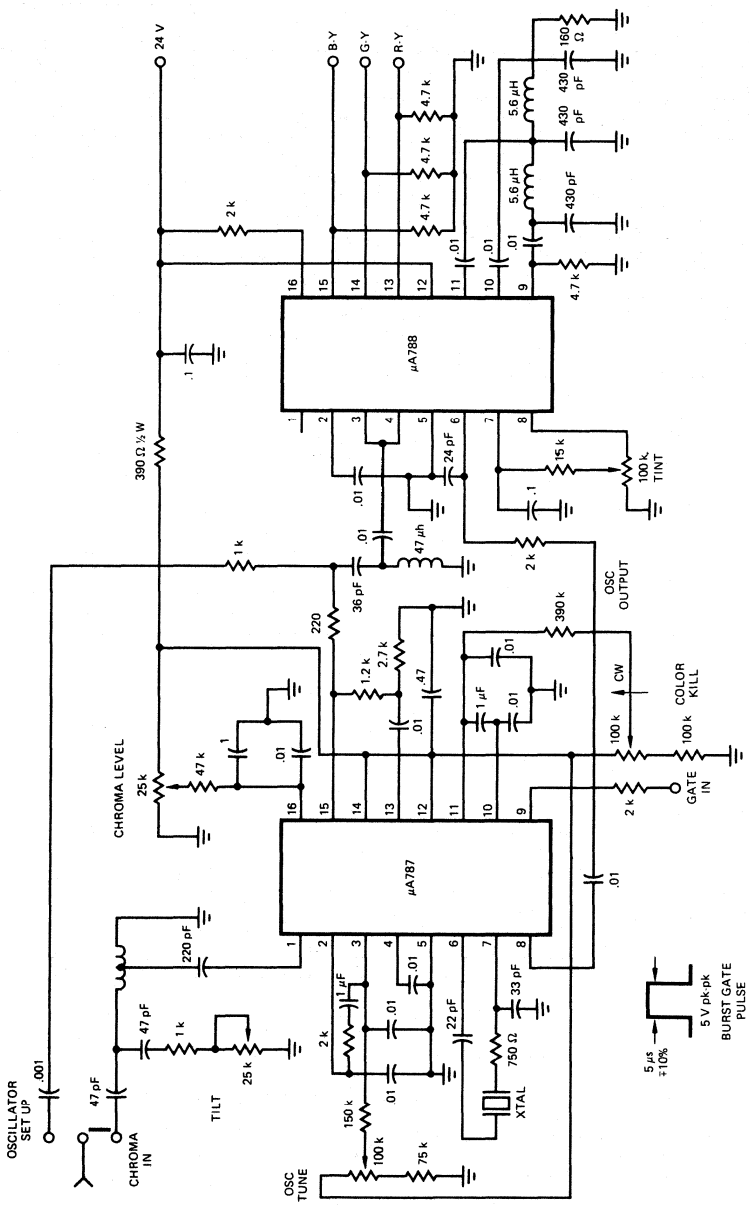
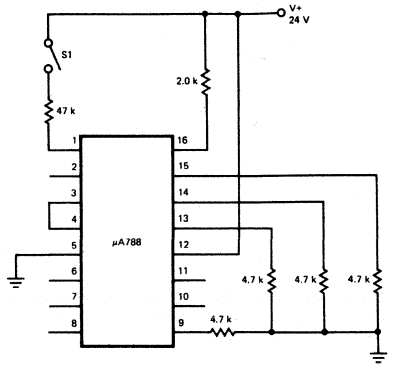
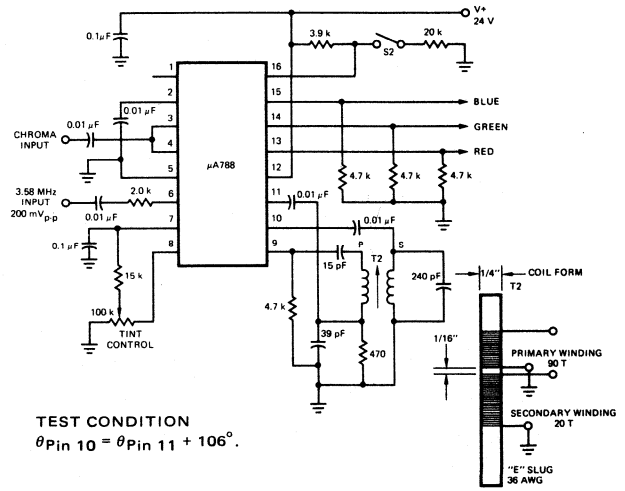
TYPICAL APPLICATION



TEST CIRCUIT 1



TEST CIRCUIT 2



TEST CONDITION

$\theta_{Pin\ 10} = \theta_{Pin\ 11} + 106°$.

10

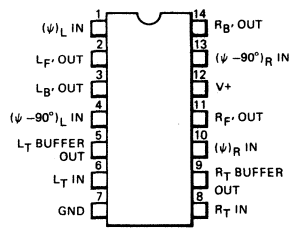
μA1312

MONOLITHIC CBS SQ** DECODER

GENERAL DESCRIPTION – The 1312 is a matrix circuit which decodes SQ** encoded program material into four separate channels. SQ** quadrophonic signals are decoded without sacrificing high fidelity characteristics and with no change in signal level. The circuit is constructed using the Fairchild Planar* epitaxial process.

- **LOW TOTAL HARMONIC DISTORTION – 0.1 % TYP.**
- **HIGH INPUT IMPEDANCE – 3 MΩ TYP.**
- **HIGH SIGNAL HANDLING CAPABILITY – 2.0 V RMS MIN.**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACAKGE CODE P



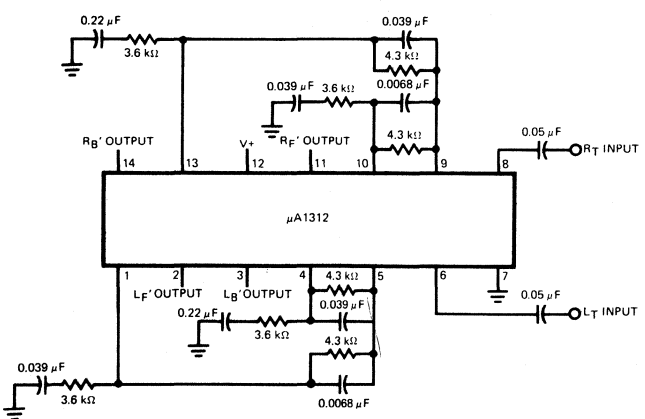
ORDER INFORMATION

TYPE	PART NO.
μA1312	μA1312PC

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	25 V dc
Operating Temperature Range	0 to +75°C
Storage Temperature Range	−65 to +150°C
Power Dissipation at T_A = 25°C	625 mW
Derate Above T_A = 25°C	5 mW/°C

TYPICAL APPLICATION



DEFINITIONS

L_T = Left total	R_T = Right total
L_F' = Left front	L_B' = Left back
R_F' = Right front	R_B' = Right back

NOTES:
1. For optimum performance, ±5% tolerance components are recommended with the exception of coupling capacitors.
2. Since dc voltages appear on output terminals it is recommended that coupling capacitors be used.
3. Refer to Figs. 5 and 6 for recommended blend circuits.

Fig. 1

**Trademark of CBS Inc.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 20 Vdc, V_{IN} = 0.5 V (rms), unless otherwise specified; See Fig. 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Drain		11	16	21	mA
Input Impedance		1.8	3.0		MΩ
Output Impedance			5.0		kΩ
Channel Balance (L_F/R_F)		−1.0	0	+1.0	dB
Voltage Gain (L_F/L_T or R_F/R_T)		−1.0	0	+1.0	dB
Relative Voltage Gain (L_B'/L_F', R_B'/L_F', L_B'/R_F', R_B'/R_F') L_F' measurements made with L_T input, R_F' measurements made with R_T input		−4.0	−3.0	−2.0	dB
Maximum Input Voltage (R_T or L_T)	1% THD at Output	2.0			V(rms)
Total Harmonic Distortion (R_T or L_T)			0.1		%
Signal to Noise Ratio (Short Circuit Input)	V_{OUT} = 0.5 V (rms), BW = 20 Hz to 20 kHz		80		dB

TYPICAL PERFORMANCE CURVE

CURRENT DRAIN AS A FUNCTION OF SUPPLY VOLTAGE

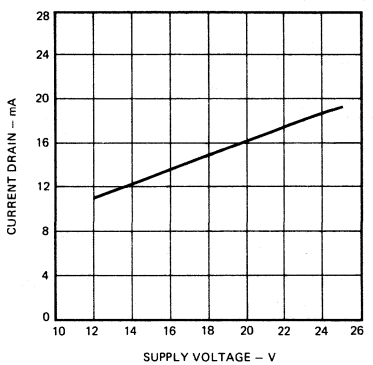
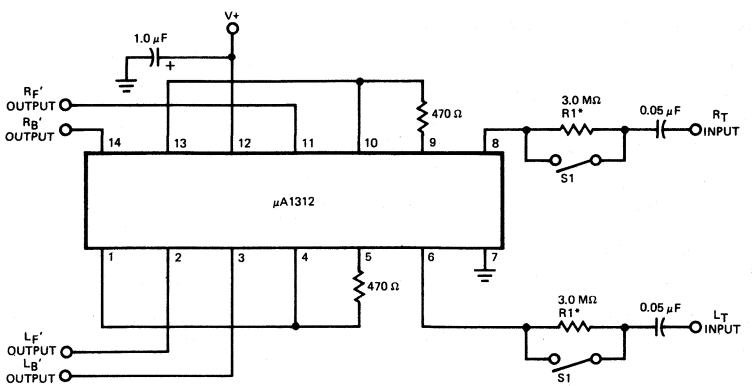


Fig. 2

TEST CIRCUIT

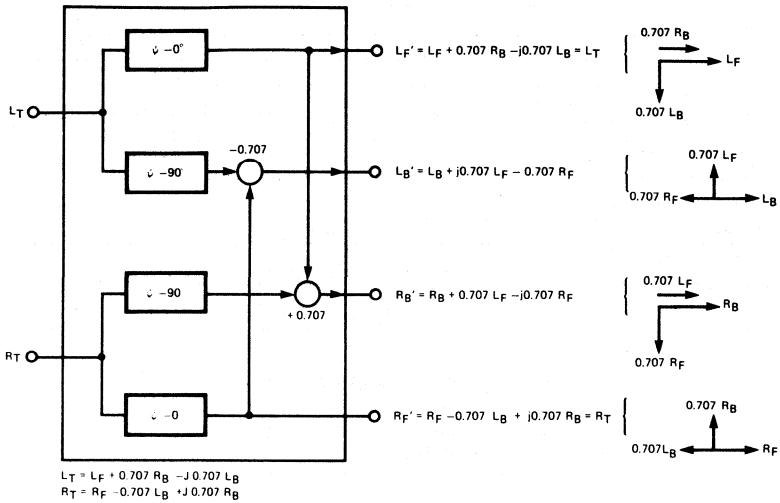


*R1 is used for input impedance measurement. S1 is normally closed.

Fig. 3

APPLICATIONS INFORMATION

DECODING PROCESS DIAGRAM



L_T and R_T are composite signals from SQ encoded records or SQ broadcast.

Fig. 4

The decoding process is shown schematically in Figure 4. The 1312 circuits which perform this function consist of two preamplifiers which are fed with left total (L_T) and right total (R_T) signals. The preamplifiers each feed two all-pass[1] networks that are used to generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left front (L_F'), right front (R_F'), left back (L_B') and right back (R_B') signals.

The all-pass networks are of the Wein bridge form with the resistive arms realized in the integrated circuit and the RC arms formed by external components. The values shown in Figure 1 are for a 100 Hz to 10 kHz bandwidth and a phase ripple of ± 8.5° on a 90° phase difference.

It is generally desirable to enhance center front to center back separation. Figure 5 shows an electrical configuration which may be used to accomplish 10% front channel blending and 40% back channel blending. The corresponding equations are:

$$R_F'' = 0.912L_T + 0.088R_T$$

$$L_F'' = 0.912R_T + 0.088L_T$$

$$R_B'' = \frac{\sqrt{2}}{2}\left[0.714\ (jR_T - L_T) + 0.286\ (R_T - jL_T)\right]$$

$$L_B'' = \frac{\sqrt{2}}{2}\left[0.714\ (jL_T - R_T) + 0.286\ (L_T - jR_T)\right]$$

To meet the EIA matrix standards with 10/40 blend, refer to the circuit in Figure 6. The equations are:

$$R_F'' = 0.772\ (0.995R_T + 0.0972L_T)$$

$$L_F'' = 0.772\ (0.995L_T + 0.0972R_T)$$

$$R_B'' = \frac{\sqrt{2}}{2}(0.769)\left[0.928\ (jR_T - L_T) + 0.372\ (R_T - jL_T)\right]$$

$$L_B'' = \frac{\sqrt{2}}{2}(0.769)\left[0.928\ (jL_T - L_T) + 0.372\ (L_T - jR_T)\right]$$

[1] An all-pass network produces phase shift without amplitude variations.

CIRCUIT FOR 10/40 BLEND

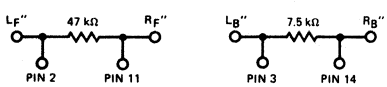


Fig. 5

EIA STANDARD BLEND

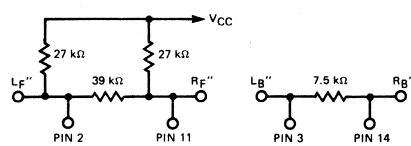


Fig. 6

μA2136

FM IF AMPLIFIER/LIMITER/DETECTOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

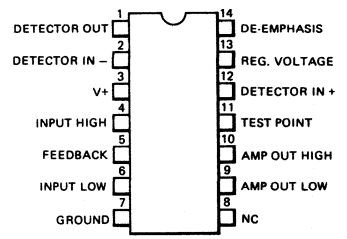
GENERAL DESCRIPTION – The 2136 is a monolithic three-stage limiting amplifier and FM detector circuit constructed using the patented Fairchild Planar* epitaxial process. The chip also contains a regulator which reduces parameter variations with temperature and applied supply voltage. The stabilized dc outputs of the regulator and the detector make the device especially suited for AFC applications using varactor diodes. The device is designed as a pin-to-pin substitute for the ULN2136. With minor changes in external components, it also serves as a replacement for the ULN2111 and similar products. In these applications the regulated output terminal (pin 13) is used as the supply terminal.

- **EXCELLENT AM REJECTION – 40 dB TYPICAL AT 10.7 MHz**
- **QUADRATURE DETECTOR EMPLOYING SINGLE TUNED CIRCUIT**
- **ACTIVE CIRCUITRY PERFORMANCE INSENSITIVE TO SUPPLY VARIATIONS**
- **TEMPERATURE STABILIZED VOLTAGE REGULATOR IS SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:	
(Used as μA2136) Supply on Pin 3	+20 V
(Used as μA2111) Supply on Pin 13	+15 V
Input Voltage (Pin 4)	+3.5 V
Power Dissipation (Note 1)	670 mW
Regulator Output Current (Pin 13)	30 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P

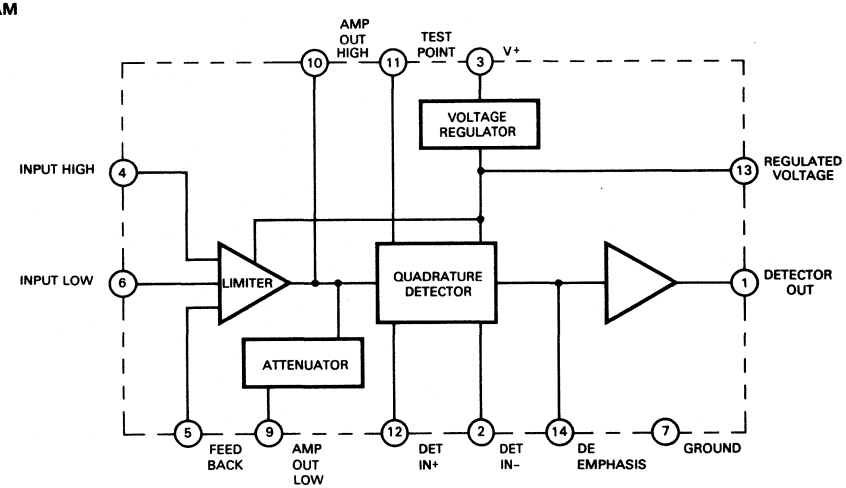


ORDER INFORMATION

TYPE	PART NO.
μA2136	μA2136DC
μA2136	μA2136PC

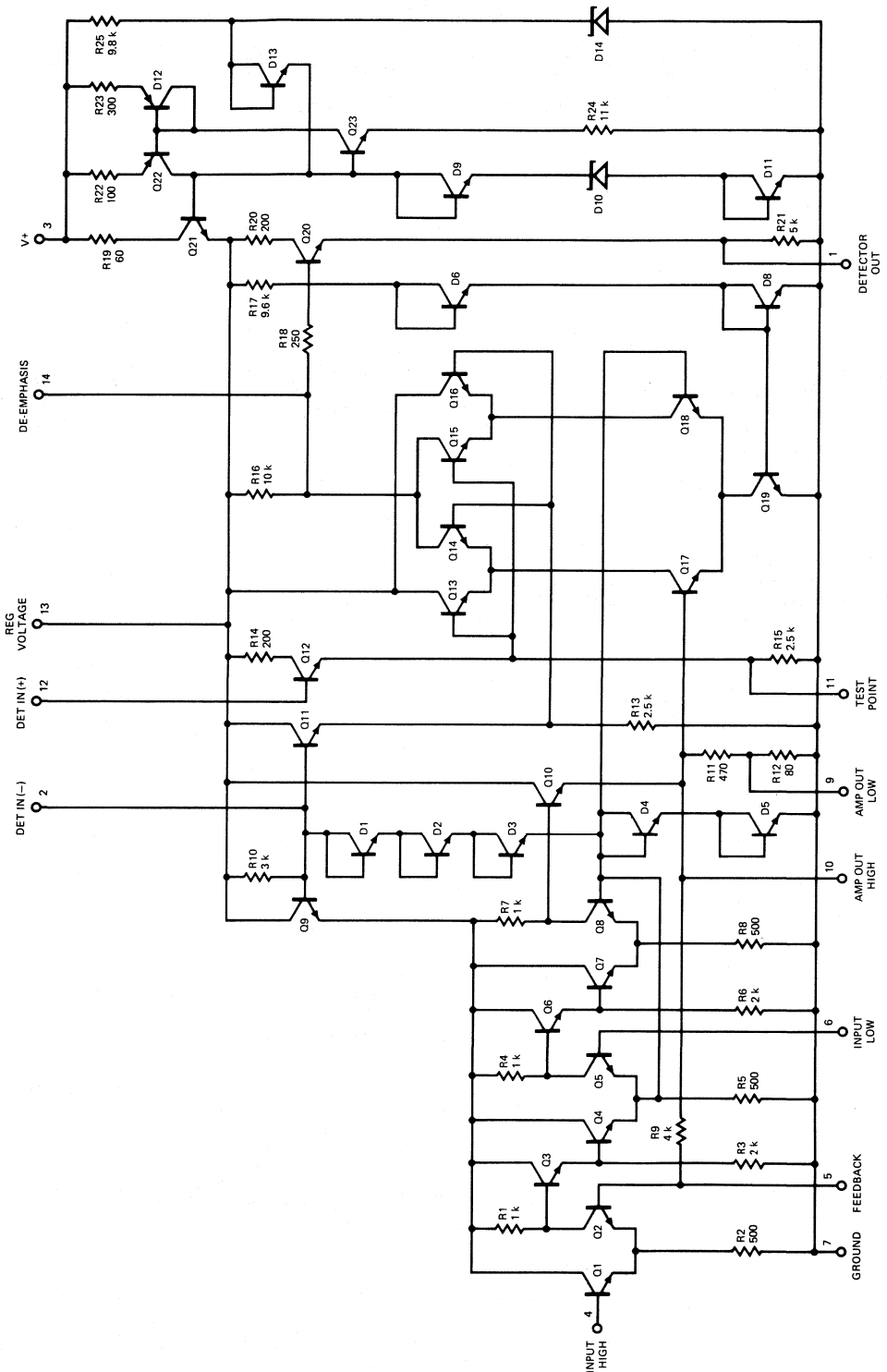
10

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A = 25°C, Supply Voltage - 12 V, See Test Circuit, Note 2, unless otherwise specified)

DC CHARACTERISTICS (V_{IN} = 0 V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_3	Pin 13 open	12	17	22	mA
Detector Output Level	V_1		3.0	3.8	4.6	V
Temperature Sensitivity of V_1		I_{13} = 20 mA		+1.5		mV/°C
Temperature Sensitivity of V_{13}		I_{13} = 20 mA		+1.5		mV/°C
De-Emphasis Resistance	R_{14}		7.0	10	13	kΩ
Amplifier Input Resistance	R_{IN4}			5.0		kΩ
Amplifier Input Capacitance	C_{IN4}			11		pF
Detector Input Resistance	R_{IN12}			70		kΩ
Detector Input Capacitance	C_{IN12}			2.7		pF
Amplifier HIGH Output Resistance	R_{OUT10}			60		Ω
Detector Output Resistance	R_{OUT1}			200		Ω

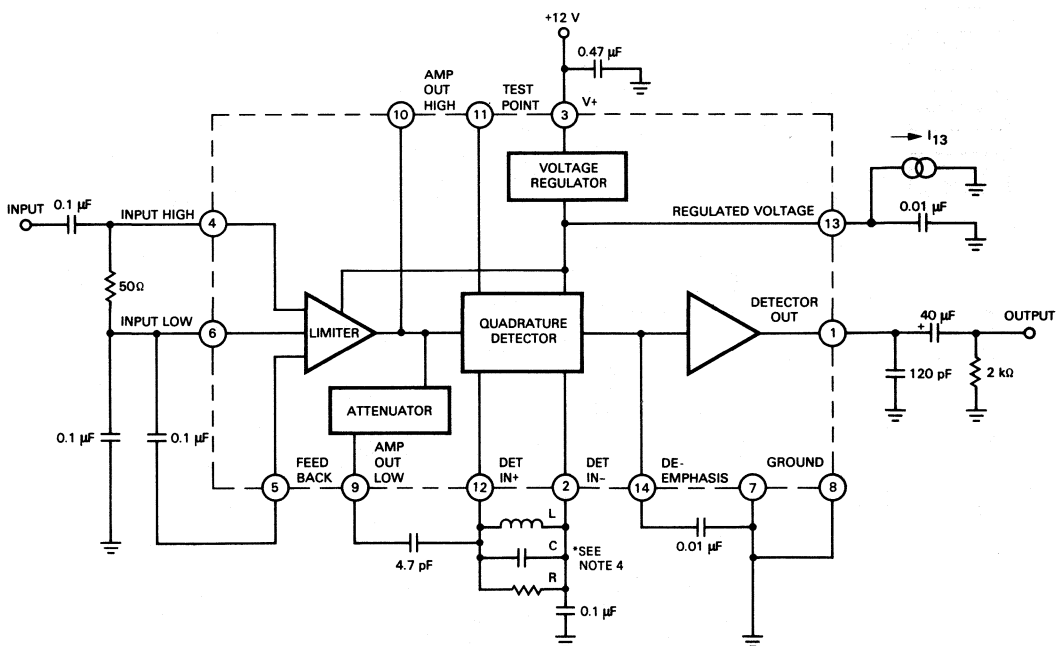
AC CHARACTERISTICS (f_o = 10.7 MHz, Deviation = ±75 kHz, Modulation Frequency = 400 Hz)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Voltage Gain	$V_G = V_{10}/V_4$	$V_{IN} < 0.3\ mV_{RMS}$		56		dB
Input Limiting Threshold	V_{TH}	Recovery Audio = V_{OUT} −3.0 dB		450	800	μV_{RMS}
Recovered Audio Output	V_{OUT}	V_{IN} = 10 mV_{RMS}		400		mV_{RMS}
Output Distortion	THD	V_{IN} = 10 mV_{RMS}		1.0	3.0	%
AM Rejection	AMR	(Note 3)		40		dB
Line Regulation	$\Delta V_{13}/\Delta V_3$	I_{13} = 20 mA		5.0	25	mV/V

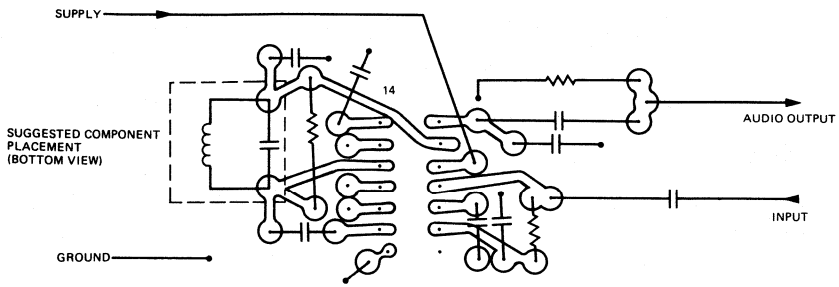
NOTES:
1. Rating applies up to 70°C operating temperature. Derate 8.3 mW/°C between 70°C and 85°C.
2. The tank circuit parameters apply to the finished test jig. They are measured between pins 12 and 2 without IC inserted.
3. $AMR = 20 \log \frac{V_{OUT} \text{ at 10 mV FM, 100\% modulated with } f_m = 400 \text{ Hz}}{V_{OUT} \text{ at 10 mV AM, 10.7 MHz, 30\% modulated with } f_m = 400 \text{ Hz}}$
4. Tank circuit values: L = 1.5 – 3 μH, C = 120 pF, R = 3.9 kΩ, Q_L = 20 ± 5%.

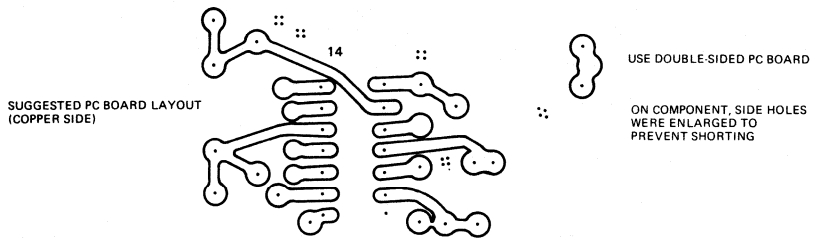
10

TEST CIRCUIT

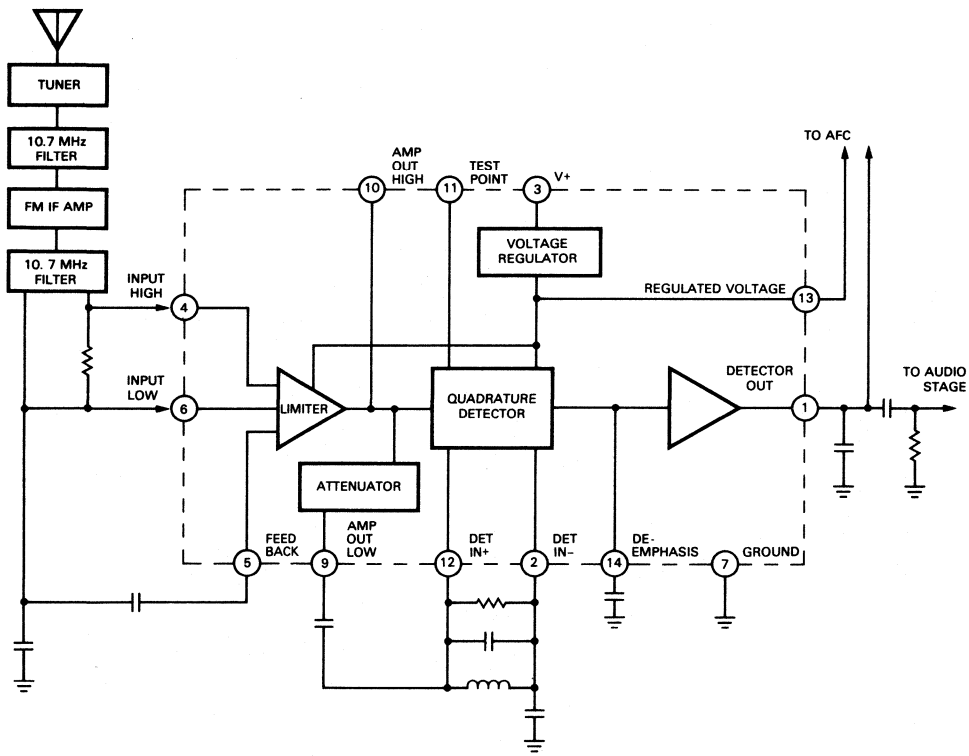


PC BOARD LAYOUT





TYPICAL APPLICATIONS



μA3064

TV AUTOMATIC FINE-TUNING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3064 is a monolithic TV Automatic Fine-Tuning Circuit constructed using the Fairchild Planar* epitaxial process. The 3064 combines all of the automatic fine-tuning circuitry, except transformers, in one integrated circuit. Systems with low level IF amplifiers can now achieve tuning accuracies of ±25 kHz due to the 3964's high sensitivity. Internal voltage regulation improves overall performance and reduces system cost.

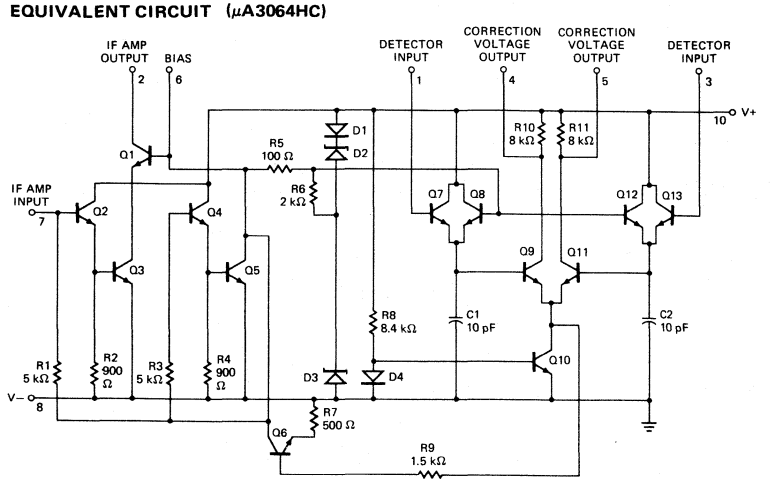
- **HIGH SENSITIVITY**
- **25 kHz MAX. FREQUENCY DEVIATION**
- **INTERNAL VOLTAGE REGULATOR**
- **INTERNAL AGC**

ABSOLUTE MAXIMUM RATINGS (Note 1)

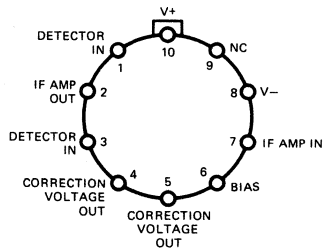
Supply Voltage	(Note 2)
Internal Power Dissipation (Note 3)	700 mW
Detector Differential Voltage ($V_{1\text{-}3}$)	±10V
Detector Input Voltage Range (V_1, V_3)	+5V, –6V
I.F. Amp Output (V_2)	+20V, 0V
Bias Voltage (V_6)	+2V, 0V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering, 60 s) HC	300°C
Lead Temperature (Soldering, 10 s) PC	260°C

NOTES:
(1) All voltages referenced to V_ except as noted.
(2) V_+ terminal may be connected to any positive voltage source through a suitable dropping resistor, provided the dissipation rating is not exceeded.
(3) Derate linearly at 5.6 mW/°C for ambient temperatures above +25°C.

EQUIVALENT CIRCUIT (μA3064HC)



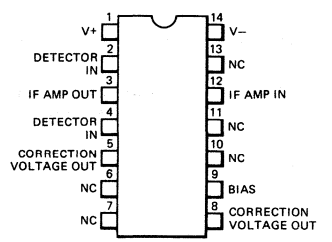
CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3064	μA3064HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



ORDER INFORMATION

TYPE	PART NO.
μA3064	μA3064PC

*Planar is a patented Fairchild process.

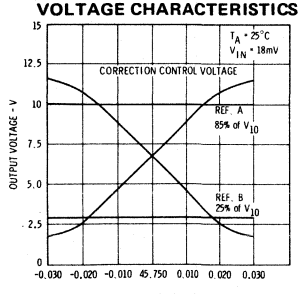
10

ELECTRICAL CHARACTERISTICS (V_+ = +30V, R_S = 1.5 kΩ, T_A = 25°C, Test Circuit 1, unless otherwise specified.)
(Pin Connections for H Package)

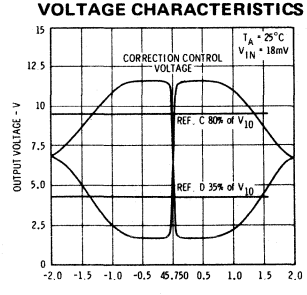
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Consumption	T_A = +25°C	130	140	150	mW
	T_A = −25°C		135	150	mW
	T_A = +85°C		145	150	mW
Supply Current — I+	V_{10} = +10.5V Test Ckt 2	4.0	6.5	9.5	mA
Regulated Supply Voltage — V_+	Test Ckt 2	10.9	11.8	12.8	V
Quiescent Operating Current — I_2		1.0	2.0	4.0	mA
Quiescent Operating Voltages — V_4, V_5		5.0	6.9	8.0	V
Output Offset Voltage — (V_4−V_5)		−1.0	0	1.0	V
Input Admittance — Y_{11}	f = 45.75 MHz		0.41 + j 1.0		mmho
Reverse Transfer Admittance — Y_{12}	f = 45.75 MHz		0 + j 3.4		μmho
Forward Transfer Admittance — Y_{21}	f = 45.75 MHz		24.5 − j 29		mmho
Output Admittance — Y_{22}	f = 45.75 MHz		0.04 + j 0.9		mmho
Correction Control Voltage — V_4 (Test Circuit 1)	V_{IN} = 18 mV RMS f_o = 45.750 MHz Δf as listed (MHz) −0.030	85			% V_+
	+0.030			25	% V_+
	−0.900	80			% V_+
	+0.900			35	% V_+
	−1.500			80	% V_+
	+1.500	35			% V_+
Correction Control Voltage — V_5 (Test Circuit 1)	V_{IN} = 18 mV RMS f_o = 45.750 MHz Δf as listed (MHz) −0.030			25	% V_+
	+0.030	85			% V_+
	−0.900			35	% V_+
	+0.900	80			% V_+
	−1.500	35			% V_+
	+1.500			80	% V_+

TYPICAL PERFORMANCE CURVES FOR 3064

NARROW-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

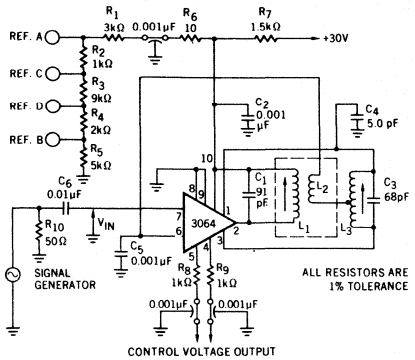


WIDE-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS



NOTE: See test circuit 1.

TEST CIRCUIT 1
CORRECTION VOLTAGES
(Pin Connections for H Package)



NOTE: Parts placement is critical. Use P.C. board layout on last page for best results.

L_1 is aligned for symmetrical bandwidth on either side of 45.750 MHz.

L_2 tertiary winding wound on L_1 coil form.

L_3 is aligned for zero differential output between terminals 4 and 5 at f_o = 45.750 MHz.

REFERENCE VOLTAGE PERCENTAGES	
Ref. A	85% of V_{10}
Ref. B	25% of V_{10}
Ref. C	80% of V_{10}
Ref. D	35% of V_{10}

COIL DATA FOR DISCRIMINATOR WINDINGS

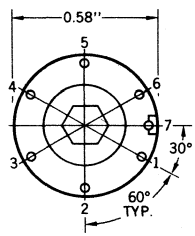
L_1 – Discriminator Primary: 3 1/16 turns; #20, Enamel-covered wire–close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz. Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2 1/16 turns; #20 Enamel-covered wire–close wound over botton end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3 1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz. Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

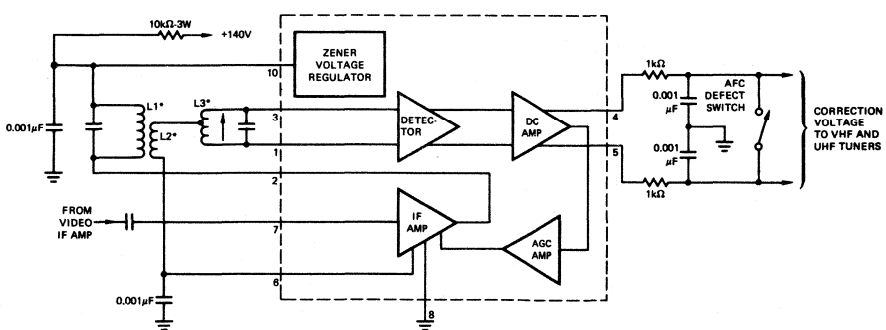
NOTES:
1. Coil Forms; Cylindrical; 0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

COIL FORM BASE TERMINAL DIAGRAM



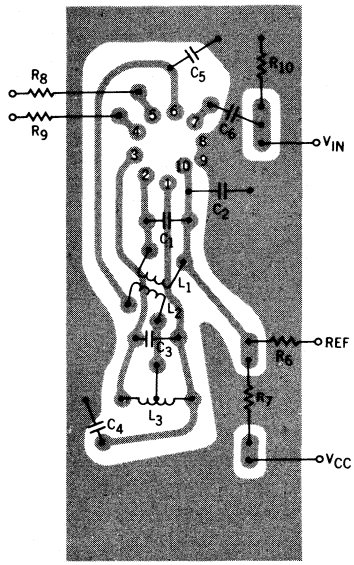
Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

BLOCK DIAGRAM
(Pin Connections for H Package)

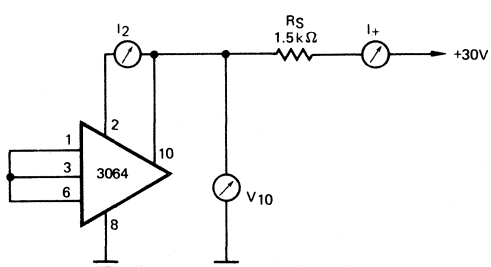


10

PRINTED CIRCUIT BOARD FOR CORRECTION VOLTAGE TEST CIRCUIT
(Full Size Bottom View)



TEST CIRCUIT 2
Regulated Voltage, Total Supply Current and Quiescent Current at Terminal 2
(Pin Connections for H Package)



μA3065

TV SOUND SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3065 is a monolithic TV Sound System constructed using the Fairchild Planar* epitaxial process. It contains a multi-stage limiting IF amplifier, dc gain (volume) control, FM detector and an audio driver. Excellent sensitivity, high AM rejection and an internally regulated supply, coupled with low external component requirements make the 3065 ideally suited for TV sound channels.

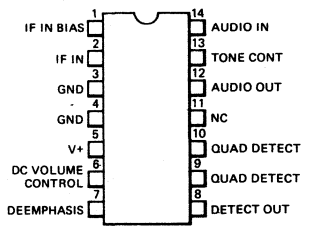
- **DC VOLUME CONTROL ELIMINATES NEED FOR SHIELDED CABLES**
- **EXCELLENT AM REJECTION – 50 dB TYPICAL AT 4.5 MHz**
- **DIFFERENTIAL PEAK DETECTOR REQUIRES ONLY ONE SINGLE-TUNED COIL**
- **INTERNAL ZENER DIODE REGULATED SUPPLY**
- **LOW HARMONIC DISTORTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	Note 1
Internal Power Dissipation (Note 2)	670 mW
Power Supply Current	50 mA
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature	
Molded DIP (Soldering, 10 s) μA3065PC	260°C

NOTES
1. V_+ terminal may be connected to any positive voltage through a suitable dropping resistor, provided the dissipation rating is not exceeded.
2. Rating applies to ambient temperature up to 70°C. Derate linearly at 8.3 mW/°C above 70°C.

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P

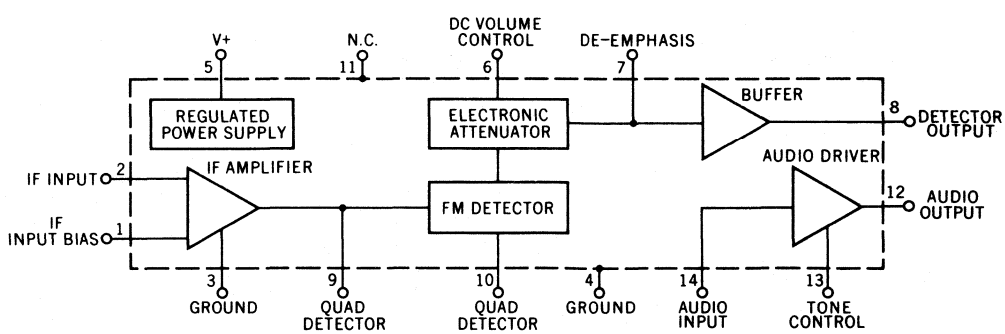


ORDER INFORMATION

TYPE	PART NO.
μA3065	μA3065PC

10

BLOCK DIAGRAM



*Planar is a patented Fairchild process

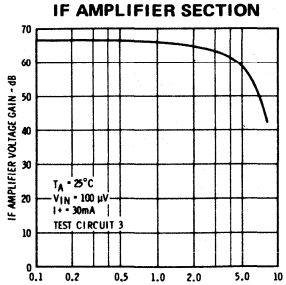
ELECTRICAL CHARACTERISTICS (T_A = 25°C, I+ = 30 mA unless otherwise specified)

PARAMETER	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Zener Regulating Voltage (V_5)			10.3	11.2	12.2	V
Supply Current (I_5)	V_+ = 9.0V		10	16	24	mA
Internal Power Dissipation	I_+ = 33 mA		343	370	400	mW
Voltage at IF Input Bias (V_1)				2.0		V
Voltage at DC Volume Control (V_6)				4.8		V
Voltage at De-emphasis (V_7)				6.1		V
Voltage at Quad Detector (V_9)				3.7		V
Voltage at Audio Output (V_{12})			4.0	5.1	5.8	V
AC CHARACTERISTICS						
IF AMPLIFIER Input Limiting Voltage at −3 dB point	f = 4.5 MHz			200	400	μV
AM Rejection	f_o = 4.5 MHz, FM ± 25 kHz at 400 Hz, V_{IN} = 100 mV AM = 30% at 1 kHz		40	50		dB
IF Transconductance Magnitude Phase Angle	f = 4.5 MHz			 500 45		 mmho degrees
Feedback Capacitance	f = 1.0 MHz, Pin 2 to Pin 9			<0.02		pF
Input Impedance Components Parallel Input Resistance Parallel Input Capacitance	f = 4.5 MHz, Pin 1 to Pin 2			 17 4.0		 kΩ pF
Output Impedance Components Parallel Output Resistance Parallel Output Capacitance	f = 4.5 MHz, Pin 9 to Ground			 3.25 75		 kΩ pF
DETECTOR Recovered AF Voltage	(f_o = 4.5 MHz, FM = ±25 kHz at 400 Hz, V_{IN} = 100 mV)		 0.5	 0.75		 Vrms
Total Harmonic Distortion				0.9	2.0	%
Output Resistance De emphasis Output Detector Output				 7.5 300		 kΩ Ω
ATTENUATOR Max. Attenuation Max. Play-through Voltage*	 R_X = ∞ R_X = ∞		 60	 80 0.075	 1.0	 dB mV
AUDIO AMPLIFIER Voltage Gain Total Harmonic Distortion Undistorted Output Voltage Input Resistance Output Resistance	 V_{14} = 0.1 Vrms, f = 400 Hz V_{12} = 2 Vrms, f = 400 Hz THD = 5%, f = 400 Hz f = 400 Hz f = 400 Hz	 2 2 2	 17.5 2.0	 20 1.5 2.5 70 270	 	 dB % Vrms kΩ Ω

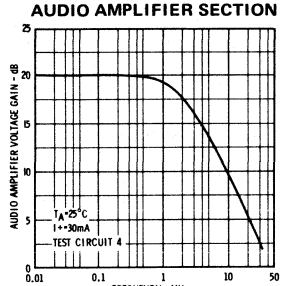
* Play-through voltage is the unwanted signal, measured at the detected output (Pin 8), when the volume control is set for minimum output.

TYPICAL PERFORMANCE CURVES FOR μA3065

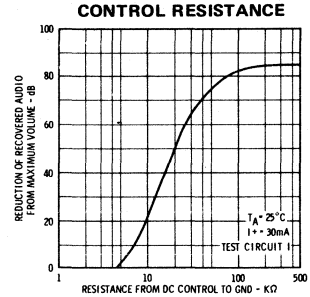
FREQUENCY RESPONSE OF IF AMPLIFIER SECTION



FREQUENCY RESPONSE OF AUDIO AMPLIFIER SECTION

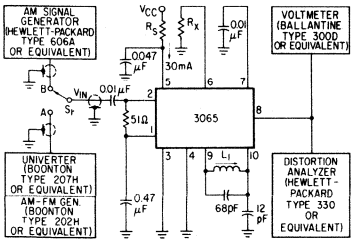


AUDIO GAIN REDUCTION VERSUS DC VOLUME CONTROL RESISTANCE



TEST CIRCUITS

INPUT LIMITING VOLTAGE, AM REJECTION, RECOVERED AUDIO, TOTAL HARMONIC DISTORTION, MAXIMUM ATTENUATION, MAXIMUM "PLAY-THROUGH" TEST CIRCUIT.



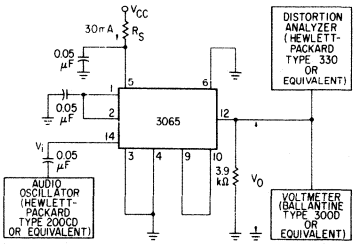
PINS 11, 12, 13, 14 NO CONNECTION

*L_1 = 16μH NOMINAL

$Q_{(UNLOADED)}$ = 50

TEST CIRCUIT 1

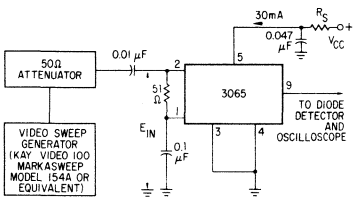
AUDIO VOLTAGE GAIN (UNDISTORTED OUTPUT)



PINS 7, 8, 11, 13 NO CONNECTION

TEST CIRCUIT 2

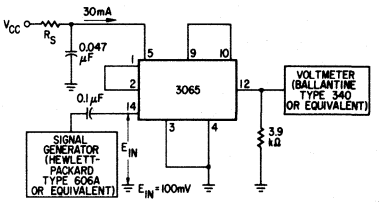
IF AMPLIFIER SECTION



E_{IN} = 100μVrms

TEST CIRCUIT 3

AUDIO AMPLIFIER SECTION

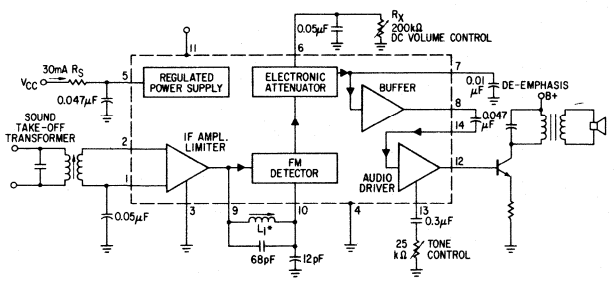


E_{IN} = 100 mV

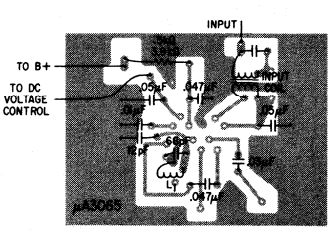
TEST CIRCUIT 4

TYPICAL APPLICATION

TV SOUND SYSTEM



SUGGESTED CIRCUIT LAYOUT COMPONENT SIDE



*L_1 = 16μH NOMINAL, $Q_{(UNLOADED)}$ = 50

μA3075

FM IF AMPLIFIER/LIMITER/DETECTOR/AUDIO PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3075 is a monolithic FM IF sub-system constructed using the Fairchild Planar* epitaxial process. The system consists of a three stage limiting amplifier with a zener diode regulated power supply, a differential peak detector stage and an internally biased audio preamplifier stage.

The IF amplifier stage provides typically 60 dB gain at 10.7 MHz and is followed by a differential limiting stage with constant current source to provide excellent limiting characteristics. The differential peak detector circuit requires only one coil and thus provides easy tuning and minimum external components.

Applications include automotive and home FM receivers, mobile communications equipment, and television sound channels.

- **250μV TYPICAL LIMITING SENSITIVITY AT 10.7MHz**
- **125μV TYPICAL LIMITING SENSITIVITY AT 4.5MHz**
- **55dB TYPICAL AM REJECTION AT 4.5MHz**
- **SINGLE COIL TUNING**
- **DIFFERENTIAL PEAK DETECTION**
- **INTERNAL ZENER DIODE REGULATION FOR IF SECTION**

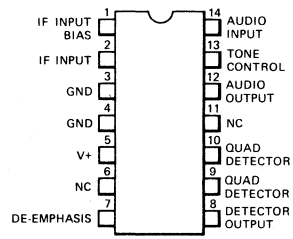
ABSOLUTE MAXIMUM RATINGS (Voltage at any terminal must not exceed V+)

Supply Voltage (Pin 5)	+18V
Input Voltage (between pins 1 and 2)	±3V
Power Dissipation (Note 1)	670mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering 60 s) μA3075DC	300°C
Molded DIP (Soldering 10 s) μA3075PC	260°C

NOTE 1: Rating applies to T_A = 70°C. Above 70°C derate at 8.3mW/°C.

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)

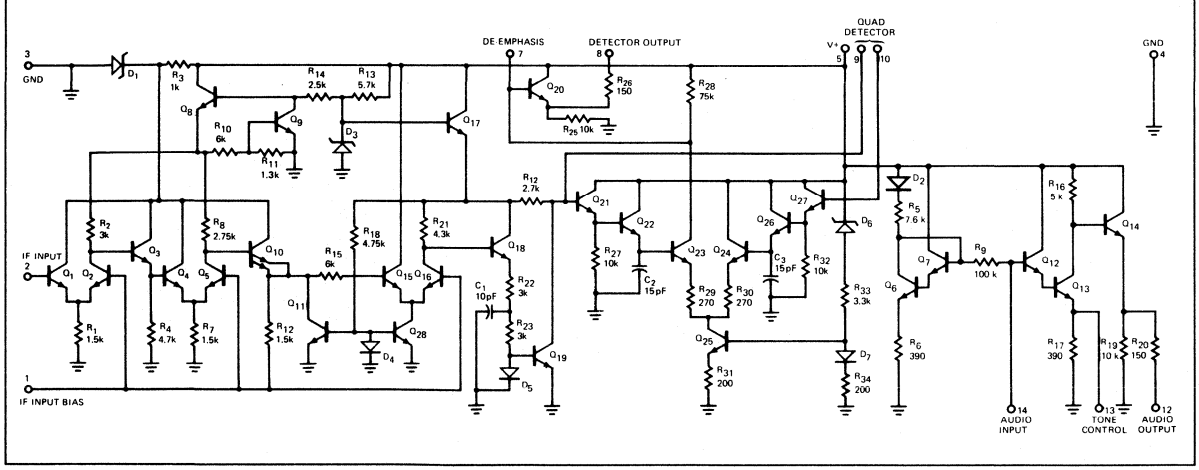
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA3075	μA3075DC
μA3075	μA3075PC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

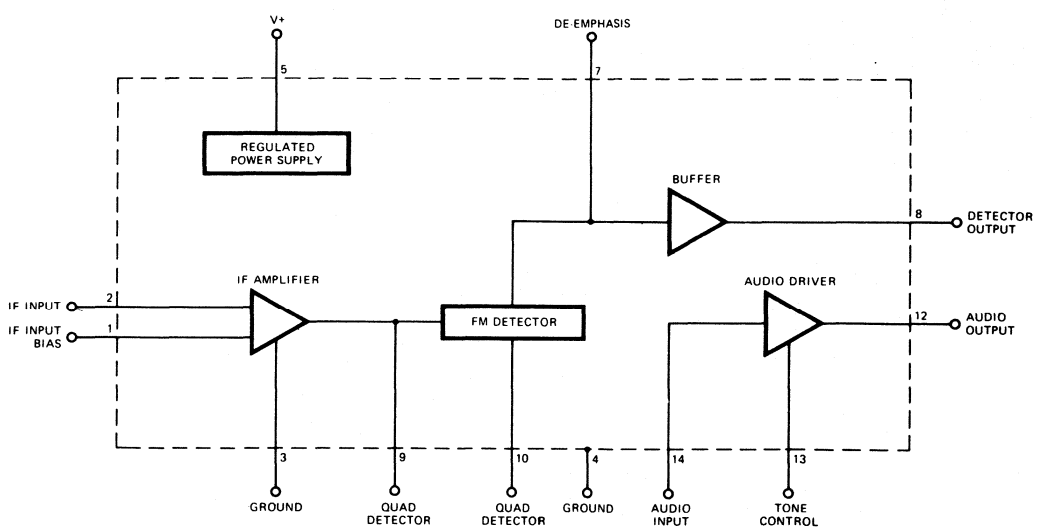
μA3075

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = +12V, unless otherwise specified)

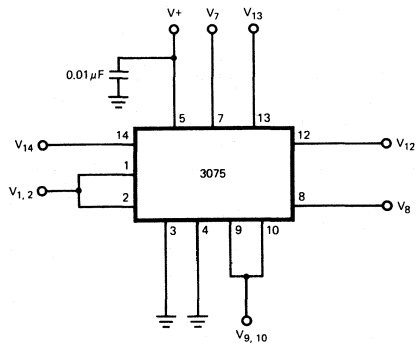
PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (Test Circuit 1)						
Supply Current I_5		V+ = 8.5V	8.0	11		mA
		V+ = 12V	12	17	28	mA
		V+ = 16V		25	35	mA
Power Dissipation					340	mW
Terminal Voltages	Pin 7			6.0		V
	Pin 8			5.5		V
	Pin 12	R_L at Pin 12 = 3.9Ω		5.0		V
DC Shift Pin 8		Change V+ from 10V to 16V	−600		+600	mV
AC CHARACTERISTICS (IF Stage f = 10.7 MHz, Test Circuit 2)						
−3dB Limiting Sensitivity				250	600	μV
Recovered Audio at Detector Output			0.5	0.7		V_{RMS}
THD at Detector Output				1.0	2.0	%
AM Rejection			40	50		dB
AC CHARACTERISTICS (IF Stage f = 4.5 MHz, Test Circuit 2)						
−3dB Limiting Sensitivity				125	400	μV
Recovered Audio at Detector Output			1.0	1.4		V_{RMS}
THD at Detector Output				1.5	2.0	%
AM Rejection			40	56		dB
AC CHARACTERISTICS (Audio Amplifier f = 1 kHz, Test Circuit 3)						
Input Resistance			40			kΩ
Voltage Gain			10	12	17	V/V
THD at Detector Output		V_{OUT} = 2 V_{RMS}		2.0	4.0	%
Maximum Available Output Swing			8.4			Vp-p

10

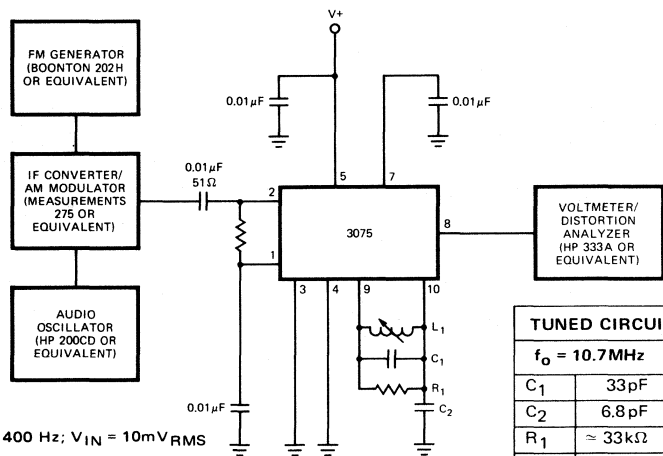
BLOCK DIAGRAM



TEST CIRCUITS



TEST CIRCUIT 1

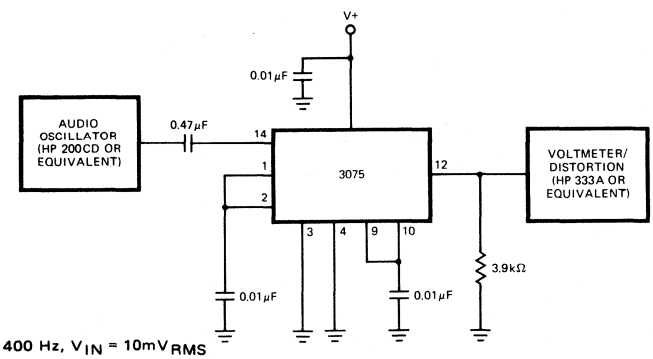


FM = 10.7 MHz ± 75 kHz @ 400 Hz; V_{IN} = 10mV$_{RMS}$

FM = 4.5MHz ± 25kHz @ 400Hz; V_{IN} = 10mV$_{RMS}$
NO CONNECTION TO PINS 6, 11, 12, 13, 14
AM modulation = 30% @ 400 Hz
Select R_1 for desired loaded Q (Q_L).

TUNED CIRCUIT COMPONENTS		
	f_o = 10.7MHz	f_o = 4.5MHz
C_1	33pF	68pF
C_2	6.8pF	12pF
R_1	≃ 33kΩ	
L_1	7μH	16μH
Q_L	55	55

TEST CIRCUIT 2



FM = 10.7 MHz ± 75 kHz @ 400 Hz, V_{IN} = 10mV$_{RMS}$
NO CONNECTION TO PINS 6, 7, 8, 11, 13

TEST CIRCUIT 3

μA3089

FM IF LIMITER DETECTOR AUDIO PREAMPLIFIER

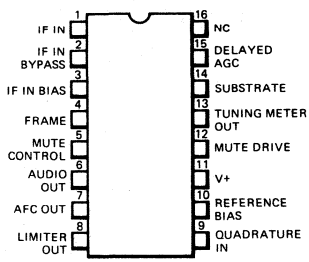
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3089 is a multifunction FM IF detector subsystem. It contains a three stage FM IF amplifier, a detector and an audio buffer amplifier. Auxiliary functions of the device include AGC and AFC for the tuner, a muting circuit and a tuning meter circuit. The circuit is fabricated using the Fairchild Planar† epitaxial process.

The 3089 is a direct replacement for the CA3089E.

- **3-STAGE FM IF AMPLIFIER PROVIDING A 12 μV (TYP) LIMITING SENSITIVITY**
- **LEVEL DETECTORS ON EACH STAGE WITH A COMMON DRIVE FOR A TUNING METER OR A STEREO THRESHOLD LOGIC CIRCUIT**
- **DELAYED AGC OUTPUT FOR THE TUNER**
- **DOUBLY BALANCED QUADRATURE DETECTOR PROVIDING LOW DISTORTION – TYPICALLY 0.1 % WITH DOUBLE TUNED CIRCUIT**
- **FLEXIBLE AFC CIRCUIT**
- **AUDIO PREAMPLIFIER PROVIDING 400 mV (TYP) OF DRIVE**
- **AUDIO MUTE (SQUELCH) CONTROL CIRCUITS**
- **INTERNAL VOLTAGE REGULATOR**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B
PACKAGE CODE P

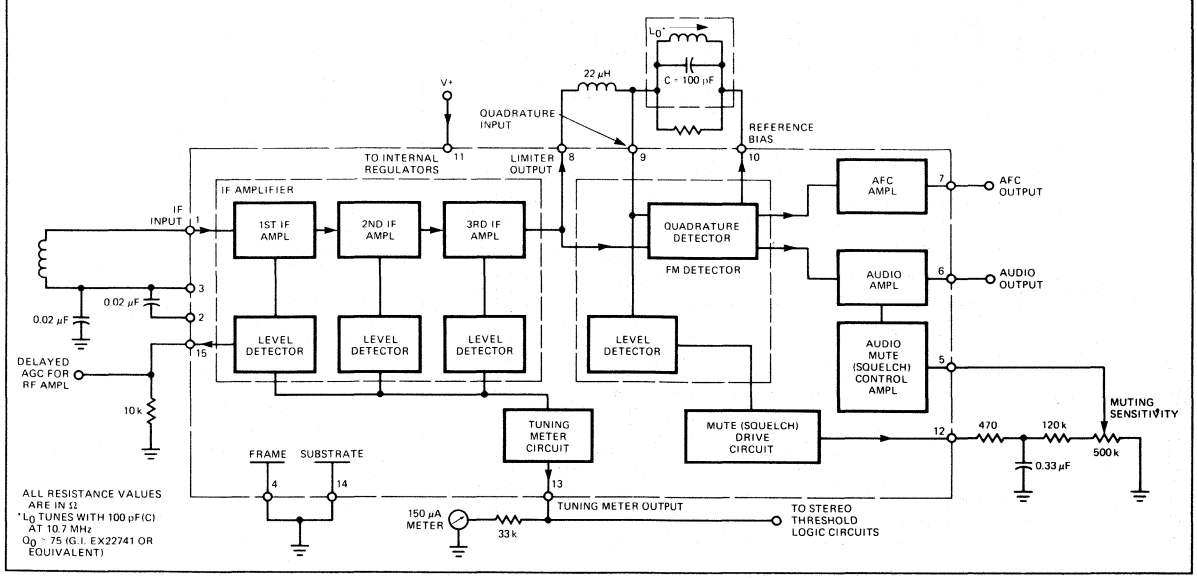


ORDER INFORMATION

TYPE	PART NO.
μA3089	μA3089PC

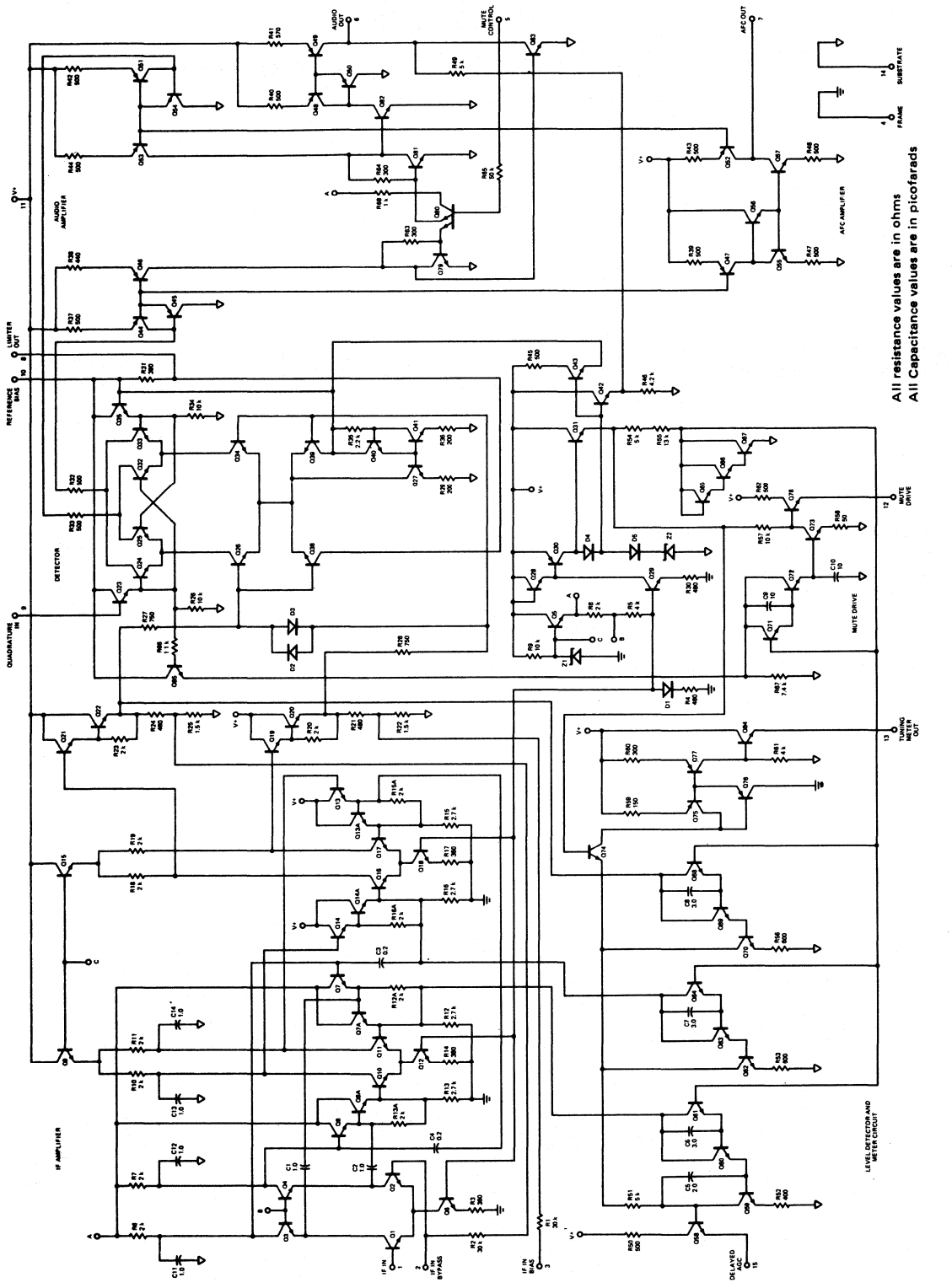
10

BLOCK DIAGRAM



†Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Between Pins 11 and 4	+16 V
Between Pins 11 and 14	+16 V
DC Current Out of Terminal 15 for AGC	2.0 mA
DC Current Out of Terminals 12 and 13	5.0 mA
Power Dissipation	
$T_A \leq 60°C$	600 mW
$60°C \leq T_A \leq 85°C$	Derate at 6.7 mW/°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 s)	260°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12 V)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (V_{IN} = 0, Non-Muted, Test Circuit 1 or 2)						
Quiescent Circuit Current	I_{11}			23	30	mA
DC Voltages at:						
IF Input	V_1		1.2	1.9	2.4	V
IF Input Bypass	V_2		1.2	1.9	2.4	V
IF Input Bias	V_3		1.2	1.9	2.4	V
Audio Output	V_6		5.0	5.6	6.0	V
Reference Bias	V_{10}		5.0	5.6	6.0	V
AC CHARACTERISTICS (f_o = 10.7 MHz, f_{MOD} = 400 Hz, Deviation = ± 75 kHz, V_{IN} = 0.1 V, Figure 1 or 2, unless otherwise stated)						
Input Limiting Voltage (−3 dB Point)		V_{IN} = Parameter		12	25	μV
AM Rejection (Lead 6)		400 Hz, 30 % MOD	45	55		dB
Recovered AF Voltage (Lead 6)			300	400	500	mV
*Total Harmonic Distortion (Lead 6)						
Single Tuned		See Fig. 1		0.5	1.0	%
Double Tuned		See Fig. 2		0.1		%
Signal Plus Noise to Noise Ratio			60	67		dB

*THD Characteristics are mainly a function of the phase characteristics of the circuit connected between pins 8, 9 and 10.

TEST CIRCUITS

TEST CIRCUIT USING A SINGLE TUNED DETECTOR COIL

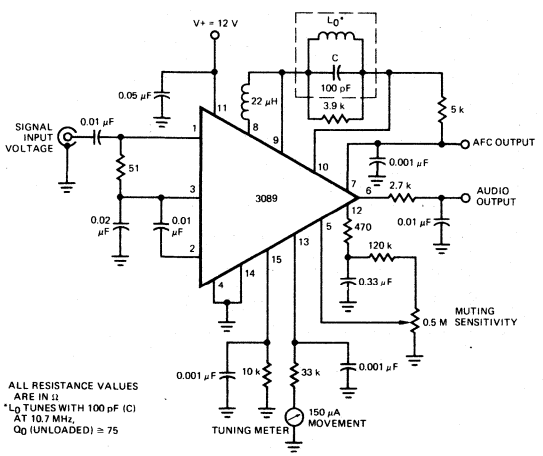


Fig. 1

TEST CIRCUIT USING A DOUBLE TUNED DETECTOR COIL

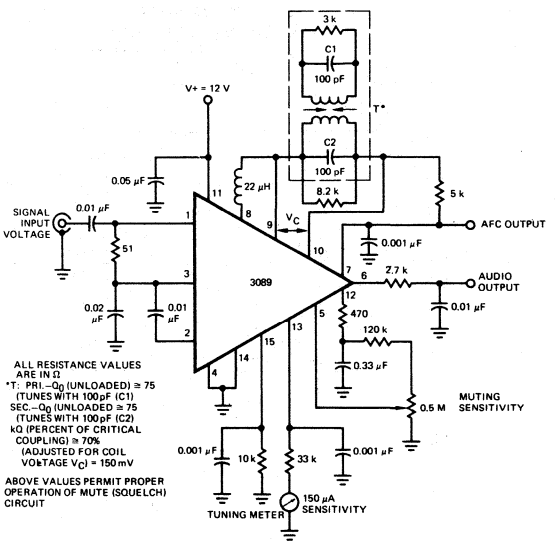
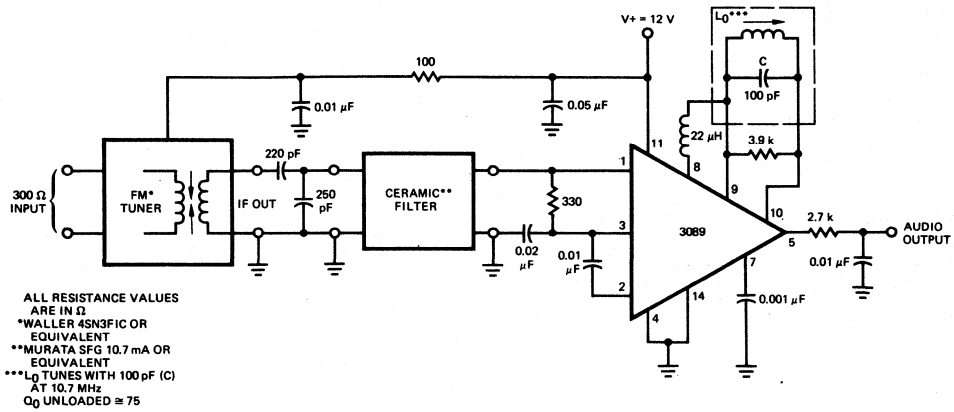


Fig. 2

TYPICAL FM SUBSYSTEM USING THE μA3089 WITH A SINGLE TUNED DETECTOR COIL



ALL RESISTANCE VALUES ARE IN Ω
*WALLER 4SN3F1C OR EQUIVALENT
**MURATA SFG 10.7 mA OR EQUIVALENT
***L_O TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O UNLOADED ≅ 75

Performance data at f_o = 98 MHz, f_{MOD} = 400 Hz, Deviation = ± 75 kHz:
–3 dB Limiting Sensitivity . . . . . 2 μV (Antenna Level)
20 dB Quieting Sensitivity . . . . . 1 μV (Antenna Level)
30 dB Quieting Sensitivity . . . . . 1.5 μV (Antenna Level)
Alternate channel rejection . . . . . 60 dB

Fig. 3

TYPICAL PERFORMANCE CURVES FOR μA3089

MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT AS A FUNCTION OF INPUT SIGNAL VOLTAGE

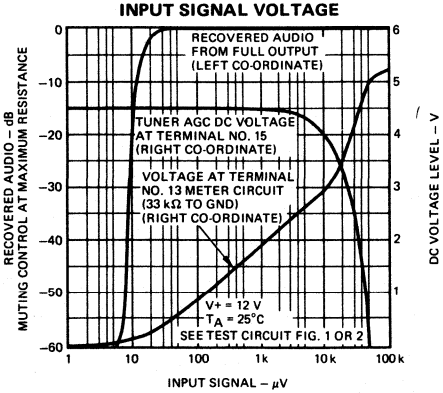


Fig. 4

AFC CHARACTERISTICS (CURRENT AT TERM. 7 AS A FUNCTION OF CHANGE IN FREQUENCY)

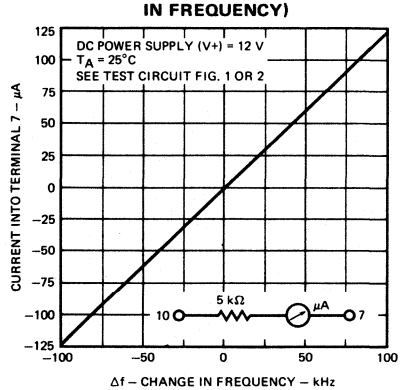


Fig. 5

TAA630S

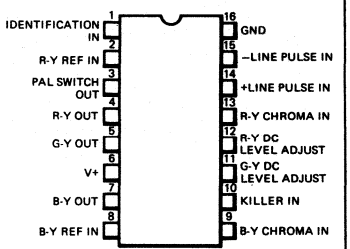
PAL CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TAA630S is a synchronous demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The TAA630S is designed for use in color television receivers operating on the Phase Alternate Line (PAL) system. This circuit consists of two synchronous demodulators, a decoding matrix, a PAL switch with internal multivibrator and a color killer switch.

- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **EMITTER FOLLOWER OUTPUTS**
- **INTERNAL PAL SWITCH**
- **INTERNAL COLOR KILLER**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

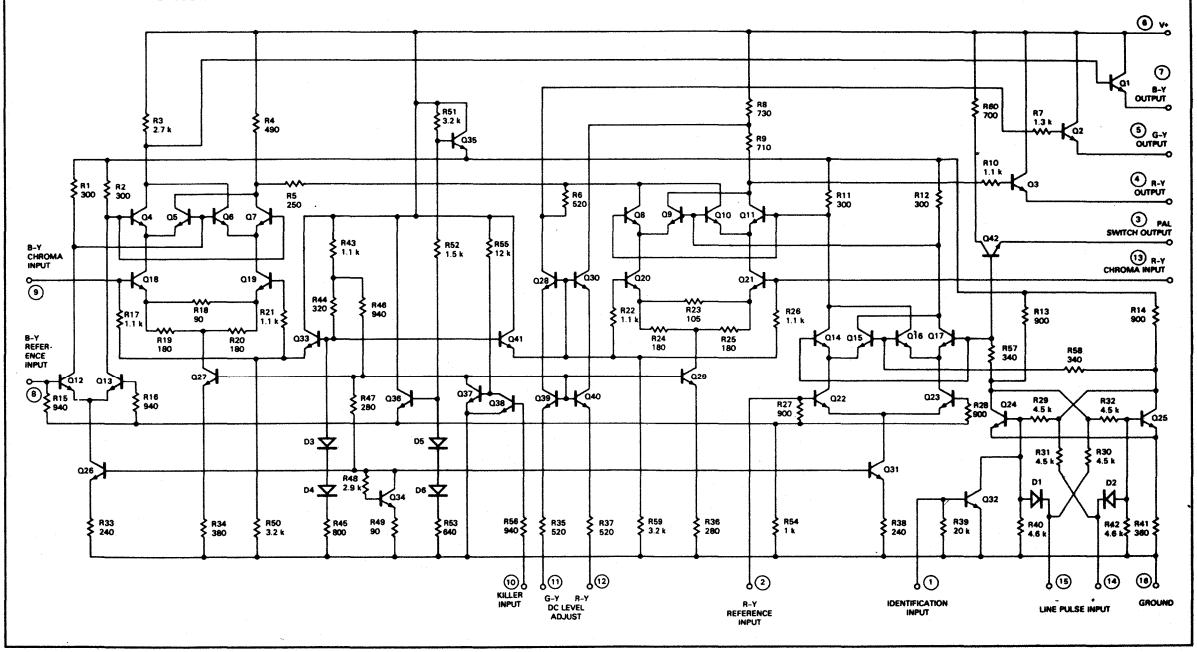
TYPE	PART NO.
630S	TAA630S
(630T)	(TAA630T)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	13.2 V
Internal Power Dissipation (Note 1)	550 mW
Color Difference Output Currents	5.0 mA
Voltage on Identification Input	5.0 V
Current Into Identification Input	1.0 mA
Operating Temperature Range	–20°C to +60°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



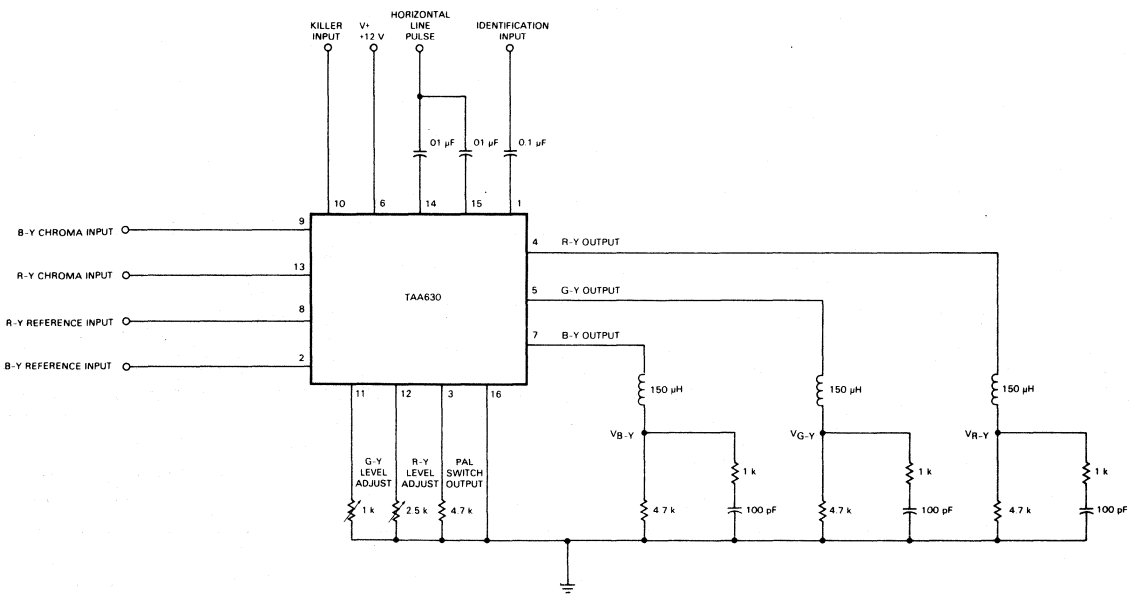
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_+ = 12 V, See Test Circuit, unless otherwise specified)

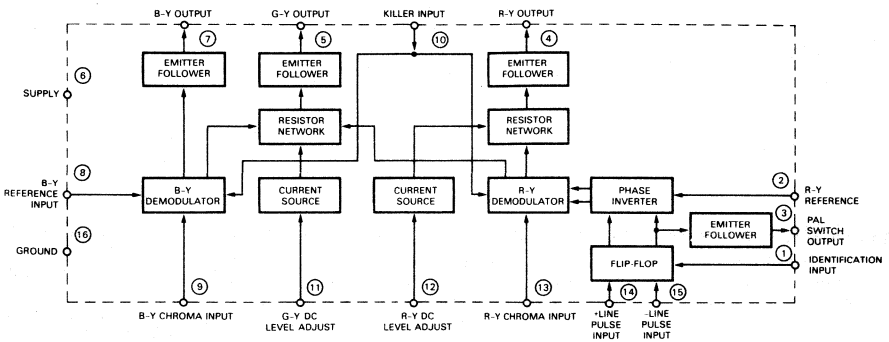
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			32		mA
Color Difference Gain	$V_9 = V_{13}$ = 50 mV p-p				
R-Y Channel	f = 4.4 MHz		7.0		
B-Y Channel/R-Y Channel			1.78		
G-Y Channel			Note 2		
Maximum Color Difference Output Voltage	Notes 3, 4				
R-Y Output (V_4 p-p)			3.2		Vp-p
B-Y Output (V_7 p-p)			4.0		Vp-p
G-Y Output (V_5 p-p)			1.8		Vp-p
Color Difference DC Output Voltage					
R-Y Output (V_4)	Note 5		Adjustable to V_7		
B-Y Output (V_7)			7.4		V
G-Y Output (V_5)	Note 5		Adjustable to V_7		
Input Resistance of Chroma Inputs (R_9, R_{13})	$V_9 = V_{13}$ = 20 mV_{RMS}	800			Ω
Input Capacitance of Chroma Inputs (C_9, C_{13})	f = 4.4 MHz (sinusoidal)			10	pF
Output Resistance at Color Difference Terminals (R_4, R_5, R_7)				100	Ω
Input Resistance of Reference Inputs (R_2, R_8)	Note 7	660		1250	Ω
Peak-to-Peak PAL Switch Output Voltage (V_3 p-p)	Note 6		2.5		Vp-p
Activation Threshold Voltage (V_1)	Identification circuit is active	0.75			V
Activation Threshold Current (I_1)		80			μA
Deactivation Threshold Voltage (V_1)	Identification circuit is inactive			0.4	V
DC Voltage at Color Killer Input (V_{10}):					
Color On		0.9			V
Color Off				0.3	V

NOTES:
1. 16 V is permissable during warm-up.
2. G-Y Output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
3. Gain is equal to 0.7 of small signal gain.
4. Reference input (V_2 p-p and V_8 p-p) range is 0.5 V to 2.0 V.
5. To be adjusted with a variable voltage (V ≤ 1.2 V) or with resistors connected between pin 11 and ground for G-Y and pin 12 and ground for R-Y.
6. f_{out} = 0.5 x Line Pulse Frequency, $V_{14} = V_{15}$ = −2.5 V to −5.0 V (Peak), PAL identification signal required, V_1 = 2.0 to 6.0 V p/p.
7. $V_2 = V_8$ = 400 mV RMS, f = 4.4 MHz (sinusoidal).

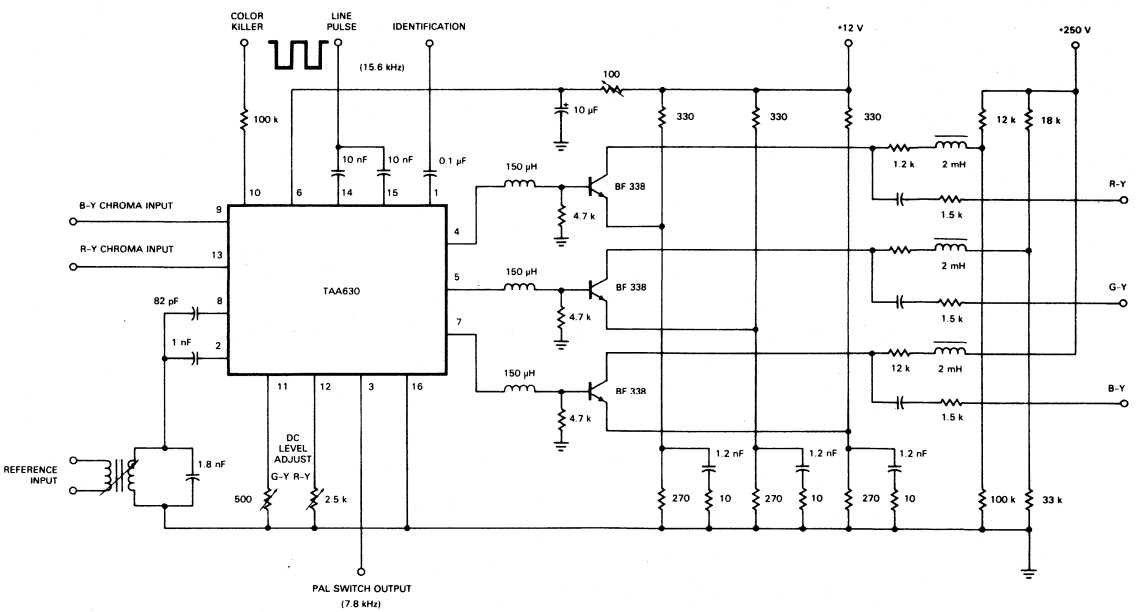
TEST CIRCUIT



BLOCK DIAGRAM



TYPICAL APPLICATION



TBA510

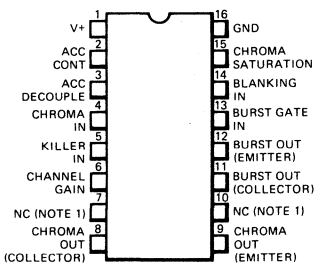
CHROMA PROCESSING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The TBA510 is a monolithic integrated circuit designed to perform the chrominance amplifier function for television receivers. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. A dc chroma gain control, which can be ganged to the receiver contrast control, is provided. Also incorporated is a variable gain automatic color control (ACC) stage, chroma blanking, burst gating, burst output stage. Two single output transistors provide burst and chroma output.

- **DC CHROMA CONTROL**
- **PAL DELAY LINE DRIVER**
- **ACC AMPLIFIER**
- **COLOR KILLER**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

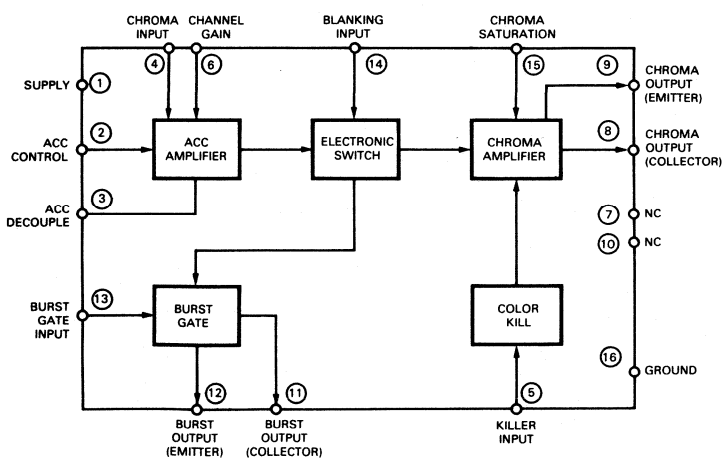
TYPE	PART NO.
510	TBA510
(510Q)	(TBA510Q)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

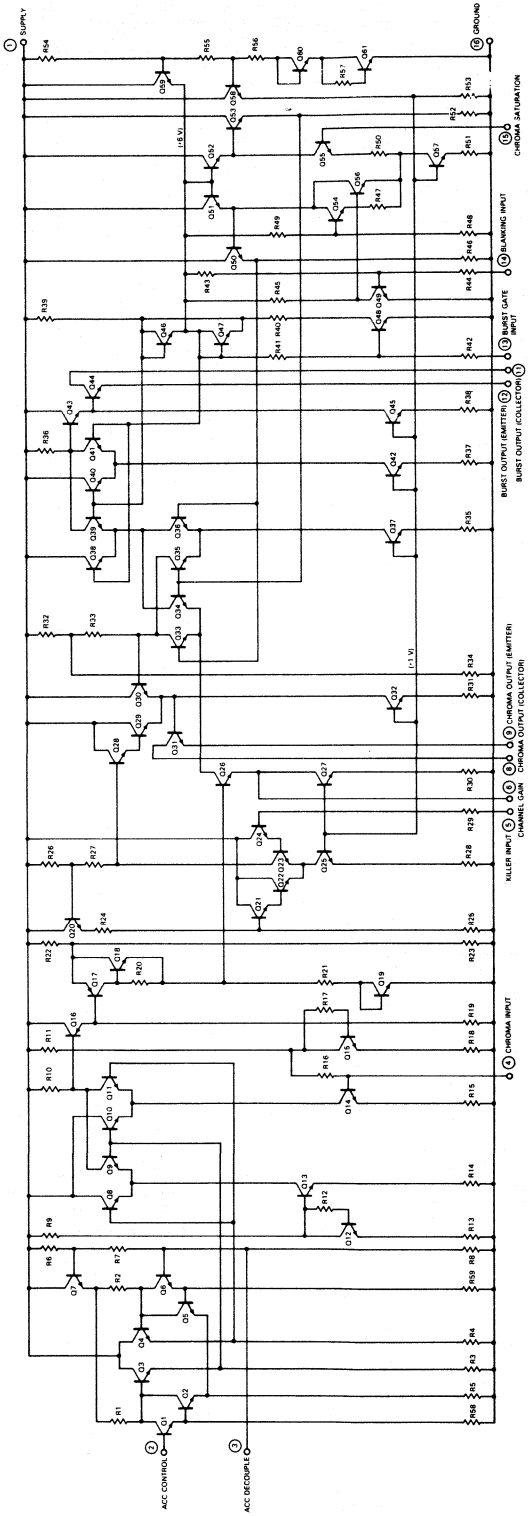
Supply Voltage	13.2 V
Internal Power Dissipation	550 mW
Current into Chroma Delay Line Driver (Collector)	20 mA
Current into Color Burst Output (Collector)	20 mA
Current out of Color Burst Output (Emitter)	20 mA
Current out of Chroma Delay Line Driver (Emitter)	20 mA
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT

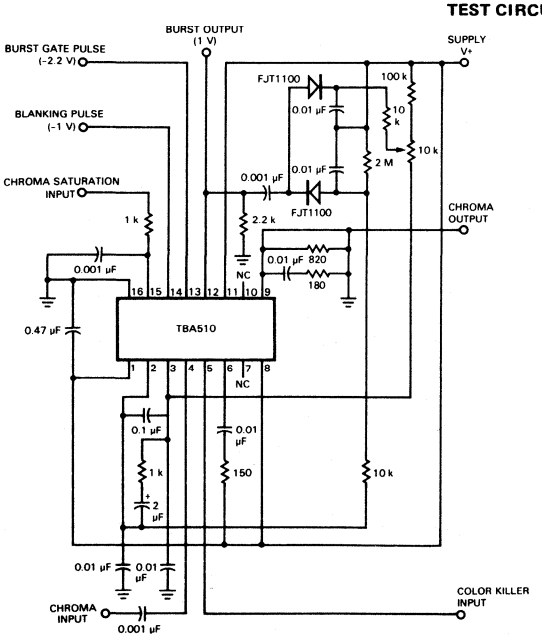


○ = Pin Numbers

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_+ = 12 V, See Test Circuit, unless otherwise specified)

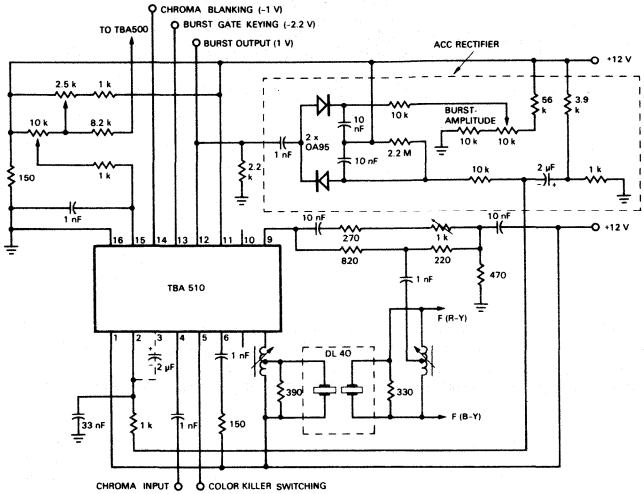
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 4)					
Peak-to-Peak Signal at Chroma Input (V_{4p-p})		15	150	300	mV_{p-p}
Input Impedance of Chroma Signal (Z_4)			3.0		kΩ
Burst Output (pin 11 and 12)					
DC Voltage at Color Burst Output (V_{12})			8.0		V
Peak-to-Peak Signal at Color Burst Output (V_{12p-p})	(Note 2)		1.0		V_{p-p}
Collector Current of Color Burst Output (I_{11})			4.0		mA
Chroma Output (pin 8 and 9)					
DC Voltage at Chroma Output (V_9)			7.0		V
Peak-to-Peak Signal at Chroma Output (V_{9p-p})	(Note 3)		1.0		V_{p-p}
Range of Contrast and Saturation Control		−30		+6.0	dB
Collector Current at Chroma Output (I_8)			5.0		mA
ACC Input (pin 2)					
ACC Input Voltage (V_2) for Maximum Gain (Note 4)			2.5		V
Input Impedance of ACC Control (Z_2)		50			kΩ
Chroma Saturation Control Input (pin 15)					
Control Voltage Range (V_{15}) (Note 4)		1.5		4.5	V
Input Impedance (Z_{15})		50			kΩ
Chroma Blanking Input (pin 14)					
Switching Level Range (V_{14})		−5.0		−1.0	V
Input Impedance (Z_{14})			2.0		kΩ
Burst Gate Input (pin 13)					
Switching Level Range (V_{13})		−5.0		−2.2	V
Input Impedance (Z_{13})			4.0		kΩ
Color Killer Input (pin 5)					
Input Voltage (V_5) for:					
Color on		2.5		4.0	V
Color off		0		1.8	V
Signal Suppression at Color Off		50			dB
Input Impedance (Z_5)		100			kΩ

TEST CIRCUIT



NOTES:
1. NC — no connection (not to be used as a tie point).
2. Color burst output kept constant by ACC circuit.
3. Chroma output (emitter) at nominal saturation and maximum contrast.
4. Gain control characteristic positive.

APPLICATION INFORMATION



The function is quoted against the corresponding pin number.

1. **Positive 12 V supply**
2. **A.C.C. control potential input**
   The potential required at pin 2 for maximum gain is about 2.5 V; gain reduction occurs when this potential is reduced; Zin > 50 kΩ.
3. **A.C.C. bias ripple compensation**
   The internal A.C.C. circuit consists of differential pair. The "cold" side is established internally at +2.5 V and is brought out on pin 3. This enables a decoupling capacitor to be connected and returned to the point which secures the lowest supply line ripple amplitude injection into the A.C.C. loop.
4. **Chroma signal input**
   The allowable input voltage range is from 15 mV to 300 mV peak-to-peak with a color bar signal. The input impedance is greater than 2 kΩ.
5. **Color killer switching input**
   The input impedance is greater than 50 kΩ. Color "on" 2.5 to 4 V; color "off" 0 to 1.8 V. The chroma signal suppression when killed is greater than 50 dB.
6. **Emitter decoupling network**
   The series network decouples an emitter of an amplifier stage in the chroma channel. The value of resistance influences the chroma channel gain.
7. **No connection**
   Not to be used as a tie point. It is recommended that pins 7 and 10 be grounded.
8. **Delay line driver (collector)**
   Supplies the chroma signal drive to the delay line driver transformer, the "cold" end of which is connected to +12 V. The maximum permitted voltage excursion at this pin is 20 V peak. Maximum current, 12 mA peak.
9. **Delay line driver (emitter)**
   Supplies the chroma to the network which provides the non-delayed signal to the delay line output transformer. The emitter is established internally at a potential of 6.8 ± 1.0 V and the external network, which must incorporate a resistive dc path to ground, must not demand more than 20 mA peak current.
10. **No connection**
    Not to be used as a tie point. (See pin 7.)
11. **Color burst output (collector)**
    If a low impedance color burst is required (from the emitter of the color burst output, pin 12) pin 11 will be connected to the +12 V supply. The maximum voltage and current excursions permitted on pin 11 are 20 V peak and 20 mA peak.
12. **Color burst output (emitter)**
    An external load resistor of 2.0 kΩ is required connected to ground and dc potential of 7.7 ± 1.0 V is established on pin 12 due to the internal circuitry. The burst output voltage is 1.0 V peak-to-peak.
13. **Burst gate gating pulse**
    The horizontal flyback pulse can be used as a source of gating waveform. A negative-going pulse of not greater than 5.0 V amplitude is necessary, the input impedance is 4.0 kΩ and the switching level is between −2.2 V and −5.0 V.
14. **Chroma blanking pulse input**
    A negative going horizontal flyback pulse can be used here. Its amplitude should not exceed −5.0 V. The input impedance at this pin is 2.0 kΩ and the switching level is about −1.0 V. During scan time, the dc voltage on this pin should not be negative.
15. **Chroma saturation control**
    The dc control voltage range required is from 1.5 to 4.5 V (highest gain at 4.5 V). The input impedance is > 50 kΩ and a control range from +6.0 to −30 dB is given.
16. **Ground**

TBA520

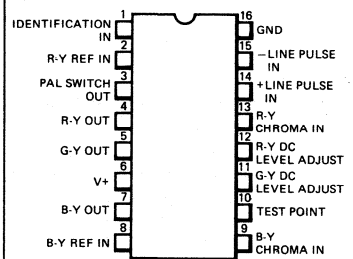
PAL TV CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA520 is a synchronous demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The TBA520 is designed for use in color television receivers, operating on the Phase Alternate Line (PAL) system. This circuit consists of two synchronous demodulators, a decoding matrix and a PAL switch with internal multivibrator.

- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **INTERNAL PAL SWITCH**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

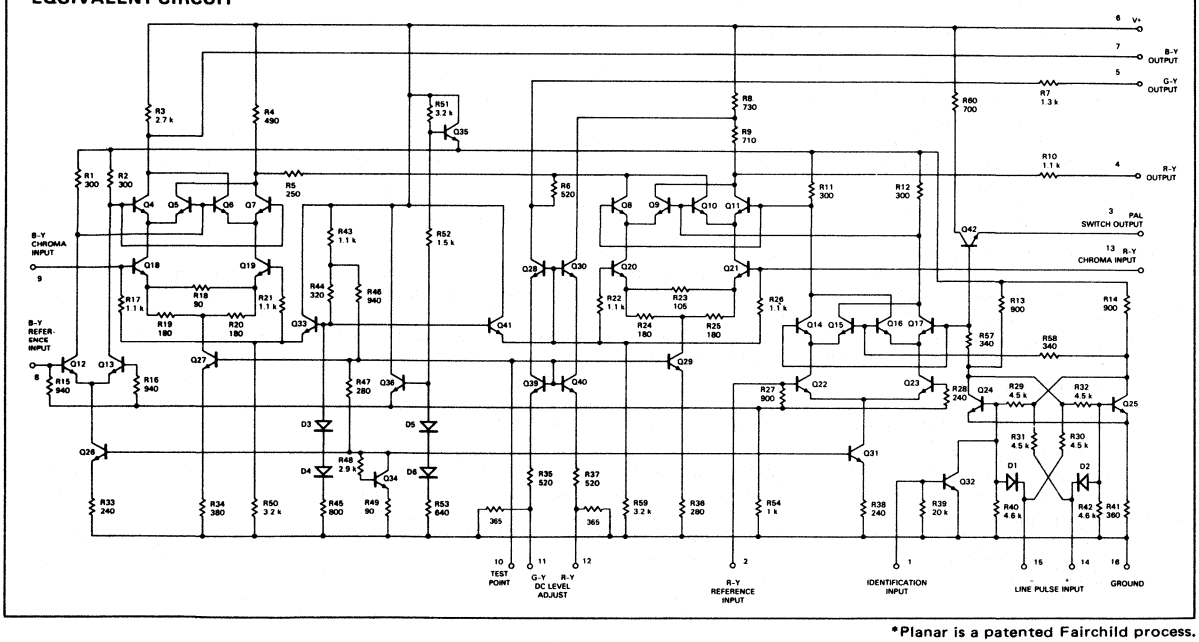
TYPE	PART NO.
520	TBA520
(520 Q)	(TBA520 Q)†

†Not recommended for new design.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Internal Power Dissipation	550 mW
Voltage on Identification Input	5.0 V
Current into Identification Input	1.0 mA
Operating Temperature Range	–20°C to +60°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

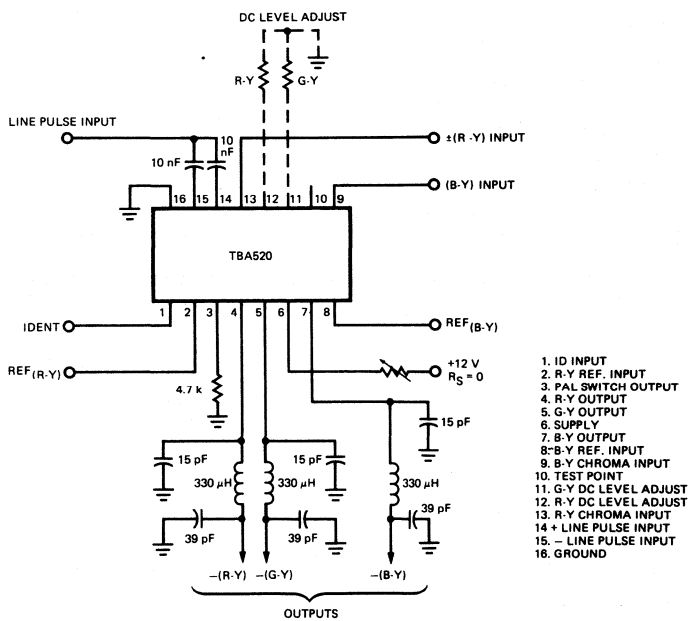
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_+ = 12 V, See Test Circuit, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			32		mA
Color Difference Gain					
R-Y Channel	$V_9 = V_{13}$ = 50 mVpk-pk, f = 4.4 MHz		7.0		V/V
B-Y Channel			12.5		V/V
G-Y Channel			(Note 1)		
Maximum Color Difference Output Voltage (Notes 2,3)					
R-Y Output ($V_{4\ pk-pk}$)	(Notes 2,3)		3.2		V_{pk-pk}
B-Y Output ($V_{7\ pk-pk}$)			4.0		V_{pk-pk}
G-Y Output ($V_{5\ pk-pk}$)			1.8		V_{pk-pk}
Color Difference dc Output Voltage					
R-Y Output (V_4)			7.9		V
B-Y Output (V_7)			7.9		V
G-Y Output (V_5)			7.9		V
Input Resistance of Chroma Inputs (R9, R13)	$V_9 = V_{13}$ = 20 mVrms (Sinusoidal)	800			Ω
Input Capacitance of Chroma Inputs (C9, C13)	f = 4.4 MHz			10	pF
Output Resistance at Color Difference Terminals (R4, R5, R7)			2.7		kΩ
Input Resistance of Reference Inputs (R2, R8)			1.0		kΩ
Peak-to-Peak PAL Switch Output Voltage ($V_{3\ pk-pk}$)	(Note 4)		2.5		V_{pk-pk}
Activation Threshold Voltage (V_1)	Identification Circuit is Active	0.75			V
Activation Threshold Current (I_1)		80			μA
Deactivation Threshold Voltage (V_1)	Identification Circuit is Inactive			0.4	V

NOTES:
1. G-Y output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
2. Gain is equal to 0.7 of small signal gain.
3. Reference input (V_{2pk-pk} and V_{8pk-pk}) range is 0.5 V to 2.0 V.
4. f_{out} = 0.5 x line pulse frequency; $V_{14} = V_{15}$ = −3.0 V to −4.5 V (peak).

10

TEST CIRCUIT



APPLICATION INFORMATION

The function is quoted against the corresponding pin numbers.

1. **Identification bias**
   The input current required to stop the flip-flop, "Ident on": $I_{on} \geq 80\,\mu A$. For "Ident off": $V_{off} = -5.0$ to $+0.4$ V.
2. **R-Y subcarrier reference input**
   An 1.0 V peak-to-peak signal is required via a dc blocking capacitor. Under no circumstances should this signal be less than 0.5 V peak-to-peak. The input resistance at this pin is typically 1 kΩ.
3. **PAL square wave output**
   The amplitude is 2.5 V peak-to-peak from an emitter follower.
4. **R-Y signal output** (G-Y at pin 5 and B-Y at pin 7)
   No external dc load needed except that direct connection must be made via the low pass filter to the R G B matrix of the TBA530.

   The signals produced are in the following ratios:

   $$V_{B-Y} = 1.3\ V_{R-Y}$$
   (a) $$V_{G-Y} = 0.76\ V_{R-Y}$$
   (b) $$V_{G-Y} = 0.26\ V_{R-Y}$$

   Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix. Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

   The dc levels should each be adjusted, starting with the (B-Y) to +7.5 V at nominal supply voltage.

   The maximum peak-to-peak voltages for the condition $m \geq 0.7$ (m = ratio of minimum to maximum differential gains) are:

   $$V_{R-Y(pk-pk)} = 3.2\ V$$
   $$V_{G-Y(pk-pk)} = 1.8\ V$$
   $$V_{B-Y(pk-pk)} = 4.0\ V$$

   The output impedance for each signal is 2.7 kΩ.

   The drifts in dc levels of the color difference output signals for a change in ambient temperature of 40°C (after equilibrium is reached from switch-on) are typically:

Absolute shift	−50 to +50 mV
V_{R-Y} relative to V_{B-Y}	−20 to +20 mV
V_{G-Y} realtive to V_{B-Y}	−20 to +20 mV
V_{R-Y} relative to V_{G-Y}	−20 to +20 mV

   The changes in dc level with supply voltage are approximately linear and track together.

   The −3.0 dB bandwidth of the color difference signals is 1.5 MHz.
5. **G-Y signal output** (see pin 4)
6. **Positive supply**
   Also dc level setting for B-Y output (pin 7). The maximum allowable voltage on this pin is 13.2 V. The minimum supply voltage to insure setting the B-Y output dc level correctly (+7.5 V) is 11.6 V (in such case R_S would be set to zero).
7. **B-Y signal output** (see pin 4)
8. **B-Y subcarrier reference input**
   The requirements here are identical with those for pin 2.
9. **Chrominance B-Y input signal**
   An input signal up to 360 mV peak-to-peak (color bars) is advisable. For driving the TBA530 an input signal of 160 mV is required.
10. **Internally connected**
    No external connection should be made.
11. **DC level setting for G-Y output signal** (circuit diagram on page 2).
12. **DC level setting for R-Y output** (see circuit diagram on page 2).
13. **Chrominance R-Y input signal**
    An input signal up to 500 mV peak-to-peak (color bars) is advisable. The input impedance is the same as for pin 9.
14. **Line pulse input** (flip-flop synchronizing)
    A 4.0 V peak negative going line flyback pulse should be applied via separate 10 nF capacitors to pins 14 and 15. Pulse amplitude to lie between 3.0 V and 4.5 V peak-to-peak.
15. **Line pulse input** (see pin 14).
16. **Ground.**

TBA530

RGB MATRIX PREAMPLIFIER

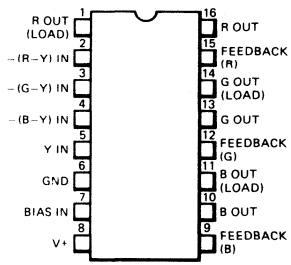
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA530 is an integrated circuit for color T.V. receivers incorporating a matrix preamplifier for RGB cathode or grid drive of the picture tube without clamping circuits. The chip layout has been designed to insure tight thermal coupling between all the transistors in each channel to minimize and equalize thermal drifts between channels.

This device is constructed on a single silicon chip using the Fairchild Planar* epitaxial process and is designed to be driven from the TBA520 or TBA990 synchronous demodulators.

- **THREE MATCHED CHANNELS FOR MATRIXING**
- **MATCHED FREQUENCY RESPONSE**
- **MATCHED TEMPERATURE STABILITY**
- **DIRECT DRIVE OF RGB OUTPUT TRANSISTORS WHEN USING TBA520 OR TBA990**
- **RGB DRIVE WITH OR WITHOUT CLAMPING**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
530	TBA530
530Q	TBA530Q†

†Not Recommended for New Designs.

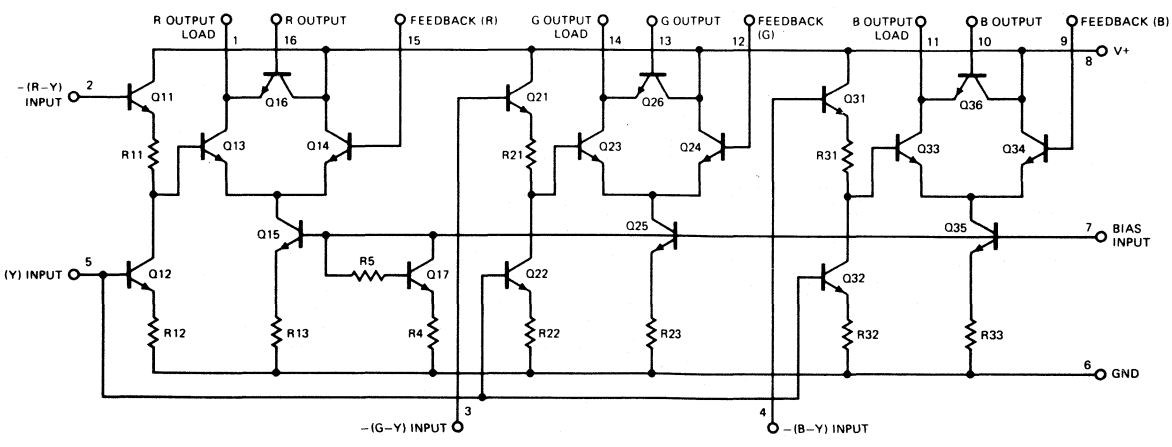
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Supply Currents (I_1, I_{11}, I_{14})	10 mA
Supply Currents (I_{10}, I_{13}, I_{16}) (Note 1)	50 mA
Total Power Dissipation (Note 1)	400 mW
Storage Temperature	−55°C to +125°C
Operating Ambient Temperature	−20°C to +60°C
Lead Temperature (Soldering 10 seconds)	260°C

NOTE:

1. In case of breakdown in the output transistors, 50 mA MAX is permitted from pins 10, 13 and 16 each to pin 8. P_D is then 500 mW MAX.

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_8 = 12 V, see application circuit)

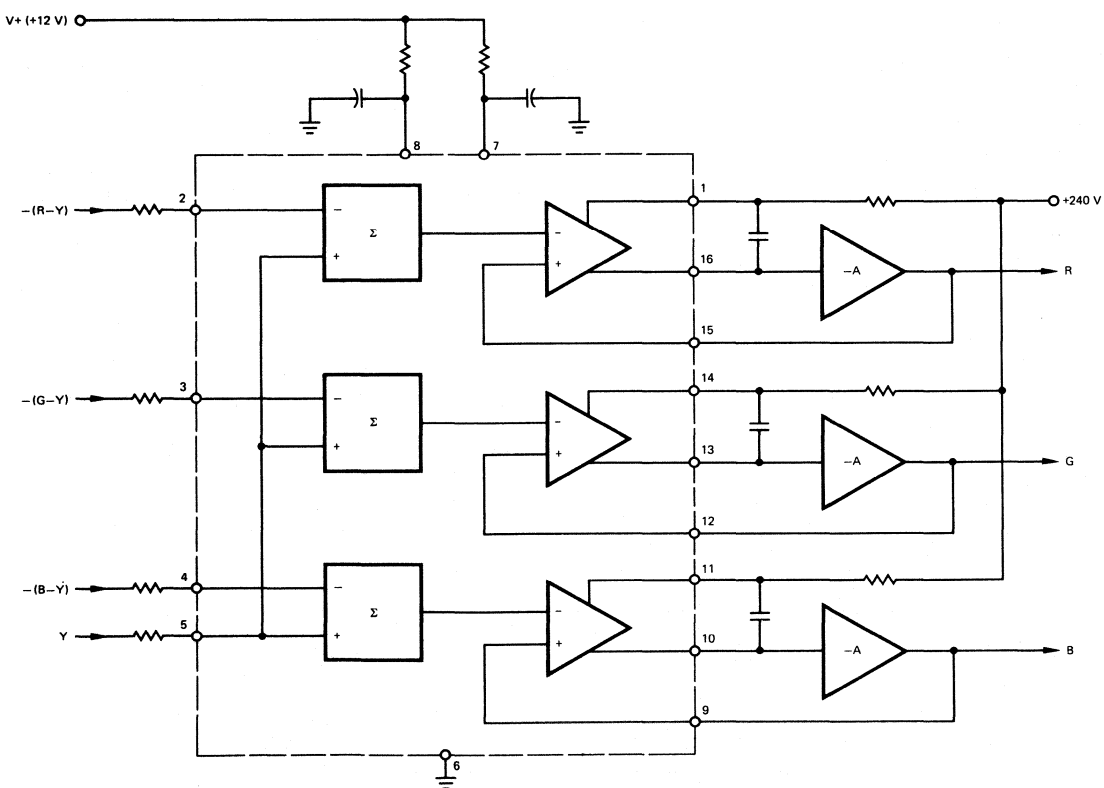
Black level settings: $V_{R-Y} = V_{G-Y} = V_{B-Y}$ = 7.5 V, V_Y = 1.5 V

PARAMETER	MIN	TYP	MAX	UNITS
Supply Current I		30		mA
Required Input Signals				
R-Y (V_2)		1.4		V_{pk-pk}
G-Y (V_3)		0.82		V_{pk-pk}
B-Y (V_4)		1.78		V_{pk-pk}
Y (V_5)		1.0		V_{pk-pk}
Gain of Channels (B-Y; G-Y, R-Y) at f = 0.5 MHz (Note 2)		100		
Gain Ratio Luminance to Each Color Amplifier		1.0		
DC Output Voltage, Each Channel		165		V
Input Resistance (Color) f = 1 kHz (R2, R3, R4)		60		kΩ
Input Resistance (Luminance) f = 1 kHz (R5)		20		kΩ
Input Capacitance (Color) f = 1 kHz (C2, C3, C4)		3.0		pF
Input Capacitance (Luminance) f = 1 kHz (C5)		10		pF
Bandwidth, Each Channel 3 dB		6.0		MHz

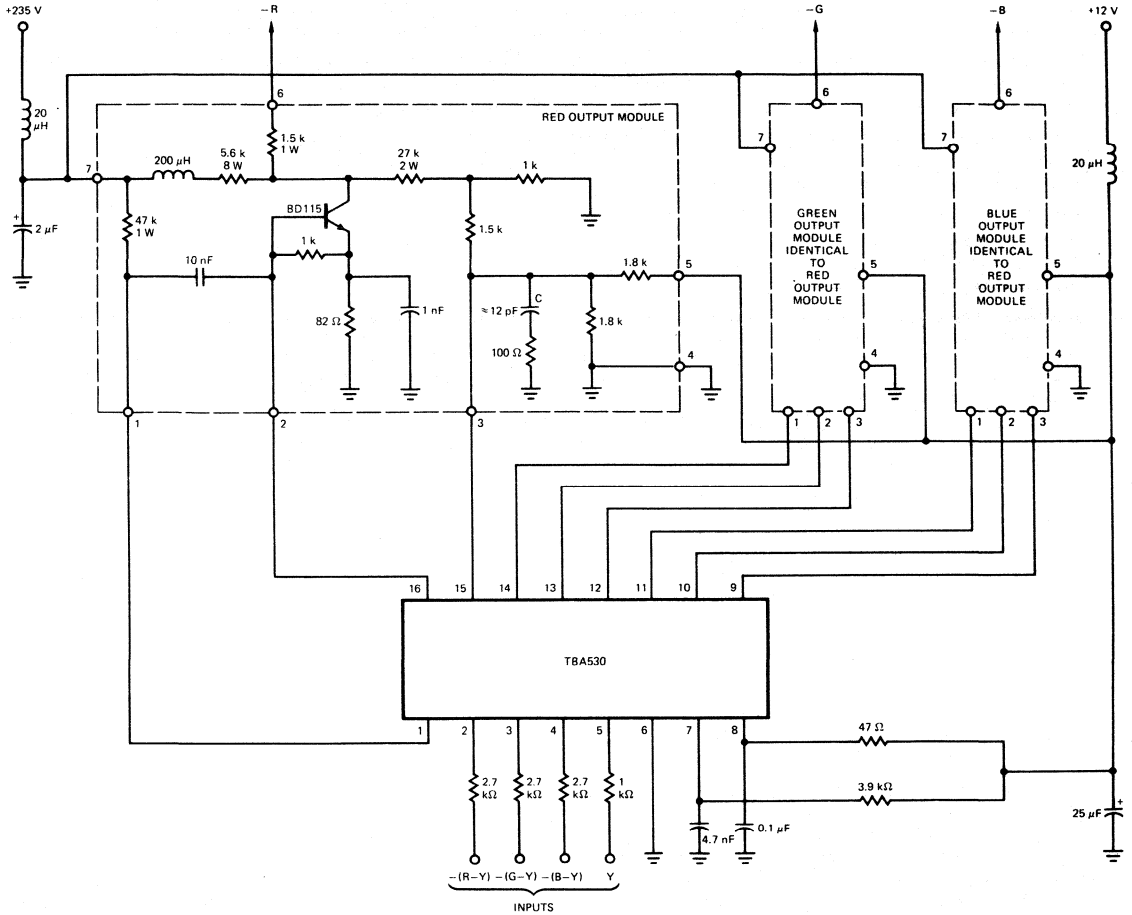
NOTE:

2. Gain is defined as the voltage ratio between the input signals at pins 2, 3, 4 and the output signals at the collectors of the output transistors.

BLOCK DIAGRAM



APPLICATION CIRCUIT



NOTE:
When using a socket for the IC, shut off the power supplies before inserting or changing devices.

APPLICATIONS INFORMATION

The function is quoted against the corresponding pin number:

1. **Output load resistor, red signal** (pin 11, blue signal; pin 14, green signal). Resistors (47 kΩ, 1 W) connected to +235 V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by an internal Zener type junction and the dc feedback and is approximately +8 V. The maximum current which can be allowed at each of these pins is 10 mA.
2. **R-Y input signal** (pin 3: G-Y input signal, pin 4: B-Y input signal). This signal is fed via a low-pass filter from the TBA520 or TBA990 demodulator having a dc level of +7.5 V and an amplitude of 1.40 $V_{pk\text{-}pk}$.
3. **G-Y input signal** The dc black level of this signal is +7.5 V and its amplitude is 0.82 $V_{pk\text{-}pk}$ (pin 2).
4. **B-Y input signal** The dc black level of this signal is +7.5 V and its amplitude is 1.78 $V_{pk\text{-}pk}$ (pin 2).
5. **Luminance signal input** The dc level on this pin for picture black is +1.5 V. The required signal amplitude is 1.0 V black-to-white with negative-going sync (or blanking) for cathode drive as shown.
6. **Ground**
7. **Current feed point** — A current of approximately 2.5 mA is required at this pin, fed via a 3.9 kΩ resistor from +12 V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7 nF is necessary.
8. **Positive 12 V supply** — Maximum supply voltage permitted, 13.2 V.
9. **Blue channel feedback** (pin 12, green channel; pin 15, red channel). The dc working points and gains of both the output stages and the IC amplifier stages are stabilized by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by correctly setting the dc level of the color difference signals produced by the demodulator IC. The gains of the RGB output stages are adjusted to give the correct white temperature setting on the picture tube by adjusting the 1.5 kΩ resistor in the feedback paths. (See applications circuit)
10. **Blue signal output** (green and red signal outputs on pins 13 and 16). These pins internally connected with pins 11, 14 and 1 respectively via Zener type junctions to give a dc level shift appropriate for driving the output transistor bases directly. To by-pass the Zener junctions at high frequencies three 10 nF capacitors are required.
11. **Output load resistor,** blue channel (see pin 1).
12. **Green channel feedback** (see pin 9).
13. **Green channel output** (see pin 10).
14. **Output load resistor,** green channel (see pin 1).
15. **Red channel feedback** (see pin 9).
16. **Red signal output** (see pin 10).

BRIEF PERFORMANCE DETAILS AND COMMENTS

1. Spread of the ratio of voltage gains for color difference and luminance signal inputs 0.9 to 1.1.
2. Very careful attention to ground paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon high frequency response of inevitable differences, e.g., the absence of a potentiometer in one of the stages, the compensating capacitors (C) may be appropriately selected for any given board layout.
3. The signal black level at the collectors of the RGB output stages depends upon the +12 V supply, the dc level of the color difference signals from the demodulator IC and the black level potential of the luminance signal applied to the TBA530 matrix IC. The dc levels of the signals produced and handled by the ICs are designed to have approximately proportional tracking with the 12 V supply potential.

$$\text{i.e., } \frac{\Delta V \text{ (dc level, signal)}}{\Delta V+} \approx \frac{V\text{nom (dc level, signal)}}{12}$$

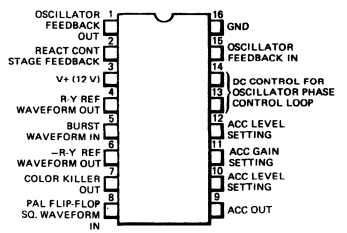
To ensure that changes in picture black level due to variations on the 12 V supply to the ICs occur in a predictable way, all the ICs should be operated from a common supply line. This is specially important for the TBA520 or TBA990 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12 V supply should have a stability of not worse than ± 3% due to operational variations, and preferably be tracked with the screen-grid supply of the picture tube.

TBA540
REFERENCE COMBINATION
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA540 is an integrated reference oscillator circuit for PAL color television receivers. It incorporates an automatic phase and amplitude controlled crystal oscillator. The half-line frequency synchronous demodulator circuit compares the phases and amplitude of the swinging burst ripple with the PAL flip-flop waveform, and generates appropriate ACC, color killer and identification signals. The use of synchronous demodulation for these functions permits high noise immunity. This circuit is constructed on a single silicon chip using the Fairchild Planar* process.

- **COMPLETE SUBCARRIER REGENERATOR**
- **ACC AMPLIFIER**
- **COLOR KILLER**
- **AUTOMATIC PHASE CONTROL LOOP**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
540	TBA540
(540Q)	(TBA540Q)†

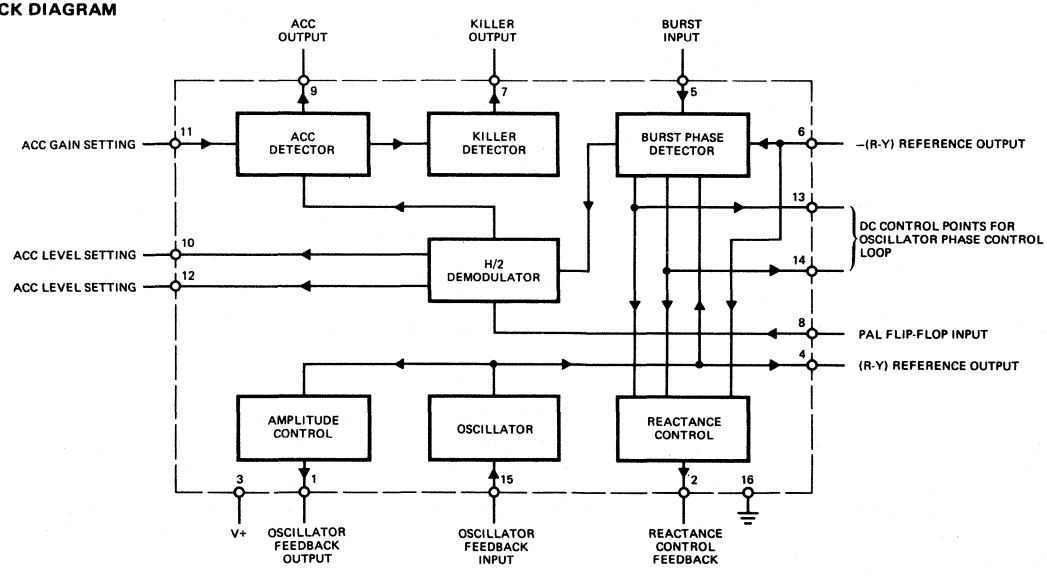
†Not recommended for new designs.

10

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Total Power Dissipation at T_A = 50°C	680 mW
Storage Temperature	−55 to +125°C
Operating Ambient Temperature	−20 to +60°C
Lead Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM

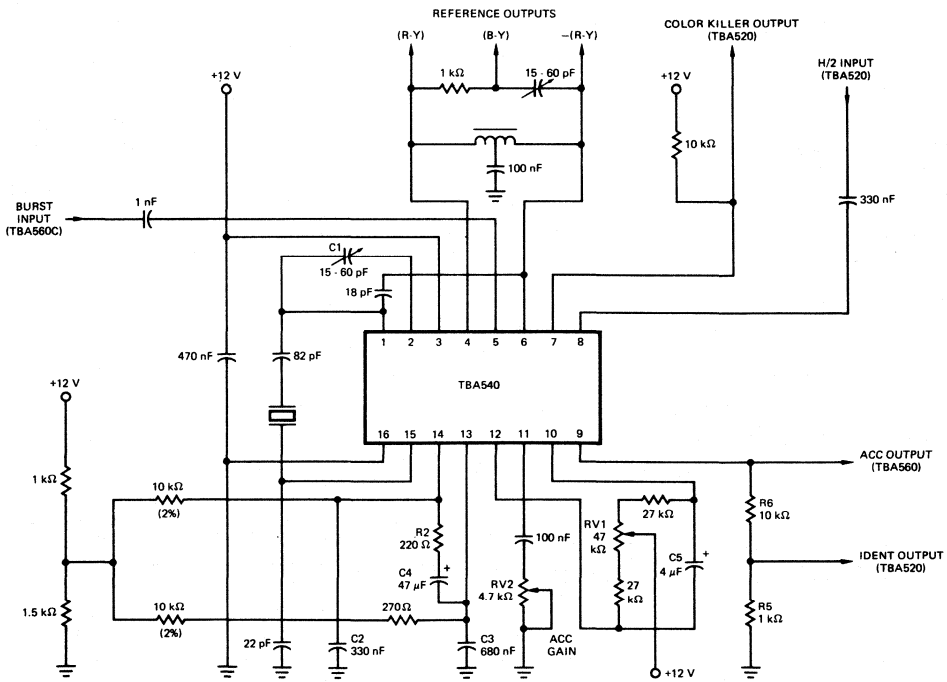


*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS [V_{3-16} = 12 V; T_A = 25°C; V_{5-16} = 1.0 V_{p-p} (burst signal input); V_{8-16} = 2.5 V_{p-p} (PAL Square wave input). Measured in circuit shown in Application Information.]

PARAMETER		MIN	TYP	MAX	UNITS
Output Signals					
R-Y Reference Signal Output	V_{4-16}		1.5		V_{p-p}
Color Killer Output					
Color On	V_{7-16}		12		V
Color Off	V_{7-16}			250	mV
ACC Output Signal Range					
at Correct Phase of PAL Switch	V_{9-16}		+4.0 to +0.2		V
at Incorrect Phase of PAL Switch	V_{9-16}		+4.0 to +11.0		V
Oscillator Section (Amplifier)					
Input Resistance	R_{15}		3.5		kΩ
Input Capacitance	C_{15}		5.0		pF
Voltage Gain	V_{15}/V_1		4.7		V/V
Reactance Control Section					
Voltage Gain with Leads 13 and 14 Interconnected	V_{15}/V_2		1.3		V/V
Rate of Change of Gain V_{15}/V_2 with Phase Difference Between Burst and Reference Signal	$\frac{\Delta(V_{15}/V_2)}{\Delta(\phi_5 - \phi_4)}$		5.0		$\frac{1}{\text{rad}}$
Supply Current Consumption	I_3		38		mA

APPLICATION



LEAD NAMES

1. Oscillator Feedback Output
2. Reactance Control Stage Feedback
3. Supply Voltage (12 V)
4. Reference Waveform Output (+)
5. Burst Waveform Input
6. Reference Waveform Output (−)
7. Color Killer Output
8. PAL Flip-Flop Square Wave Input
9. ACC Output
10. ACC Level Setting (see also Lead 12)
11. ACC Gain Setting
12. ACC Level Setting (see also Lead 10)
13. } DC Control Points for
14. } Oscillator Phase Control Loop
15. Oscillator Feedback Input
16. Ground (Negative Supply)

APPLICATION INFORMATION

The function is quoted against the corresponding lead number.

1. **Oscillator Feedback Output**
   The crystal receives its energy from this lead. The input impedance is approximately 2 kΩ in parallel with 5 pF.
2. **Reactance Control Stage Feedback**
   This lead is fed internally with a sinewave derived from the reference input (lead 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from lead 2 to the crystal via C1 is such that the value of C1 is effectively increased. Lead 2 is held internally at a very low impedance, therefore, the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.
3. **Positive 12 V Supply**
   The maximum voltage must not exceed 13.2 V.
4. **Reference Waveform Output**
   This lead is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No dc load to ground is required. A dc connection between leads 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on lead 6, a signal of equal amplitude and opposite phase [-(R-Y)] to that on lead 4. A center tap on the inductor, connected to ground via a dc blocking capacitor, is therefore necessary.
5. **Burst Waveform Input**
   A burst waveform amplitude of 1 V peak-to-peak is required to be ac coupled to this lead. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this lead is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A dc bias of 400 mV is internally derived for lead 5. The absolute level of the tip of the burst at lead 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions, the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the IC which inhibits the performance of the phase lock loop.
6. **Reference Waveform Output**
   This lead requires a reference waveform in the -(R-Y) phase, derived from lead 4 via a bifilar transformer (see lead 4), to drive the internal balanced reactance control stage. A dc connection between leads 4 and 6 must be made via the transformer.
7. **Color Killer Output**
   This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this lead are then +12 V and < 250 mV respectively. (The voltage on lead 9 at which switching of the color killer output on lead 7 occurs is nominally +2.5 V.)
8. **PAL Flip-Flop Square Wave Input**
   A 2.5 V peak-to-peak square wave derived from the PAL flip-flop (in the TBA520 demodulator IC) is required at this lead, ac coupled via a capacitor. The input impedance is about 3.3 kΩ.
9. **ACC Output**
   An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal, the dc potential produced at lead 9 is set to be +4 V (RV1). The appearance of a burst signal on lead 5 will cause the potential on lead 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at lead 9 is determined by the control characteristics of the ACC amplifier (i.e. for the TBA560C from 1 V to 0.2 V). The potential at lead 9 will fall to a value within this range as the burst input signal is stabilized at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong, the potential on lead 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cutoff function in the TBA520 demodulator IC. The switching of the color killer output at lead 7 is designed to occur as the potential on lead 9 moves past +2.5 V.
10. **ACC Level Setting**
    The network connected between leads 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4 on lead 9 with no burst input signal to lead 5. C5 provides filtering.
11. **ACC Gain Control**
    RV2 is adjusted to give the correct amplitude of burst signal on lead 5 (1.5 V peak-to-peak) under ACC control.
12. See lead 10.
13. See lead 14.
14. **DC Control Points in Reference Control Loop**
    Leads 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes of dc balancing the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3, and R4, C4. The dc potentials on these leads are nominally +7.2 V.
15. **Oscillator Feedback Input**
    The input impedance at this lead is nominally 3.5 k in parallel with 5 pF. No dc connection is required on this lead. The signal voltage ratio in the IC between lead 15 and lead 1 is nominally 4.7 times.
16. **Negative Supply (Ground)**

PERFORMANCE AND COMMENTS

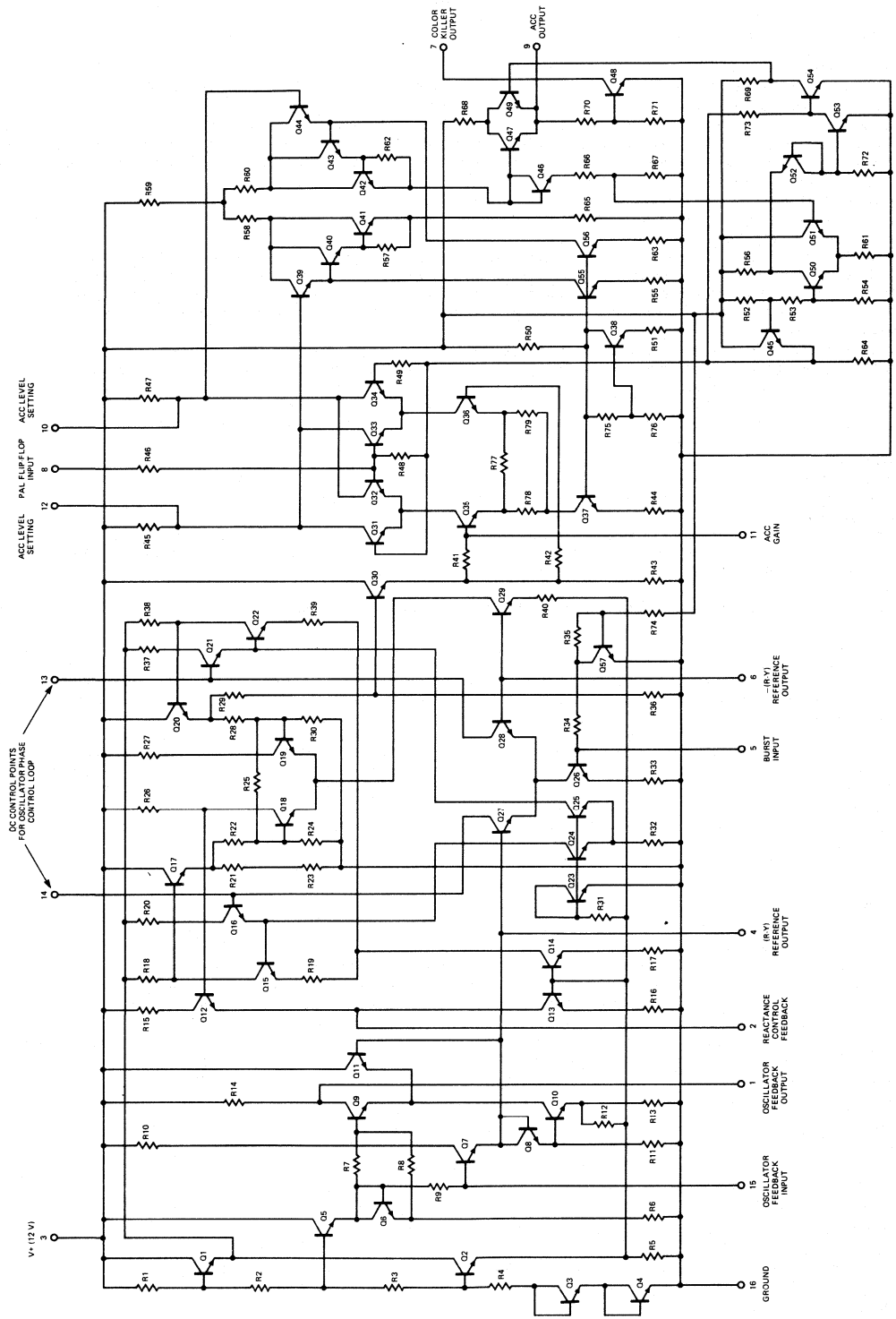
Initial Adjustment

(a) Remove burst signal.
(b) Short circuit leads 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.
(c) Set the ACC level adjustment RV1, to give +4 V on lead 9.
(d) Apply burst signal.
(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5 V peak-to-peak on lead 5.

Phase Lock Loop Performance

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, ±10°.
(b) Typical holding range, ±600 Hz.
(c) Typical pull in range, ±300 Hz.
(d) Temperature coefficient of oscillator frequency, IC only, 2 Hz/°C.

EQUIVALENT CIRCUIT – TBA540



TBA560C

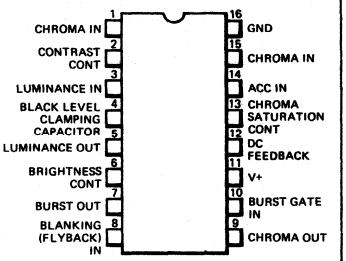
LUMINANCE AND CHROMINANCE CONTROL COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA560C is a monolithic integrated circuit used in the decoding system of color television receivers. It is constructed on a single silicon chip using the Fairchild Planar* process. The circuit consists of a luminance and a chroma amplifier. The luminance amplifier input is matched to the delay line. DC contrast, brightness, black level clamping, blanking, and beam current limiting functions are provided by the luminance amplifier portion of the circuit. The chroma amplifier performs functions such as gain controlled amplification, chroma gain control tracked with contrast control, separate saturation control, PAL delay line driver, burst gating and color killer.

- **DC CONTRAST CONTROL**
- **DC BRIGHTNESS CONTROL**
- **BLACK LEVEL CLAMPING**
- **BEAM CURRENT LIMITING**
- **COLOR KILLER**
- **PAL DELAY LINE DRIVER**
- **CHROMA GAIN/CONTRAST TRACKING**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

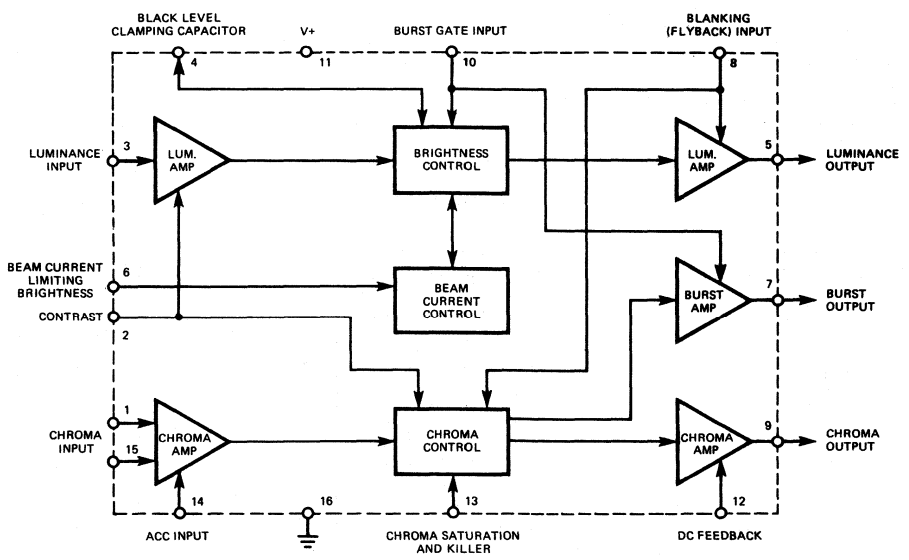
TYPE	PART NO.
560C	TBA560C
(560CQ)	(TBA560CQ)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS (Cont'd on Page 2)

Supply Voltage (Note 1)	13 V
Total Power Dissipation (Note 1)	510 mW
Storage Temperature	−55 to +125°C
Operating Ambient Temperature	0 to +60°C
Lead Temperature (soldering, 10 s)	260°C

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS(Cont'd)

Voltages

V_{1-16}	0 to +5.0 V	V_{10-16}	−5.0 V
V_{2-16}	0 to +12 V (Note 2)	V_{12-16}	−5.0 to +6.0 V
V_{4-16}	0 to +6.0 V	V_{13-16}	−3.0 to +6.5 V (Note 2)
V_{6-16}	0 to +3.0 V	V_{14-16}	−5.0 V
V_{8-16}	−5.0 to +5.0 V	V_{15-16}	0 to +5.0 V

Currents (Positive when flowing into the integrated circuit)

I_1	0 to +1.0 mA	I_9	−10 to 0 mA
I_3	−1.0 to +3.0 mA	I_{10}	+3.0 mA
I_5	−5.0 to 0 mA	I_{14}	+1.0 mA
I_6	−1.0 to +1.0 mA	I_{15}	0 to +1.0 mA
I_7	−3.0 to +2.0 mA		

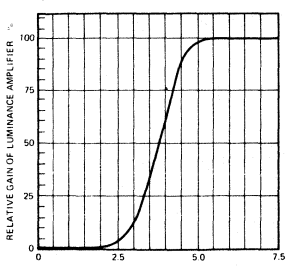
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{11-16} = 12 V, as shown in Test Circuit, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{11}			30		mA
Required Input Signals						
Chrominance Input Signal (Peak-to-Peak Value)	$V_{1-15\ (p\text{-}p)}$			4 to 80		mV
Luminance Input Current (Black to White Value)	$I_{3\ (p\text{-}p)}$			1.5		mA
Contrast Control Voltage Range (for 20 dB of Control)	V_{2-16}	See Typical Performance Curves				
Brightness Control Voltage (Note 3)	V_{6-16}	See Typical Performance Curves				
Saturation Control Voltage Range (for 20 dB of Control)	V_{13-16}	See Typical Performance Curves				
Burst Keying Pulse (Positive) (Peak-to-Peak Value)	$I_{10\ (p\text{-}p)}$		0.05	1.0		mA
Flyback Blanking Pulses (Negative) (Peak-to-Peak Value)						
for 0 V Blanking Level at Lead 5	$V_{8-16\ (p\text{-}p)}$			−0.5		V
for 1.5 V Blanking Level at Lead 5	$V_{8-16\ (p\text{-}p)}$			−2.5		V
Color Killer	V_{13-16}				1.0	V
Automatic Chrominance Control Threshold (Note 4)	V_{14-16}			1.2		V
Obtainable Output Signals						
Luminance Output Voltage at Nominal Contrast (Peak-to-Peak Value)	$V_{5-16\ (p\text{-}p)}$	Note 5		3.0		V
Burst Signal (Peak-to-Peak Value)	$V_{7-16\ (p\text{-}p)}$	Note 6		1.0		V
Chrominance Signal at Nominal Contrast & Saturation (Peak-to-Peak Value)	$V_{9-16\ (p\text{-}p)}$	Note 5		1.0		V
3.0 dB Bandwidth of Chrominance and Luminance Amplifier				5.0		MHz
Change of Ratio, Luminance to Chrominance Signals at 10 dB Contrast Control				2.0		dB

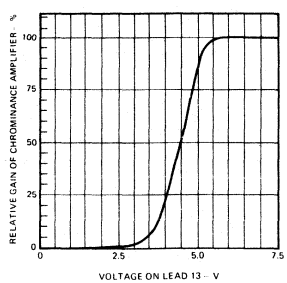
NOTES:
1. Permissible while tubes are heating up: $V_{11-16\ (max)}$ 16 V and $P_{tot\ (max)}$ 700 mW.
2. V_{2-16} and V_{13-16} must always be lower than V_{11-16}.
3. When V_{6-16} is increased above 1.7 V the black level of the output signal remains at 2.7 V.
4. A negative going potential provides a 26 dB ACC range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of 500 mV typical.
5. Nominal setting: maximum contrast and/or saturation minus 6.0 dB.
6. Burst signal is kept constant at 1.0 V peak-to-peak by automatic gain control (AGC Circuit).

TYPICAL PERFORMANCE CURVES

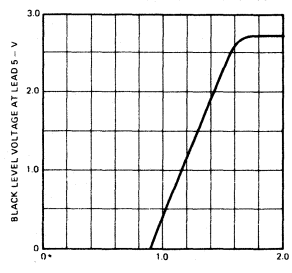
CONTRAST CONTROL OF LUMINANCE AMPLIFIER



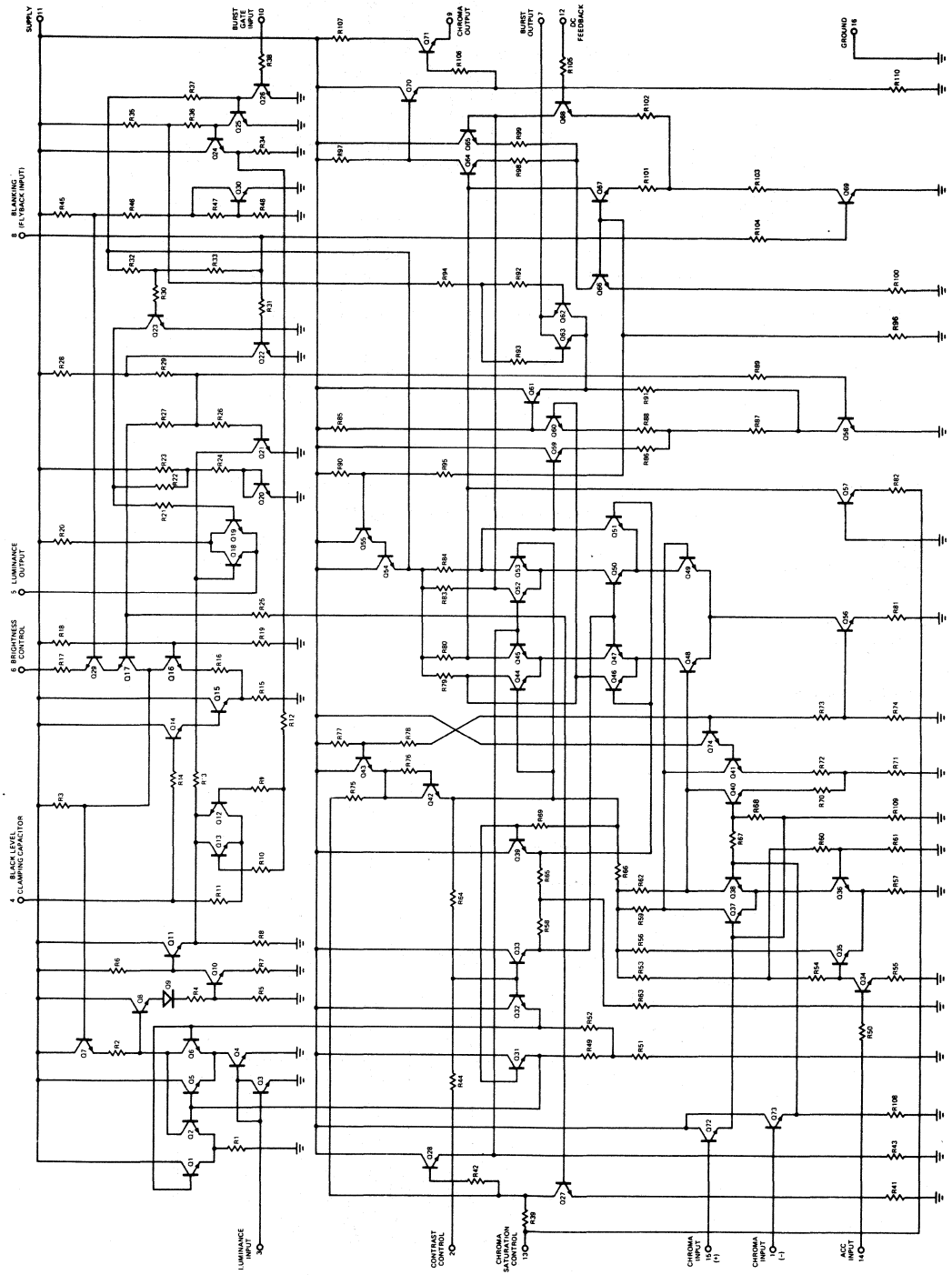
SATURATION OF CHROMINANCE AMPLIFIER



CONTROL OF BLACK LEVEL AT OUTPUT LUMINANCE AMPLIFIER



EQUIVALENT CIRCUIT – TBA560C



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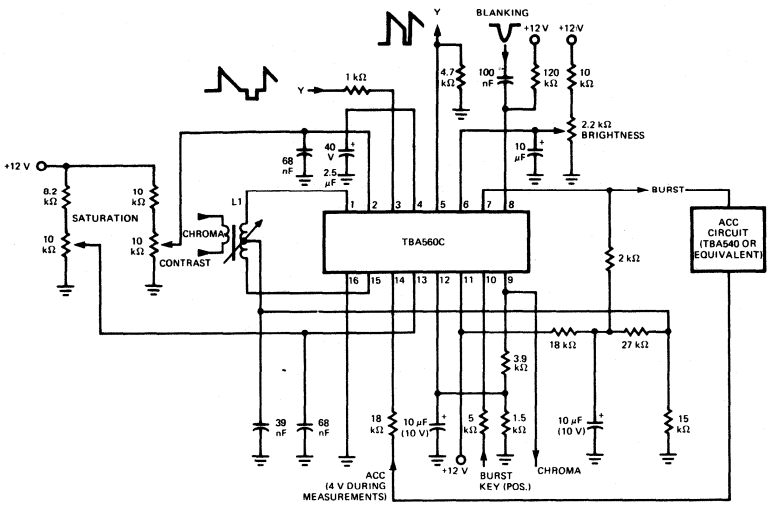
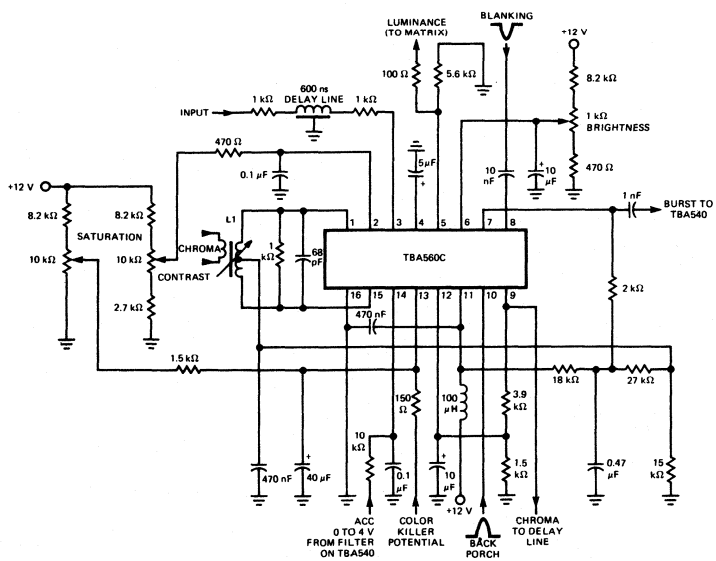
TEST CIRCUIT



APPLICATION INFORMATION

LEAD NAMES

1. Balanced Chroma Signal Input
2. Contrast Control
3. Luminance Signal Input
4. Black Level Clamp Capacitor
5. Luminance Signal Output
6. Brightness Control
7. Burst Output
8. Flyback Blanking Input
9. Chroma Signal Output
10. Burst Gate and Clamping Pulse Input
11. Supply Voltage (12 V)
12. DC Feedback for Chroma Channel
13. Chroma Saturation Control
14. ACC Input
15. Chroma Signal Input
16. Ground (Negative Supply)



Application diagram for operation in combination with the TBA540.

APPLICATION INFORMATION (Cont'd)

The function is quoted against the corresponding lead number.

1. **Balanced Chroma Signal Input** (in conjunction with lead 15)
   This is derived from the chroma signal bandpass filter, designed to provide the balanced input. A differential input signal amplitude of at least 4 mV peak-to-peak is required on leads 1 and 15. Both leads require a dc potential of approximately +3.0 V. This is derived as a common-mode signal from a network connected to lead 7 (burst output). In this way, dc feedback is provided over the burst channel to stabilize its operation.
   All figures for the chominance signals are based on a color bar signal with 75% saturation: i.e. burst to chroma ratio of input signal is 1:2.
2. **DC Contrast Control**
   With +3.7 V on this lead, the gain in the luminance channel is such that a 1.5 mA peak-to-peak input signal to lead 3 gives a luminance output signal amplitude on lead 5 of 3 V black to white. A variation of voltage on lead 2 between +6 V and +2 V gives a corresponding gain variation of +6 to > -14 dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals.
3. **Luminance Signal Input**
   This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and must have about 1.5 mA black to white amplitude.
4. **Charge Storage Capacitor for Black Level Clamp**
   Brightness control can also be achieved on this lead by inserting a negative going line flyback pulse, clipped by a diode to be rectangular, across a resistor of approximately 47 Ω in series with the storage capacitor (5.0 μF). Variation of the amplitude of this pulse shifts the black level of the clamped luminance signal and thus controls the picture brightness.
5. **Luminance Signal Output**
   An emitter follower provides a low impedance output signal of 3 V black to white amplitude at nominal contrast setting having a black level in the range 0 to +3 V. An external emitter load resistor is required, greater than 1 kΩ.
   Black level shift at contrast control is typically in the range of ±10 mV if the luminance input current during black level is about 0.75 mA. When this current has a different value a larger black level shift has to be taken into account. If the input current during black level differs 1 mA from the nominal value of 0.75 mA, the black level shift will be about 100 mV over the complete contrast control range. For smaller differences of the input current, the black level shift will be correspondingly smaller.
   Black level shift with video signal content occurs only when the input signal is ac coupled. The value depends on the drive current amplitude and can be calculated from the figures given above (for maximum contrast; for a lower contrast setting the variation is correspondingly smaller).
   Black level shift over an ambient temperature variation of 30°C is typically −140 mV.
6. **The DC Level of the Luminance Output Signal May be Controlled by the DC Potential Applied to this Lead.**
   Over the range of potential +0.9 to +1.7 V, the black level of the luminance output signal (lead 5) is increased from 0 to +2.7 V. The output signal black level remains at +2.7 V when the potential on lead 6 is increased above +1.7 V.
7. **Burst Output**
   A 1 V peak-to-peak burst (kept constant by the ACC system) is produced here. Also, to achieve good dc stability by negative feedback in the burst channel, the dc potential at this lead is fed back to leads 1 and 15 via the chroma input transformer. When limiting occurs, the burst amplitude is typically 3.0 V.
8. **Flyback Blanking Input Waveform**
   Negative going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of less than −1 V negative excursion are applied, the signal level at the luminance output (lead 5) during blanking will be 0 V. However, if the blanking pulses applied to lead 8 have an amplitude of −2 to −3 V, the signal level at the luminance output during blanking will be +1.5 V.
9. **Chroma Signal Output**
   With a 1 V peak-to-peak burst output signal (lead 7) and at nominal contrast and saturation setting (leads 2 and 13), the chroma signal output amplitude is 1 V peak-to-peak. An external dc network is required which provides negative feedback in the chroma channel via lead 12.
10. **Burst Gating and Clamping Pulse Input**
    A positive pulse of minimum 50 μA is required on this lead to provide gating in the burst channel and luminance channel black level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync pulse or picture line periods during normal operation of the receiver.
11. **+12 V Power Supply**
    Correct operation occurs within the range 10 to 13 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 510 mW at 60°C ambient temperature.
12. **DC Feedback for Chroma Channel** (See lead 9)
13. **Chroma Saturation Control**
    A control range of +6 to > -14 dB is provided over a range of dc potential on lead 13 from +2.7 to +6.2 V. Color killing is also done at this terminal by reducing the dc potential to less than +1 V, e.g. from the TBA540 color killer output terminal. The kill factor is min 40 dB.
14. **ACC Input**
    A negative going potential gives a 26 dB range of ACC starting at +1.2 V and giving maximum gain reduction at an input voltage of typically 500 mV.
15. **Chroma Signal Input** (See lead 1)
16. **Negative Supply** (Ground)

10

TBA641

AUDIO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

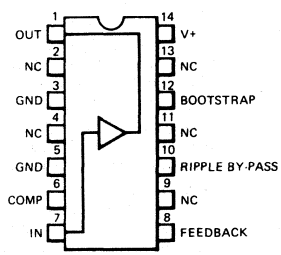
GENERAL DESCRIPTION – The TBA641 is a monolithic integrated circuit designed for use as an audio power amplifier in portable radio receivers, tape recorders, record players and in industrial applications which require high output power, low distortion and high reliability performance.

Special features of the circuit include low quiescent current, self-centering bias operation at supply voltages ranging from 6 V to 12 V (16 V on TBA641 B11) and direct coupling of the input. The circuit requires a minimum of external components. It is constructed on a single silicon chip using the Fairchild Planar* process.

- **OUTPUT POWER 2.2 W (9 V – 4 Ω) – TBA641 A12**
- **OUTPUT POWER 4.5 W (14 V – 4 Ω) – TBA641 B11**
- **LOW DISTORTION**
- **LOW QUIESCENT CURRENT**
- **SELF-CENTERING BIAS**
- **HIGH INPUT IMPEDANCE**

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)

PACKAGE OUTLINE	9H	9J
PACKAGE CODE	A12	B11



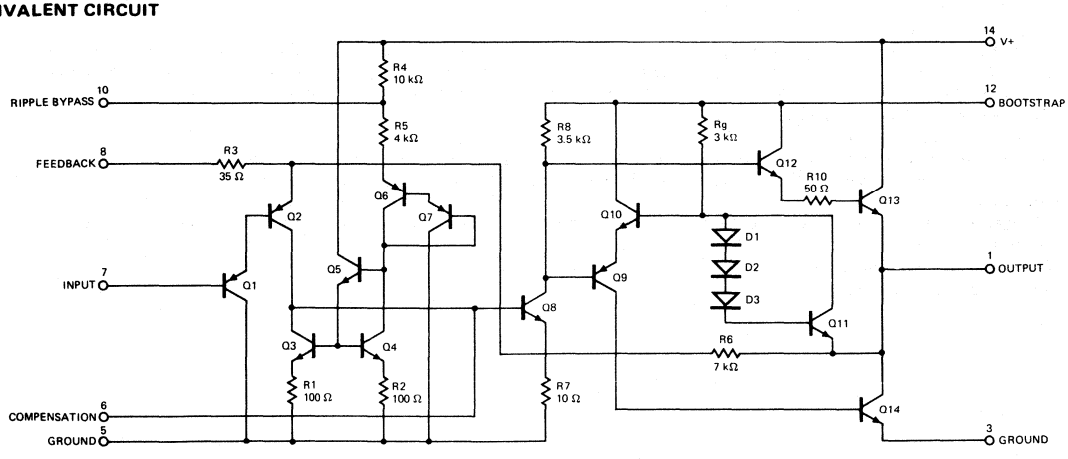
ABSOLUTE MAXIMUM RATINGS	TBA641 A12	TBA641 B11
Supply Voltage (no signal)	12 V	18 V
Supply Voltage	12 V	16 V
Input Voltage	−0.5 V to V+	−0.5 V to V+
Peak Output Current	2A	2.5A
Storage Temperature	−40°C to +150°C	−40°C to +150°C
Power Dissipation ($T_A \leq 25°C$)	1.5 W	2.3 W
Power Dissipation ($T_A = 70°C$)		1.45 W
Power Dissipation ($T_C = 70°C$)		6 W
Max. Junction Temperature	150°C	150°C

THERMAL DATA (Typical)	TBA641 A12	TBA641 B11
θ_{J-C} (thermal resistance junction to case)	13°C/W	13°C/W
θ_{J-A} (thermal resistance junction to ambient)	83°C/W	55°C/W

ORDER INFORMATION

TYPE	PART NO.
TBA641 A12	SL24617
TBA641 B11	SL24618

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

TBA641 B11

ELECTRICAL CHARACTERISTICS V+ = 14 V, R_L = 4 Ω, T_A +25°C unless otherwise specified. (See Test Circuit)

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current		P_{OUT} = 0		16	32	mA
Quiescent Current of Output Transistors		P_{OUT} = 0		13		mA
Input Bias Current (Pin 7)				250		nA
DC Output Level (Pin 1)			6.5	7	8	V
Voltage Gain		R_f = 0 Ω		46		dB
Output Power		THD = 10%, f = 1 kHz, A_V = 46 dB	4	4.5		W
Total Harmonic Distortion		P_{OUT} = 50 mW, f = 1 kHz, A_V = 46 dB		0.3		%
		P_{OUT} = 2W, f = 1 kHz, A_V = 46 dB		0.8		%
Equivalent Input Noise Voltage		R_S = 22 kΩ, BW = 10 kHz		3.4		μV
Total Supply Current		P_{OUT} = 4.5W		485		mA
Internal Feedback Resistors	R6			7		kΩ
(see equivalent circuit)	R3			35		Ω
Input Impedance (Pin 7)		A_V = 46 dB, f = 1 kHz		3		MΩ

TBA641 A12

ELECTRICAL CHARACTERISTICS V+ = 9 V, R_L = 4 Ω, T_A = 25°C unless otherwise specified. (See Test Circuit)

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current		P_{OUT} = 0		8	18	mA
Quiescent Current of Output Transistors		P_{OUT} = 0		6		mA
Input Bias Current (Pin 7)				100		nA
DC Output Level (Pin 1)			4	4.5	5	V
Voltage Gain		R_f = 0 Ω		46		dB
Output Power		THD = 10%, f = 1 kHz, A_V = 46 dB	1.8	2.2		W
Total Harmonic Distortion		P_{OUT} = 50 mW, f = 1 kHz, A_V = 46 dB		0.6		%
		P_{OUT} = 1W, f = 1 kHz, A_V = 46 dB		0.6		%
Equivalent Input Noise Voltage		R_S = 22 kΩ, BW = 10 kHz		2.5		μV
Total Supply Current		P_{OUT} = 2.2W		340		mA
Internal Feedback Resistors	R6			7		kΩ
(see equivalent circuit)	R3			35		Ω
Input Impedance (Pin 7)		A_V = 46 dB, f = 1 kHz		3		MΩ

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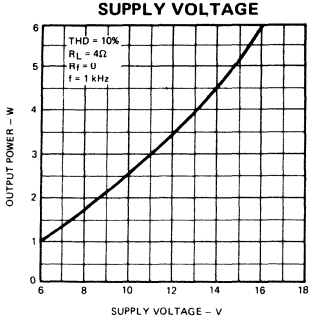
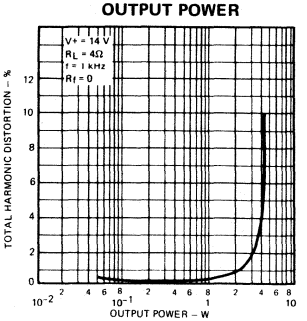
TYPICAL PERFORMANCE CURVES FOR TBA641 B11

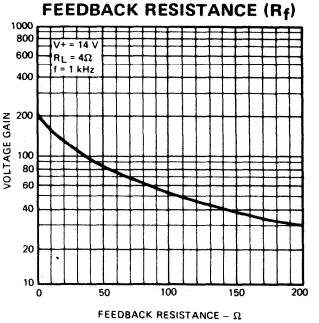
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



DISTORTION AS A FUNCTION OF OUTPUT POWER

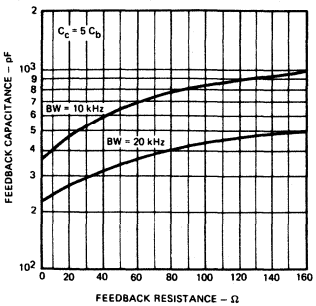


VOLTAGE GAIN AS A FUNCTION OF FEEDBACK RESISTANCE (R_f)

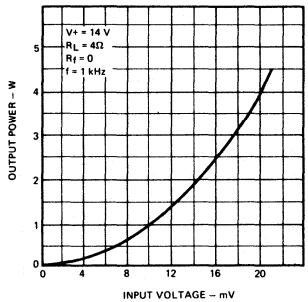


TYPICAL PERFORMANCE CURVES FOR TBA641 B11 (Cont'd)

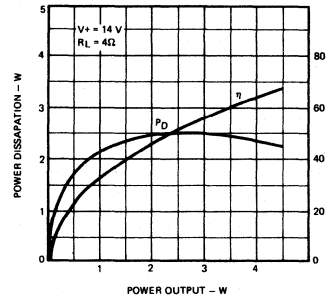
C_b AS A FUNCTION OF R_f FOR VARIOUS VALUES OF BANDWIDTH



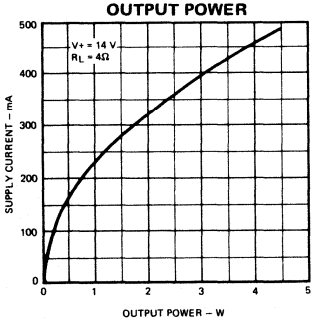
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



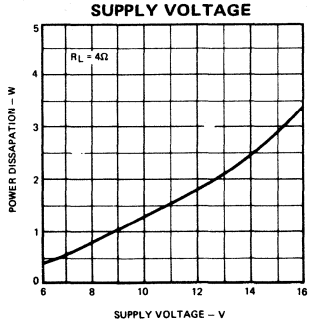
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



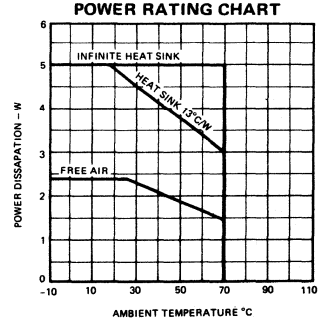
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



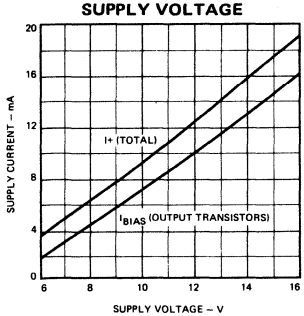
MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



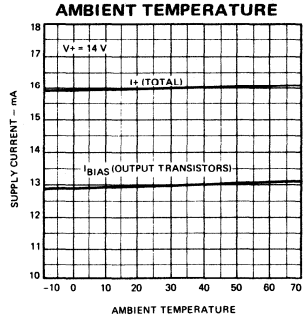
POWER RATING CHART



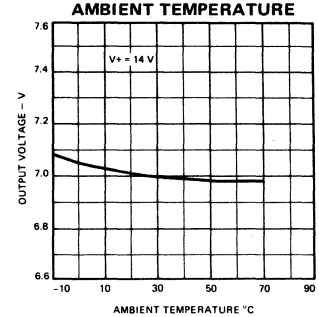
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



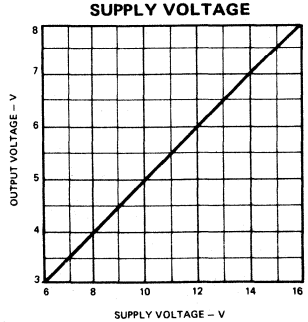
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

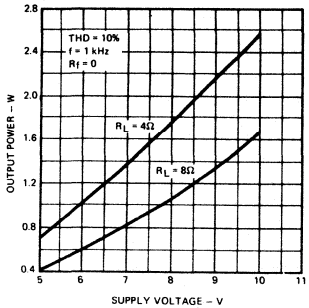


QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

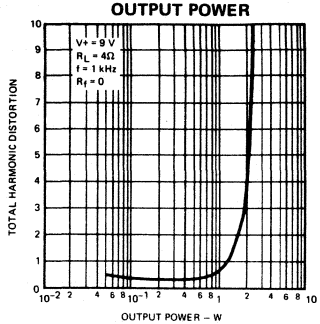


TYPICAL PERFORMANCE CURVES FOR TBA641 A12

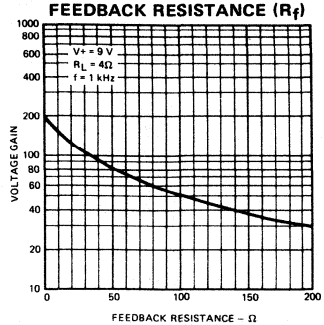
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



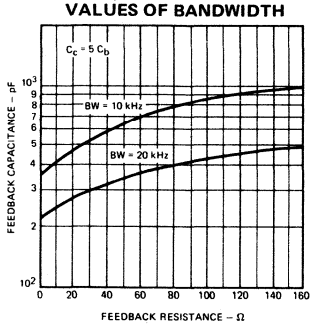
DISTORTION AS A FUNCTION OF OUTPUT POWER



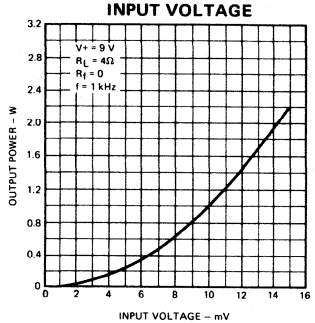
VOLTAGE GAIN AS A FUNCTION OF FEEDBACK RESISTANCE (R_f)



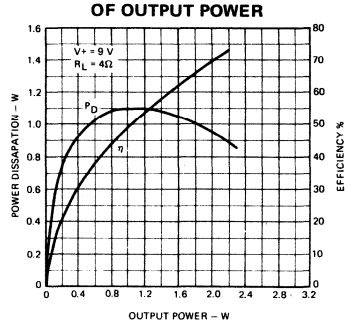
C_b AS A FUNCTION OF R_f FOR VARIOUS VALUES OF BANDWIDTH



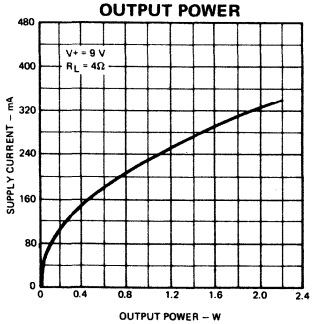
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



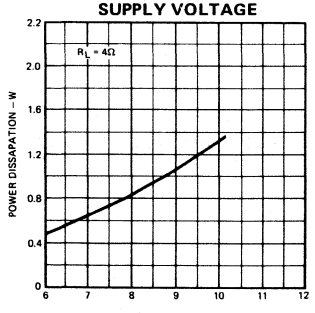
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



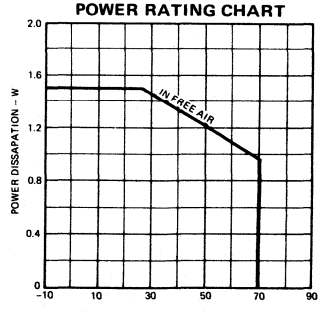
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



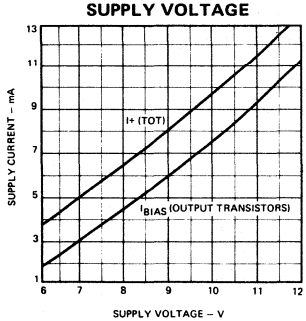
MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



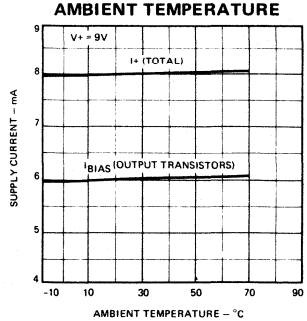
POWER RATING CHART



QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



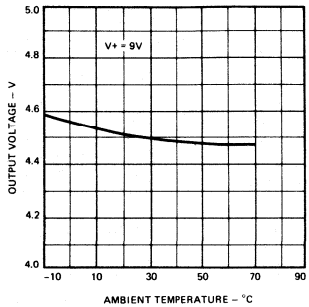
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



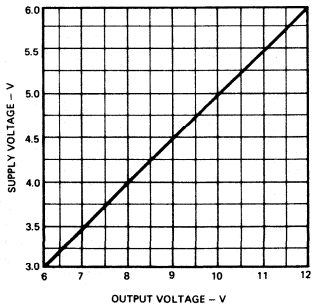
10

TYPICAL PERFORMANCE CURVES FOR TBA641 A12 (Cont'd)

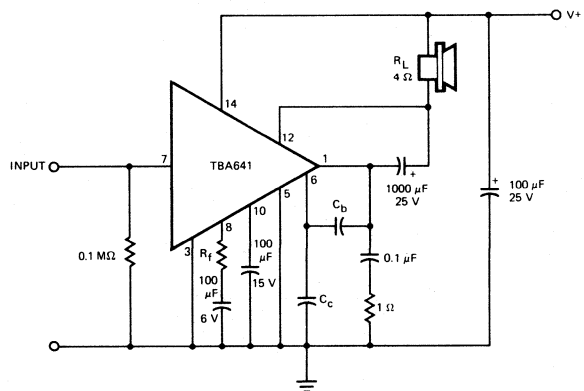
QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



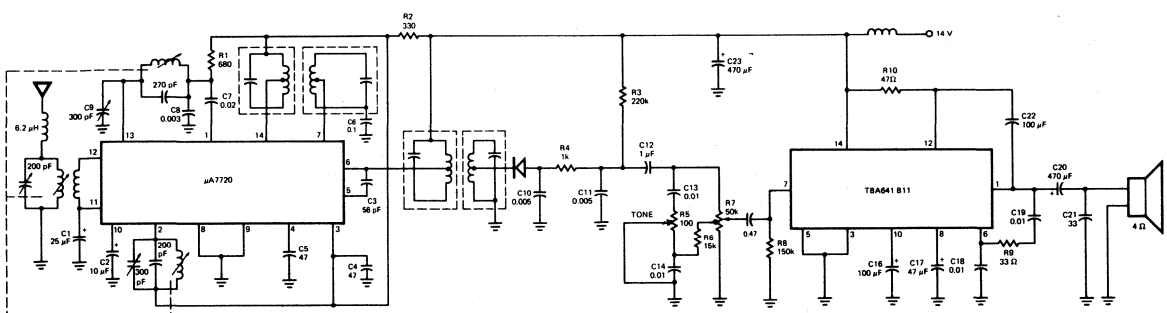
QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



TEST AND APPLICATION CIRCUIT – TBA641



AM CAR RADIO APPLICATION TBA641 B11



ELECTRICAL PERFORMANCE

Output power (THD = 10%)	4.5 W
Useable sensitivity (S/N = 20 dB)	10 μV
S/N (5 mV Input)	40 dB
AGC Range (ΔV_{OUT} = 10 dB)	80 dB

MOUNTING INSTRUCTIONS – TBA641 B11 Power dissipation can be increased by means of an additional external heat sink fixed with two screws or by soldering the pins of the external bar to suitable copper areas on the PC board (TBA641 B11).

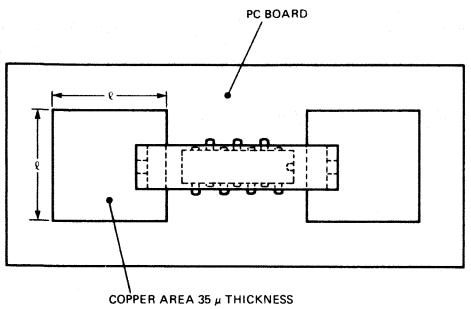
A. In the former case, the thermal resistance case-ambient of the added heat sink can be calculated as follows:

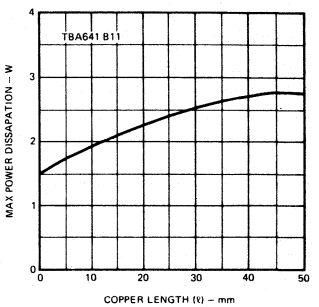
$$\theta_{C\text{-}A} = \frac{(T_{J(MAX)} - T_A) - (P_D)(\theta_{J\text{-}C})}{P_D}$$

where:

$T_{J(MAX)}$ = Max junction temperature
T_A = Ambient temperature
P_D = Power dissipation
$\theta_{J\text{-}C}$ = Thermal resistance junction to case

B. If copper areas on the PC board are used (TBA641 B11) the diagrams below give the maximum power dissipation as a function of copper area, with copper thickness 35 μ and ambient temperature 55°C.





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TBA810S/TBA810AS TBA810DS/TBA810DAS

7 WATT AUDIO POWER AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA810S is a monolithic integrated circuit in a 12-lead plastic power package intended for use as a low frequency class B power amplifier. It is constructed using the Fairchild Planar* epitaxial process. With a 4 Ω speaker impedance, it typically provides 7 W at 16 V, 6 W at 14.4 V, 2.5 W at 9 V, and 1 W at 6.0 V. It offers high output current capability (up to 2.5 A), high efficiency (75% at 6 W output) and very low harmonic and crossover distortion.

The TBA810AS has the same electrical characteristics as the TBA810S, but its cooling tabs are flat and provide mounting holes for heat sink attachment.

The TBA810DS is electrically the same as the TBA810S except it includes an overvoltage protection circuit (load dump circuit). This feature makes the TBA810DS ideally suitable for car radio applications.

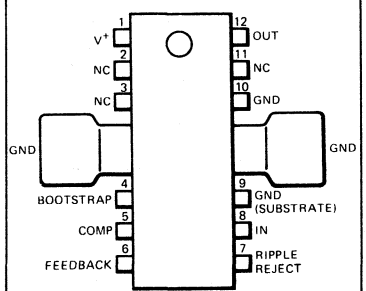
The TBA810DAS has the same electrical characteristics as the TBA810DS, but the cooling tabs are flat and provide mounting holes.

- **THERMAL SHUTDOWN**
- **OVERVOLTAGE PROTECTION (TBA810DS, TBA810DAS)**
- **WIDE SUPPLY VOLTAGE RANGE (4 V TO 20 V)**
- **HIGH CURRENT CAPABILITY (2.5 A)**
- **12-LEAD POWER PACKAGE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Peak Current (Non-Repetitive)	3.5 A
Output Current (Repetitive)	2.5 A
Input Voltage	220 mVrms
Power Dissipation: at T_A = 70°C	1.0 W
at T_C = 100°C	5.0 W
Storage and Junction Temperature	−40 to 150°C
Lead Temperature (Soldering, 12 s)	230°C

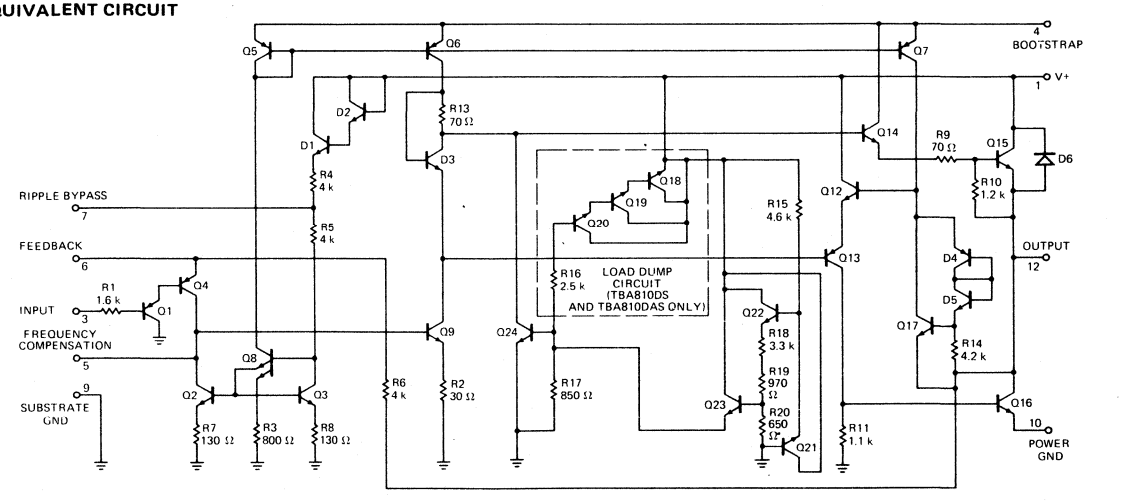
CONNECTION DIAGRAM
12-LEAD POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODES P3, P4



ORDER INFORMATION

TYPE	PART NO.
810S(P3)	TBA810S
810DS(P3)	TBA810DS
810AS(P4)	TBA810AS
810DAS (P4)	TBA810DAS

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

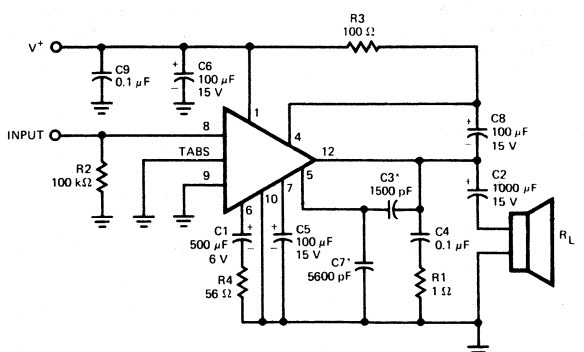
ELECTRICAL CHARACTERISTICS (Refer to the test circuit: $T_A = 25°C$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Output Voltage (Pin 12)	V+ = 14.4 V	6.4	7.2	8.0	V
Quiescent Drain Current (Pin 1)			12	20	mA
Bias Current (Pin 8)			0.4		μA
Power Output	THD = 10%, R_L = 4.0 Ω, f = 1.0 kHz				
	V+ = 16 V		7.0		W
	V+ = 14.4 V		6.0		W
	V+ = 9.0 V		2.5		W
	V+ = 6.0 V		1.0		W
Input Sensitivity	P_{OUT} = 6 W, V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz				
	R_f = 56 Ω		80		mV
	R_f = 22 Ω		35		mV
Input Resistance (Pin 8)			5.0		MΩ
Frequency Response (−3.0 dB)	V+ = 14.4 V, R_L = 4.0 Ω				
	C3 = 820 pF		40 to 20,000		Hz
	C3 = 1500 pF		40 to 10,000		Hz
Total Harmonic Distortion	P_{OUT} = 50 mW to 3 W, V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz		0.3		%
Voltage Gain (Open Loop)	V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz		80		dB
Voltage Gain (Closed Loop)	V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz	34	37	40	dB
Input Noise Voltage	V+ = 14.4 V, R_g = 0, BW (−3.0 dB) = 20 Hz to 20,000 Hz		2.0		μV
Input Noise Current	V+ = 14.4 V, BW(−3.0 dB) = 20 Hz to 20,000 Hz		0.1		nA
Efficiency	P_{OUT} = 5 W, V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz		70		%
Supply Voltage Rejection	V+ = 14.4 V, R_L = 4.0 Ω, f_{ripple} = 100 Hz		38		dB

THERMAL DATA		TBA810S/DS	TBA810AS/DAS
θ_{JC}	Thermal Resistance Junction to Case (tab)	12°C/W	10°C/W
θ_{JA}	Thermal Resistance Junction to Ambient	70°C/W**	80°C/W

**Obtained with tabs soldered to printed circuit with minimized copper area.

TEST AND APPLICATION CIRCUIT



*C3, C7 See Fig. 6

TYPICAL PERFORMANCE CURVES FOR TBA810S/TBA810AS/TBA810DS/TBA810DAS

POWER OUTPUT AS A FUNCTION OF SUPPLY VOLTAGE

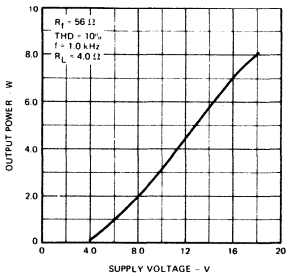


Fig. 1

MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)

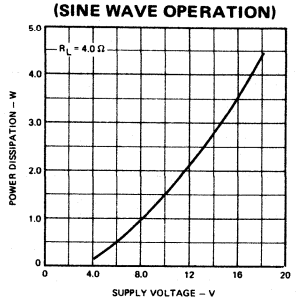


Fig. 2

TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT

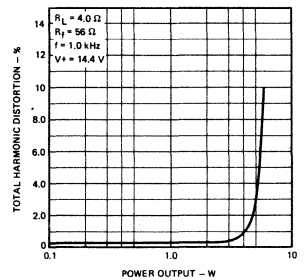


Fig. 3

TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY

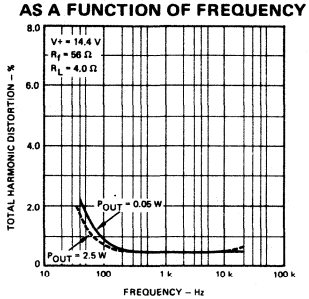


Fig. 4

TYPICAL RELATIVE VOLTAGE GAIN (CLOSED LOOP) AND TYPICAL INPUT VOLTAGE AS A FUNCTION OF FEEDBACK RESISTANCE (R_f)

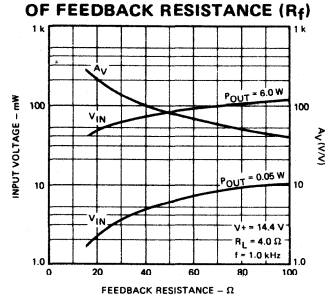


Fig. 5

TYPICAL VALUE OF C3 AS A FUNCTION OF R_f FOR VARIOUS VALUES OF BANDWIDTH

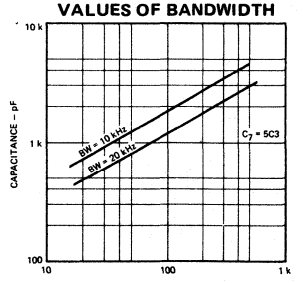


Fig. 6

TYPICAL POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT

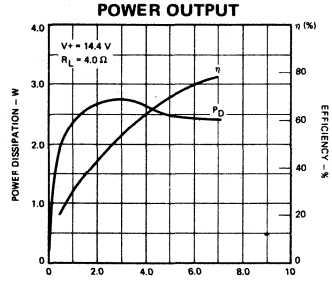


Fig. 7

TYPICAL PERFORMANCE CURVES FOR TBA810S/TBA810AS/TBA810DS/TBA810DAS (Cont'd)

TYPICAL QUIESCENT OUTPUT VOLTAGE (PIN 12) AS A FUNCTION OF SUPPLY VOLTAGE

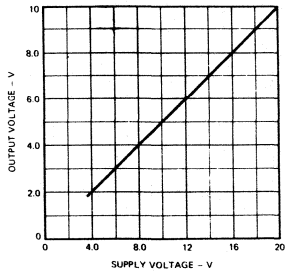


Fig. 8

TYPICAL QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

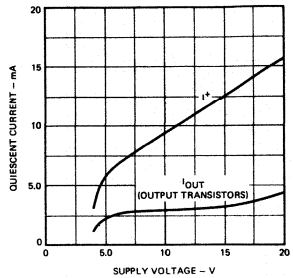


Fig. 9

TYPICAL SUPPLY VOLTAGE REJECTION AS A FUNCTION OF FEEDBACK RESISTANCE

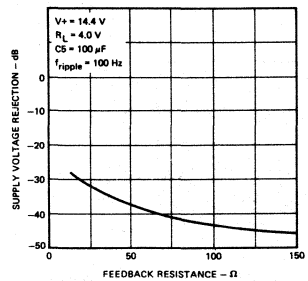


Fig. 10

TYPICAL CIRCUIT WITH LOAD CONNECTED TO THE SUPPLY VOLTAGE

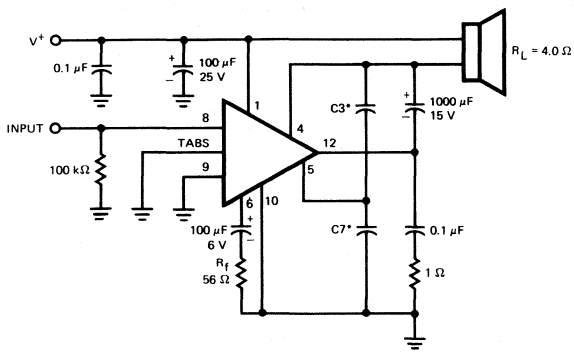


Fig. 11

TYPICAL SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_f (FIG. 11 CIRCUIT)

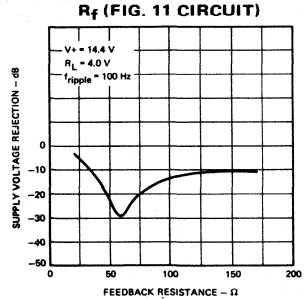


Fig. 12

*C3, C7 see Fig. 6.

10

MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heat sink (TBA810AS/TBA810DAS, Figure 13) or by soldering them to an area of copper on the printed circuit. (TBA810S/TBA810DS, Figure 14). During soldering, the tabs temperature must not exceed 230°C and the soldering time must not be longer than 12 seconds. Figures 15a and 15b show two ways that can be used for mounting the device.

MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TBA810AS AND TBA810DAS)

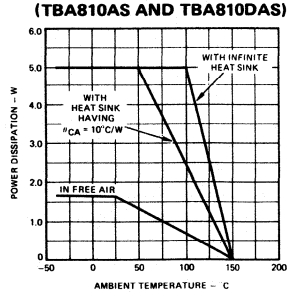
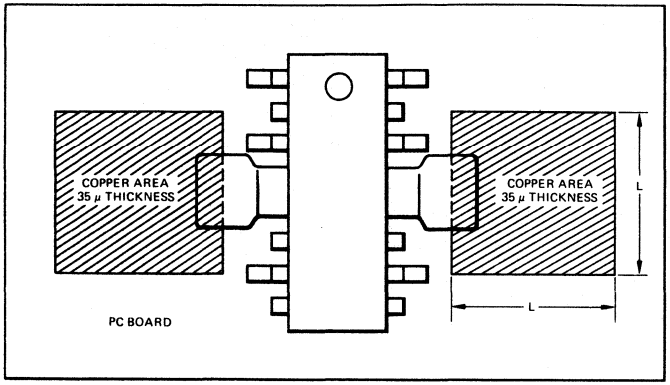


Fig. 13

MAXIMUM POWER DISSIPATION AND TOTAL THERMAL RESISTANCE AS A FUNCTION OF COPPER AREA OF PC BOARD (TBA810S AND TBA810DS)



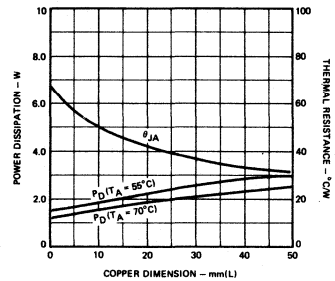


Fig. 14

Figure 15a shows a method of mounting the TBA810S or TBA810DS that is satisfactory both from the point of view of heat dissipation and from mechanical considerations. For the TBA810AS and the TBA810DAS, the desired thermal resistance is obtained attaching the hardware shown in Figure 15b, to a bracket with proper dimensions. This bracket can also act as a support for the whole printed circuit board.

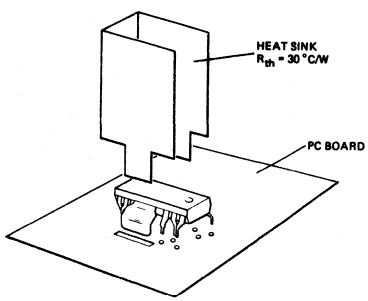


Fig. 15a

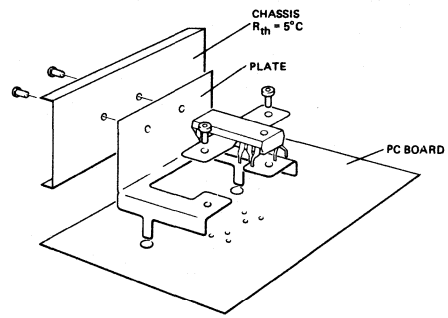


Fig. 15b

THERMAL SHUTDOWN

The on chip design of the thermal limiting circuit offers the following advantages:

1. An overload on the output (even if permanent) or an above-limit ambient temperature can be easily handled.
2. The heat sink can have a smaller factor of safety compared with that of a conventional circuit. In case of too high a junction temperature, power output, power dissipation and the supply current decrease (Figure 16) thus protecting the device.

OUTPUT POWER AND SUPPLY CURRENT AS A FUNCTION OF CASE TEMPERATURE

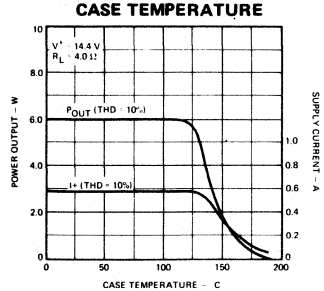


Fig. 16

TBA920 • TBA920S

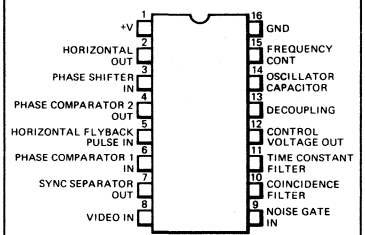
TELEVISION HORIZONTAL OSCILLATORS

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA920s are monolithic integrated circuits designed for TV receiver applications. They are constructed on a single silicon chip using the Fairchild Planar* process. They accept the composite video signal, separate sync pulses (with the added safeguard of noise gating) and provide a sync output for the vertical integrator. Also incorporated is the horizontal oscillator along with two phase comparators, one to compare flyback pulses to the oscillator and the other for sync phase comparison. The devices will interface with both SCR and transistor deflection systems.

- **SYNC SEPARATOR**
- **NOISE GATE**
- **HORIZONTAL OSCILLATOR**
- **DUAL PHASE COMPARATOR**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
920	TBA920
(920Q)	(TBA920Q)†
920S	TBA920S

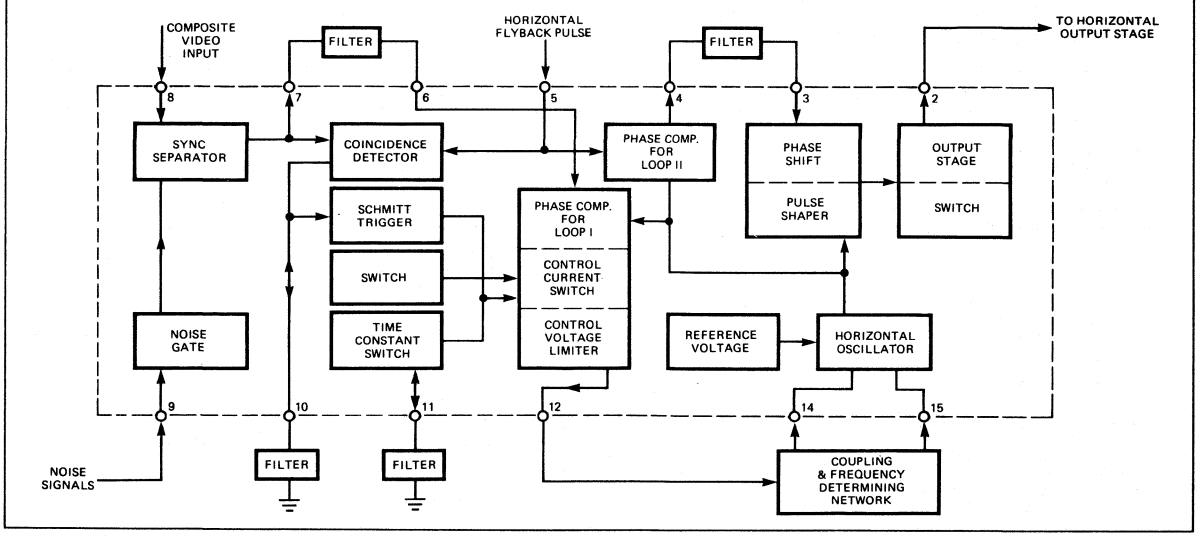
†Not recommended for new designs.

10

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Total Power Dissipation (Note 1)	600 mW
Storage Temperature	−55°C to +125°C
Operating Temperature	−20°C to +60°C
Lead Temperature (Soldering, 10 s)	260°C
Voltages	
$V_1 - 16$	13.2 V
$V_3 - 16$	0 to 13.2 V
$V_8 - 16$	−12 V
$V_{10} - 16$	−0.5 to 5.0 V
Currents	
I_2 (Average Value)	−20 mA
I_2 (Peak Value)	−200 mA
I_5 (Peak Value)	10 mA
I_7 (Peak Value)	10 mA
I_8 (Peak Value)	10 mA
I_9 (Peak Value)	10 mA

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{1-16} = 12 V, See Applications Circuit (CCIR Standard), unless otherwise specified.
***Note: TBA920S is identical to the TBA920 except as indicated.**

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption	I_1	$I_2 = 0$		36		mA
Video Signal						
Input Voltage (Positive Going Sync) Peak-to-Peak Value	V_{IN} (p-p)		1.0	3.0	7.0	V
Input Current During Sync Pulse (Peak Value)	I_8			100		μA
Noise Gating (Lead 9)						
Input Voltage (Peak Value)	V_{9-16}		0.7			V
Input Current (Peak Value)	I_9		0.03		10	mA
Input Resistance	R_{9-16}			200		Ω
Flyback Pulse (Lead 5)						
Input Voltage (Peak Value)	V_{5-16}			±1.0		V
Input Current (Peak Value)	I_5		0.05	1.0		mA
Input Resistance	R_{5-16}			400		Ω
Pulse Duration	t_5	f = 15625 Hz	10			μs
Composite Sync Pulses (Positive, Lead 7)						
Output Voltage (Peak-to-Peak Value)	V_{7-16} (p-p)			10		V
Output Resistance						
at Leading Edge of Pulse (Emitter Follower)	R_{7-16}			50		Ω
at Trailing Edge	R_{7-16}			2.2		kΩ
Additional External Load Resistance	R_{7-16} (ext.)		2.0			kΩ
Driver Pulse (Lead 2)						
Output Voltage (Peak-to-Peak Value)	V_{2-16} (p-p)			10		V
Average Output Current	I_2 (AVG)				20	mA
Peak Output Current	I_2				200	mA
Output Resistance (Low Ohmic)	R_{2-16}	Note 2		2.5 or 15		Ω
Output Pulse Duration	t_2	Note 3		12 to 32		μs
Permissible Delay Between Leading Edge of Output Pulse and Flyback Pulse	t_d (tot)	t_5 = 12 μs		0 to 15		μs
Supply Voltage at Which Output Pulses are Obtained	V_{1-16}		4.0			V
Oscillator						
Frequency, Free Running	f_o	R_{15-16} = 3.3 kΩ (Note 4)		15625		Hz
Spread of Frequency at Nominal Values of Peripheral Components (TBA920)	$\frac{\Delta f_o}{f_o}$	Note 5			±5.0	%
*Spread of Frequency at Nominal Values of Peripheral Components (TBA920S)	$\frac{\Delta f_o}{f_o}$				±1.5	%
Frequency Change When Decreasing the Supply Down to Minimum 4.0 V	$\frac{\Delta f_o}{f_o}$				10	%
Frequency Control Sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$			16.5		Hz/μA
Adjustment Range of Network in Circuit on Application Information (TBA920)	$\frac{\Delta f_o}{f_o}$			±10		%
*Adjustment Range of Network in Figure 1 (TBA920S)	$\frac{\Delta f_o}{f_o}$			±5.0		%
Influence of Supply Voltage on Frequency	$\frac{\delta f_o/\delta V}{f_o/V_{nom}}$	V_1 = 12 V			5.0	%
Control Loop I (Between Sync Pulse and Oscillator)						
Control Voltage Range	V_{12-16}			0.8 to 5.5		V
Control Current (Peak Values)	I_{12}	$V_{10-16} > 4.5$ V; $V_{6-16} > 1.5$ V,		±2.0		mA
	I_{12}	$V_{10-16} > 2.0$ V; $V_{6-16} > 1.5$ V		±6.0		mA
Loopgain of APC System						
a. Time Coincidence Between Sync Pulse and Flyback Pulse or $V_{10-16} > 4.5$ V	$\frac{\Delta f}{\Delta t}$			1.0		kHz/μs
b. No Time Coincidence or $V_{10-16} < 2.0$ V	$\frac{\Delta f}{\Delta t}$			3.0		kHz/μs
Capture and Holding Range	Δf	Note 6		±1.0		kHz
Pull In Time for $\Delta f/f_o$ = ±3%	t	Δf = 470 Hz (Note 7)		20		ms
Switch Over From Large Control Sensitivity to Small Control Sensitivity After Capture	t	Note 7		20		ms

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Control Loop II (Between Flyback Pulse and Oscillator)						
Permissible Delay Between Leading Edge of Output Pulse (Lead 2) and Leading Edge of Flyback Pulse	$t_{d\,(tot)}$			0 to 15		µs
Static Control Error	$\frac{\Delta t}{\Delta t_d}$	Note 8			0.5	%
Output Current During Flyback Pulse (Peak Value)	I_4			±0.7		mA
Overall Phase Relation						
Phase Relation Between Leading Edge of Sync Pulse and Middle of Flyback Pulse	t	Note 9		4.9		µs
Tolerance of Phase Relation (TBA920)	$\lvert\Delta t\rvert$	Note 10			1.0	µs
*Tolerance of Phase Relation (TBA920S)	$\lvert\Delta t\rvert$				0.4	µs
Voltage for t_2 = 12 to 32 µs	V_{3-16}			6 to 8		V
Adjustment Sensitivity	$\frac{\Delta t_2}{\Delta V_{3-16}}$			10		µs/V
Input Current	I_3				2.0	µA
External Switch Over of Parameters (Loop Filter and Loop Gain) of Control Loop I (e.g. for Video Recorder Application) See Note 11						
Required Switch Over Voltage	V_{10-16}	R_{11-16} = 150 Ω	4.5			V
	V_{10-16}	R_{11-16} = 2.0 kΩ			2.0	V
Required Switch Over Current	I_{10}	R_{11-16} = 150 Ω, V_{10-16} = 4.5 V (Note 11)		80		µA
	I_{10}	R_{11-16} = 2.0 kΩ, V_{10-16} = 2.0 V (Note 11)		120		µA

NOTES:
1. 800 mW permissible while tubes are heating up.
2. Depends on switch position and polarity output current. R_{2-16} = 2.5 Ω is valid for V_{2-16} = +10.5 V and a load between leads 2 and 16 (e.g. an external resistor).
3. The output pulse duration is adjusted by shifting the leading edge (V_{3-16} from 6.0 V to 8.0 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.

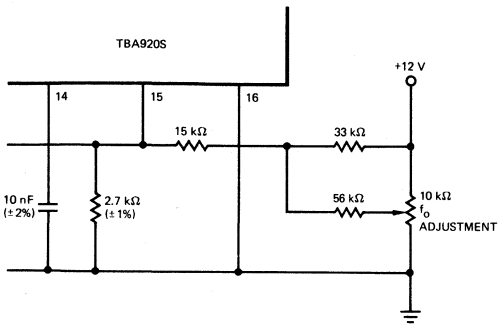
   For a line output stage with BU108 high voltage transistor the resulting duration is about 22 µs, and in such a way that the line output transistor is switched on again about 8.0 µs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.
4. The oscillator frequency can be changed for other TV standards by an appropriate value of C_{14-16}.
5. Exclusive external components tolerances.
6. Adjustable with R_{12-15}.
7. See application information circuit.
8. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
9. This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black and white sets), then the phase relation is achieved at C_{5-16} = 560 pF.
10. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at lead 2 occurs automatically by the control loop II or by applying a dc voltage to lead 3.
11. With sync pulses at lead 7 and 8; without RC network at lead 10.

10

TEST CIRCUITS

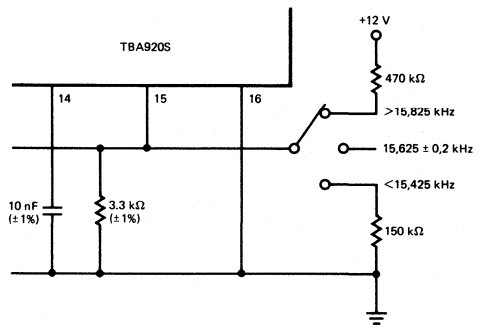
TBA920S

(See application circuit for balance of circuitry)



Frequency adjustment range. Test circuit for TBA920S.

Fig. 1

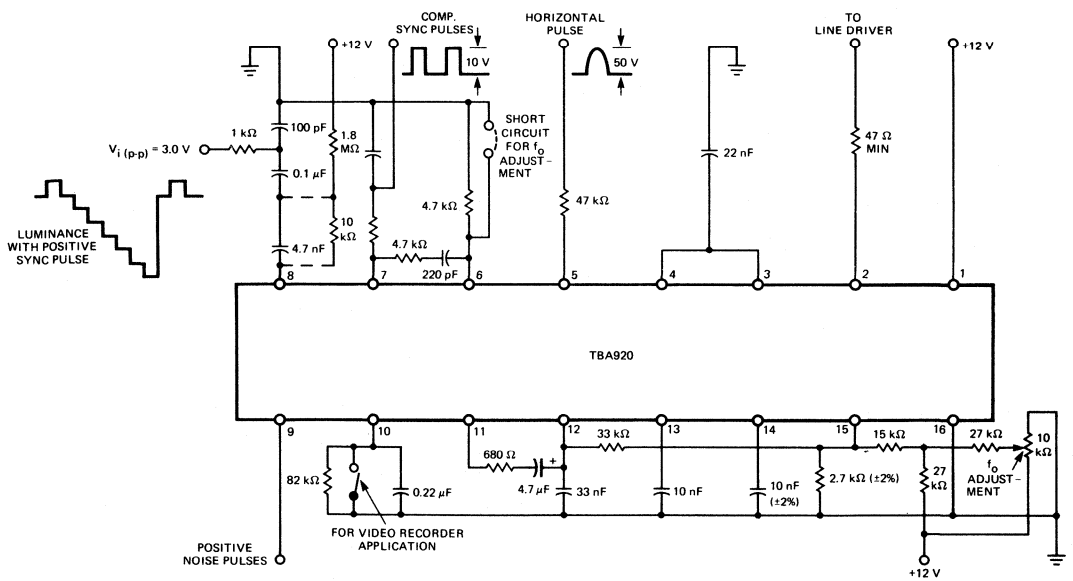


Other circuit possibilities for oscillator frequency adjustment.

Fig. 2

APPLICATION

(See Fig. 1 for TBA920S network)



TBA970

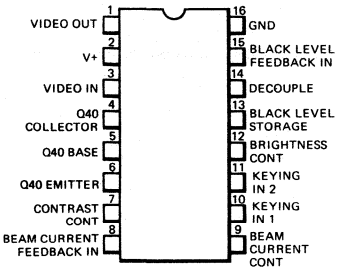
TELEVISION VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA970 is a monolithic video amplifier for television receivers. It is constructed using the Fairchild Planar* epitaxial process. The circuitry includes a video preamplifier, dc contrast control utilizing a linear potentiometer which can be ganged to the chroma gain control, beam current limiting via contrast. Beam current limiting could be obtained with either positive or negative control voltage. Black level control is achieved by a clamped feedback circuit combined with the brightness control. Emitter follower output could be used to directly drive the video output stage. A separate NPN transistor (Q40) is provided on the chip.

- **DC CONTRAST CONTROL**
- **DC BRIGHTNESS CONTROL**
- **BLACK LEVEL CLAMPING**
- **BEAM CURRENT LIMITING**
- **LOW IMPEDANCE OUTPUT**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

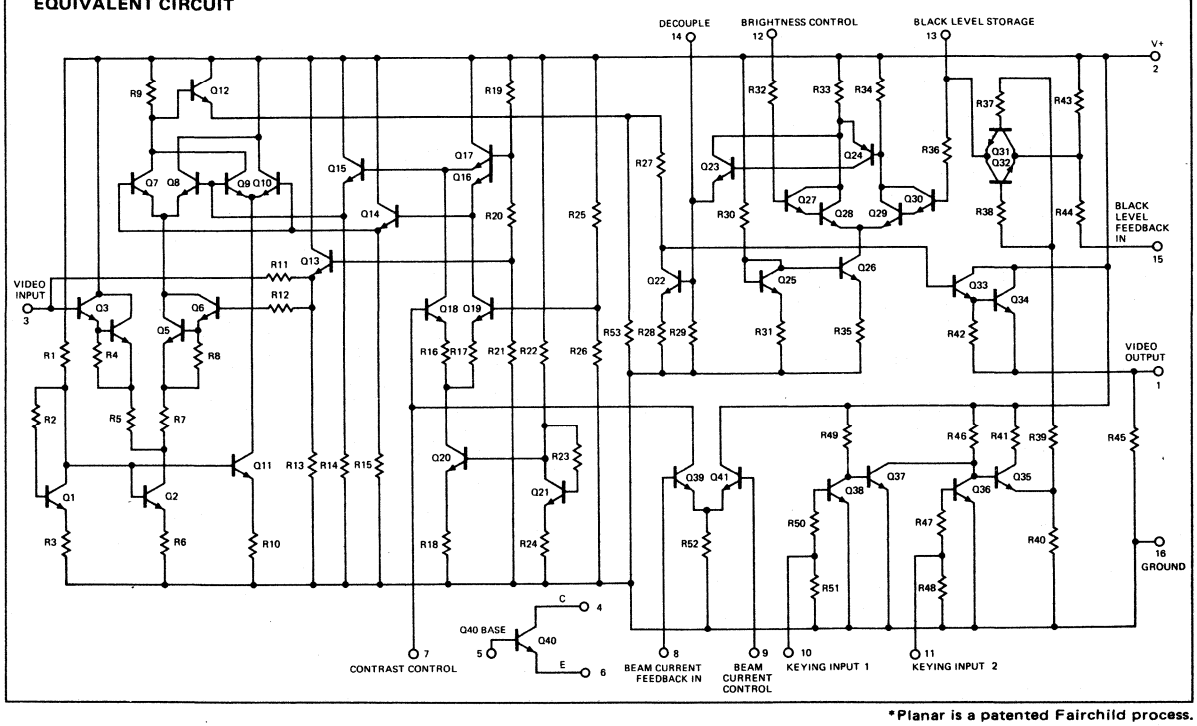
TYPE	PART NO.
970	TBA970
(970Q)	(TBA970Q)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15.5 V
Internal Power Dissipation	750 mW
Collector Current Q40	10 mA
Power Dissipation Q40	20 mW
V_{CEO} Q40	13.2 V
V_{CES} Q40	15.5 V
Operating Temperature Range	–20°C to +45°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



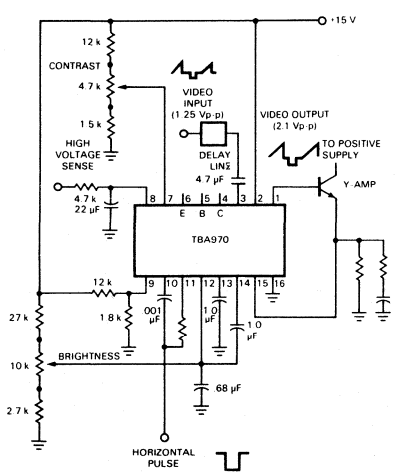
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 15 V, See Test Circuit, unless otherwise specified)

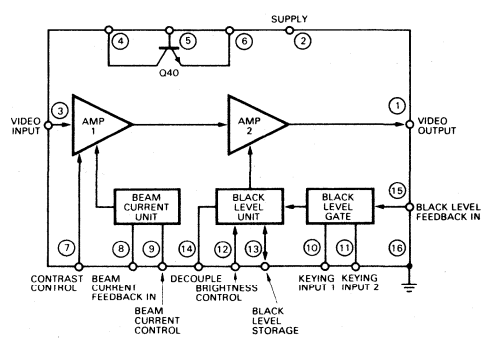
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_2)	(Note 1)		27	36	mA
Peak-to-Peak Input Voltage (V_3 p/p)	(Note 2)			1.6	Vp-p
Input Resistance (R_3)			12		kΩ
Voltage Gain			2.4		
3.0 dB Bandwidth			6.0		MHz
6.0 dB Bandwidth			9.0		MHz
Linearity of Black-to-White Video Output Signal		0.9			
Low Black Level Voltage (V_{15})				0.2	V
High Black Level Voltage (V_{15})		3.0			V
Contrast Control Range	1.5 V ≤ V_7 ≤ 4.5 V	36			dB
Input Resistance for Brightness Control (R12)			200		kΩ
Change of Black Level (ΔV_{15})	(Note 3)			20	mV
DC Voltage for Beam Current Limiting Inputs (V_8, V_9)	(Note 4)		2.0		V
Separate Transistor Q40 Gain	I_C = I_4 = 1.0 mA	40			

NOTES:
1. No input signal and at minimum brightness.
2. With negative going synchronizing pulse.
3. With constant brightness setting, due to change of picture content, contrast control setting and change in ambient temperature (ΔT_A = 20°C); black level clamping with t_c = 1 µs, I_{10} ≥ 0.25 mA, V_{11} ≤ 0.3 V.
4. Beam current limiting occurs at V_8 ≥ V_9.

TEST CIRCUIT



BLOCK DIAGRAM



TBA990

PAL TV CHROMA DEMODULATOR

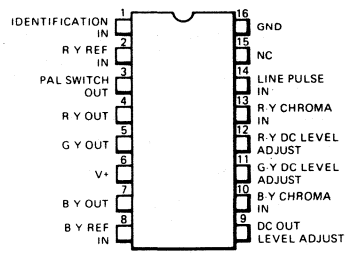
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA990 is an integrated color demodulator circuit for color television receivers incorporating two active synchronous demodulators for the R-Y and B-Y chrominance signals, a matrix (producing the G-Y color difference signal), PAL phase switch and flip-flop. It is suitable for dc coupled drive to the picture tube. When associated with the matrix integrated circuit (TBA530) it provides RGB output signals.

Special attention has been given in the design to minimizing dc level drift with temperature and direct interface with TBA530, TBA540 and TBA560. It is constructed on a single silicon chip using the Fairchild Planar* process.

- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **INTERNAL PAL SWITCH**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**
- **MINIMIZED DC LEVEL DRIFT WITH TEMPERATURE**
- **SIMULTANEOUS DC ADJUSTMENT ON CHROMA OUTPUTS**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

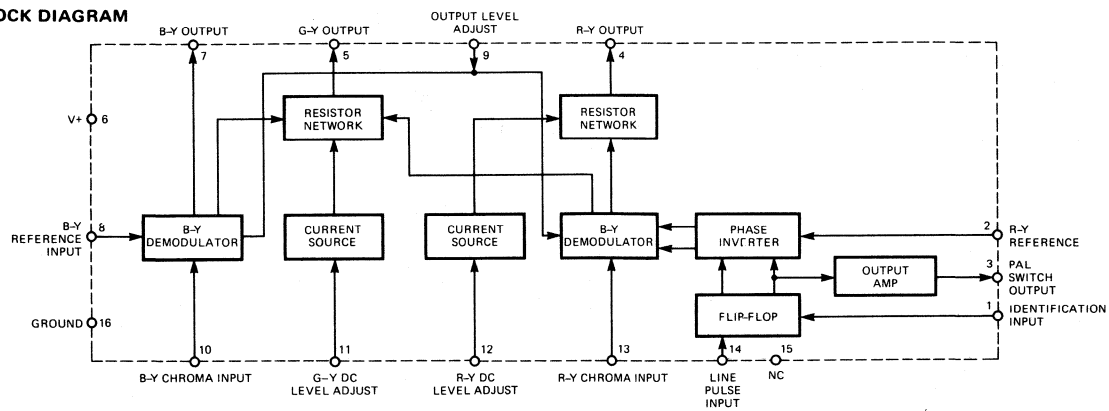
TYPE	PART NO.
990	TBA990
990Q	TBA990Q†

†Not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Internal Power Dissipation	300 mW
Operating Ambient Temperature	−20°C to +60°C
Storage Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM



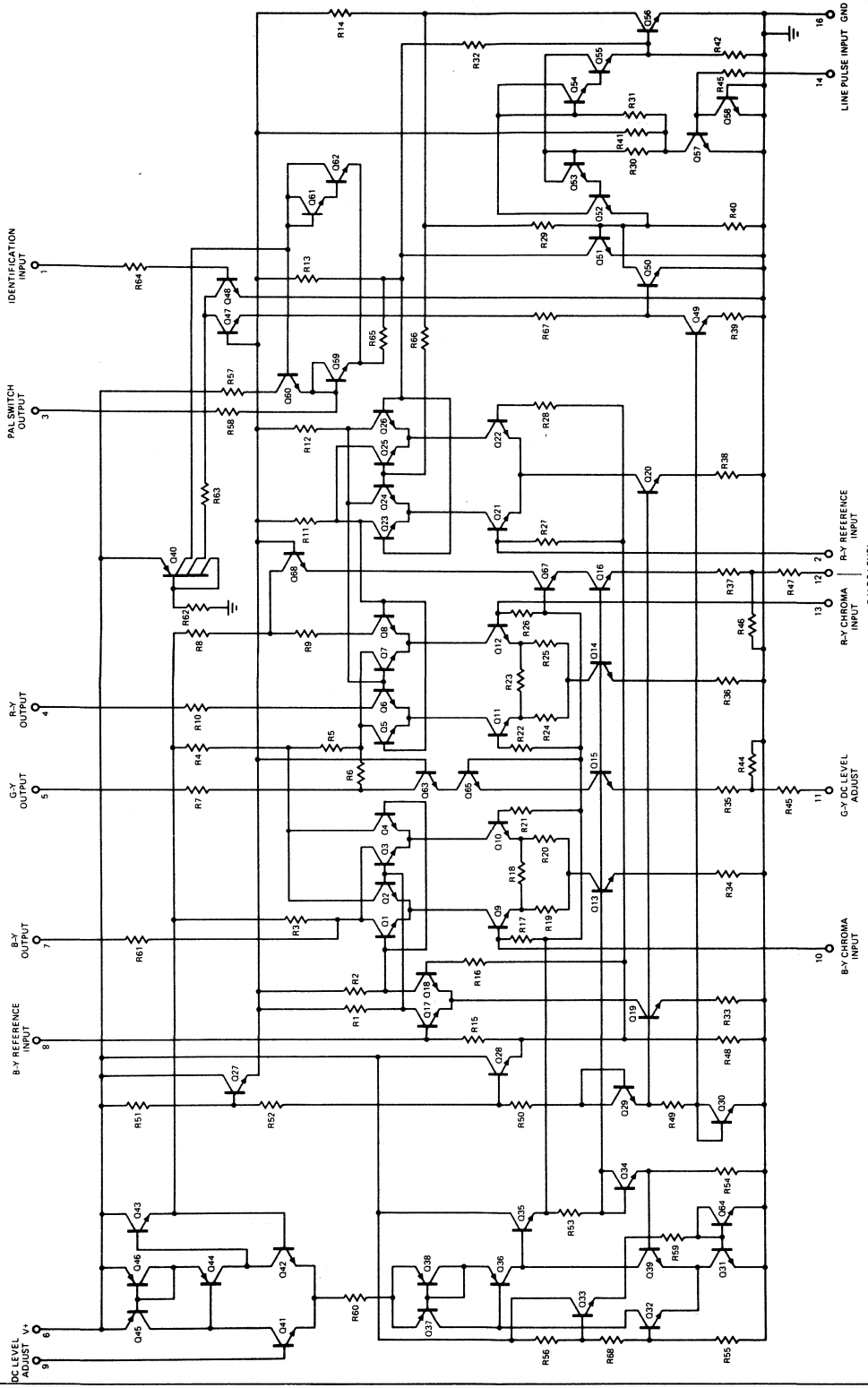
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12 V, see test circuit, unless otherwise specified)

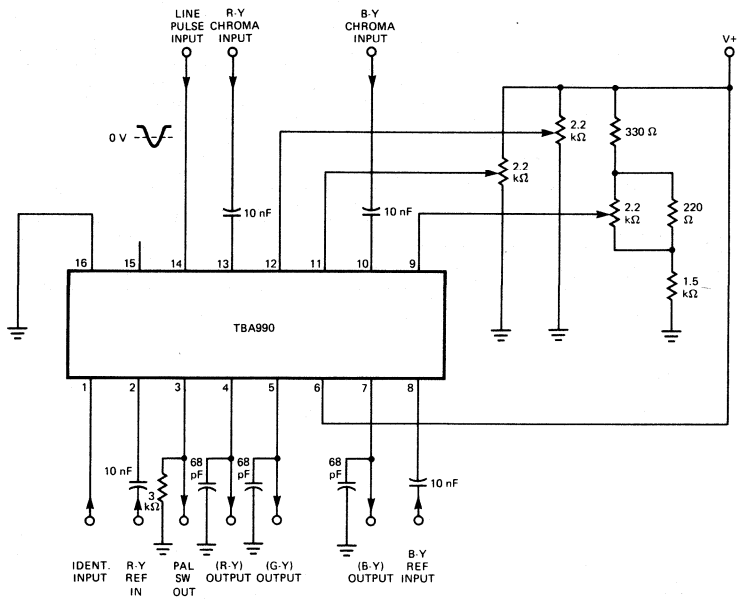
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			17		mA
Color Difference Gain					
R-Y Channel ($A_{V4/13}$)	$V_{10} = V_{13}$ = 50 mV pk-pk		3.8		V/V
B-Y Channel ($A_{V7/10}$)	f = 4.4 MHz		6.8		V/V
G-Y Channel	(Note 3)		(Note 1)		
Maximum Color Difference Output Voltage (Notes 2, 3)					
R-Y Output (V_4 pk-pk)	(Notes 2, 3)	1.6			V_{pk-pk}
B-Y Output (V_7 pk-pk)		2.0			V_{pk-pk}
G-Y Output (V_5 pk-pk)		0.9			V_{pk-pk}
Color Difference DC Output Voltage					
R-Y Output (V_4)			7.5		V
B-Y Output (V_7)			7.5		V
G-Y Output (V_5)			7.5		V
Input Resistance of Chroma Inputs (R10, R13)	$V_{10} = V_{13}$ = 20 mV rms (Sinusoidal) f = 4.4 MHz	800			Ω
Input Capacitance of Chroma Inputs (C10, C13)				10	pF
Output Resistance at Color Difference Terminals (R4, R5, R7)			3.0		kΩ
Input Resistance of Reference Inputs (R2, R8)			5.0		kΩ
Peak-to-Peak PAL Switch Output Voltage ($V_{3\ pk-pk}$)	(Note 4)		3.5		V_{pk-pk}
Activation Threshold Voltage (V_1)	Identification Circuit is Active	6.5			V
Deactivation Threshold Voltage (V_1)	Identification Circuit is Inactive			5.5	V
Identification Input Current (I_1)		−100			μA
Output Voltage Drift (ΔT_A = 40°C)					
DC Output Voltage (V_4)	$V_{11} = V_{12}$ = 6 V	−50		+50	mV
DC Output Voltage (V_7)		−50		+50	mV
DC Output Voltage (V_5)		−50		+50	mV
Relative DC Output Voltage Change between Channels		−20		+20	mV

NOTES:
1. G-Y output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
2. Increase V_{10} and V_{13} until gain is equal to 0.7 of small signal gain.
3. Reference input ($V_{2\,pk-pk}$ and $V_{8\,pk-pk}$) range is 0.5 V to 2.0 V. (typically 1.0 V).
4. f_o = 0.5 x line pulse frequency; V_{14} = 2.0 to 5.0 V_{pk-pk} (See application information).

EQUIVALENT CIRCUIT – TBA990



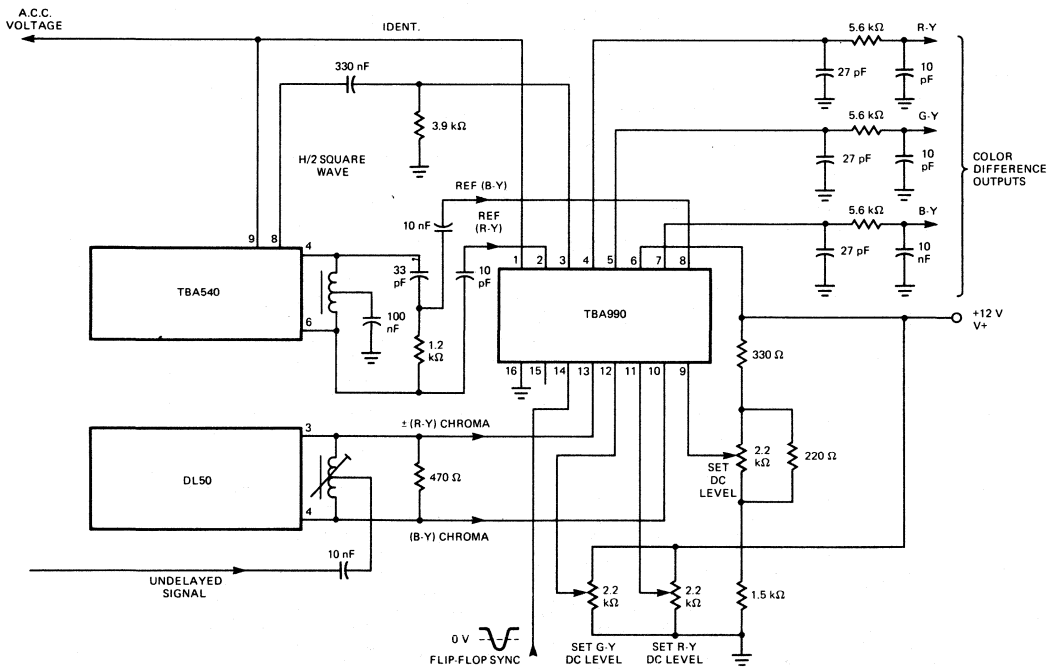
TEST CIRCUIT



$V_{11} = V_{12} = 6.0$ V

$V_9 = 9.5$ V

APPLICATION INFORMATION



APPLICATION INFORMATION (Cont'd)

The function is quoted against the corresponding lead number.

IDENTIFICATION BIAS

1. The PAL flip-flop is stopped, for identification purposes, when the voltage on pin 1 increases above 6 V. This threshold is internally generated and has a proportional behavior with the 12 V supply voltage. The threshold level of 6 V is chosen to match the output characteristic of the TBA540 and has sufficiently high safety margin above the zero chroma signal level of 4 V to eliminate spurious identifying.

R-Y SUBCARRIER REFERENCE INPUT

2. A 1 V pk-pk signal is required via a dc blocking capacitor. Under no circumstances should this signal be less than 0.5 V pk-pk. The input resistance at this pin is typically 5 kΩ.

PAL SQUARE WAVE CIRCUIT

3. The amplitude is 3.5 V pk-pk from an emitter follower.

R-Y SIGNAL OUTPUT (G-Y at pin 5 and B-Y at pin 7)

4. These outputs require no external dc loads except that direct connection must be made via the low pass filter to the appropriate pins on the RGB matrix TBA530.

   The signals produced are in the following ratios:

   $V_{B-Y} = 1.78\ V_{R-Y}$

   (a) $V_{G-Y} = 0.85\ V_{R-Y}$

   (b) $V_{G-Y} = 0.17\ V_{R-Y}$

   Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix.

   Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

   The dc levels should each be adjusted, starting with the (B-Y), to +7.5 V at nominal supply voltage. However, in a complete circuit using the TBA530 matrix and feedback integrated circuit these dc levels will be adjusted to give the correct setting of the picture tube drive black levels. The changes in dc level with supply voltage are approximately linear and track together.

   The unwanted products of demodulation occurring in the color difference outputs are chiefly 8.86 MHz and harmonics together with a small amount of 4.43 MHz due to possible unbalance in the demodulators. To avoid possible troubles in the receiver because of the radiation of these demodulation products from the RGB drive circuits, filters must be employed in each of the color-difference outputs from the TBA990. The roll-off should begin at about 1.5 MHz and attention should be given to the parallel resonance of the inductors to ensure that no serious attenuation will occur at less than 1.5 MHz. Also, some advantage may be secured by designing the inductor so that the dip due to its self-resonance occurs at about 4.43 MHz.

G-Y SIGNAL OUTPUT

5. See pin 4.

POSITIVE SUPPLY

6. The maximum allowable voltage on this pin is 13.2 V.

B-Y SIGNAL OUTPUT

7. See pin 4.

B-Y SUBCARRIER REFERENCE INPUT

8. The requirements here are identical with those for pin 2.

DC LEVEL SETTING FOR B-Y OUTPUT SIGNAL

9. See test circuit diagram, and also pin 4.

CHROMINANCE B-Y INPUT SIGNAL

10. An input signal of approximately 360 mV pk-pk (color bars) is required at this pin. The input impedance is greater than 800 Ω and the input capacitance is less than 10 pF.

DC LEVEL SETTING FOR G-Y OUTPUT SIGNAL

11. See test circuit diagram, and also pin 5.

DC LEVEL SETTING FOR R-Y OUTPUT SIGNAL

12. See test circuit diagram, and also pin 4.

CHROMINANCE R-Y INPUT SIGNAL

13. An input signal of approximately 500 mV pk-pk (color bars) is required at this pin. The input imedpance is the same as for pin 10.

LINE PULSE INPUT (flip-flop synchronizing)

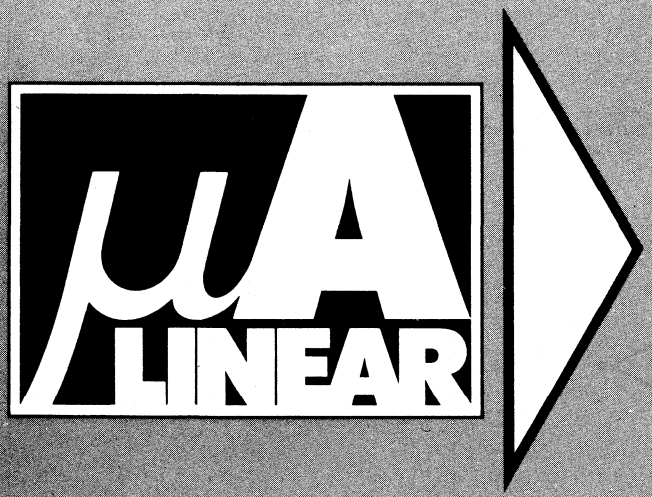
14. A waveform derived from the line timebase can be used for synchronizing providing that its amplitude lies between 2 V and 5 V pk-pk. The trigger point occurs where the negative going edge crosses approximately +0.6 V.

NOT CONNECTED

15. This pin should not be used for external connections.

GROUND

16. See pin 16.



CONSUMER –
NEW PRODUCTS TO BE ANNOUNCED

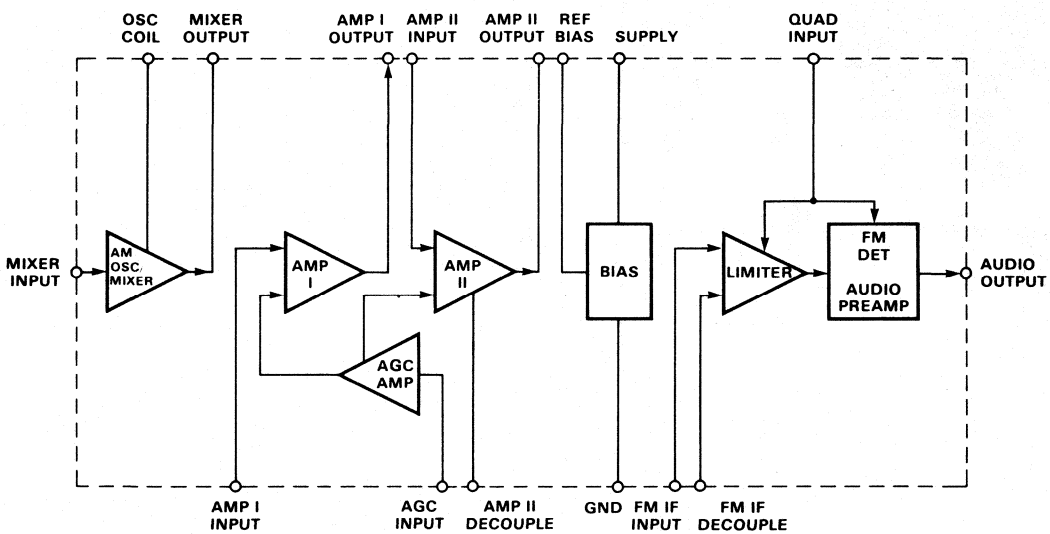
μA721

AM/FM IF SUBSYSTEM

The μA721 is a complete AM/FM IF subsystem. It provides AM conversion, AM RF and IF amplification with a wide range of AGC capability; FM IF amplification and the FM detection. The device is extremely versatile; it can be used in many applications including hi-fi radios, table radios, portable radios and car radios.

- **WIDE OPERATING VOLTAGE RANGE 3.5 V TO 16 V**
- **FEW EXTERNAL COMPONENTS**
- **SINGLE TUNED FM DETECTOR COIL**
- **LOW CURRENT DRAIN**

BLOCK DIAGRAM



μA1314
CBS SQ* LOGIC CIRCUIT

The μA1314 is a gain control and balance adjustment device for use with the CBS SQ™ system decoders. It consists of four amplifiers with the gain of each being adjustable by varying a dc voltage. With four variable resistors, the master volume and LF/RF, LB/RB, and F/B balance may be controlled.

The unit also has inputs which may be connected to the μA1315 logic enhancement device to provide increased front to back separation. This feature is highly desirable in high performance four channel stereo systems.

- **DC CONTROLLED GAIN**
- **FOUR SEPARATE AUDIO PREAMPLIFIERS**
- **COMPATIBLE WITH THE μA1312 DECODER AND THE μA1315 LOGIC ENHANCEMENT DEVICE**

μA1315
CBS SQ* LOGIC CIRCUIT

The μA1315 provides the basic logic function for enhancing the front to back separation in the CBS SQ™ four channel decoding system. The device is designed to interface with the μA1312 decoder and μA1314 balance control. The μA1315 provides variable logic enhancement control signals to the μA1314.

This device extends the performance of the basic SQ™ system to the levels desired for top of the line systems.

- **PROVIDES LOGIC ENHANCEMENT TO EXTEND FRONT TO BACK SEPARATION TO 12 dB AND AN OVERALL SYSTEM FRONT TO BACK SEPARATION OF 18 dB**
- **LOW EXTERNAL PARTS COUNT**
- **PROVISIONS FOR ENHANCEMENT CONTROLS**
- **PROVIDES DC GAIN CONTROL SIGNALS TO THE μA1314**

*Trademark of CBS Inc.

µA1391/94

TV HORIZONTAL PROCESSOR

The µA1391/1394 TV Horizontal Processor includes phase detector, horizontal oscillator, and pre-driver functions on one chip, and is offered in a 8-lead mini DIP. The device provides the entire low level horizontal signal processing function and may be used with either transistor or vacuum tube output stages.

- **INTERNAL SHUNT REGULATOR**
- **PRESET HOLD CONTROL CAPABILITY**
- **± 300 Hz TYPICAL PULL IN RANGE**
- **BALANCED PHASE DETECTOR**
- **VARIABLE OUTPUT DUTY CYCLE FOR DRIVING TUBE OR TRANSISTOR**
- **LOW THERMAL FREQUENCY DRIFT**
- **SMALL STATIC PHASE ERROR**

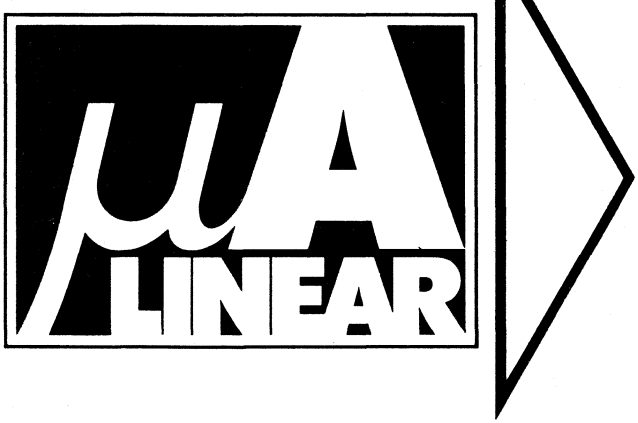
TBA800

5 WATT AUDIO POWER AMPLIFIER

The TBA800 is an integrated monolithic IC in a plastic 12-lead power package. The external cooling tabs enable 2.5 W output power to be achieved without external heat sink and 5 W output power using a small area of the PC board copper as a heat sink. This audio power amplifier is intended to be used as a class B audio amplifier.

The TBA800 provides a 5 W output power at 24 V/16 Ω and works with a wide range of supply voltages (5–30 V). It gives high output current (up to 1.5 A), high efficiency (70% at 4 W), very low harmonic distortion and no crossover distortion.

- **12-LEAD POWER PACKAGE**
- **WIDE RANGE OF SUPPLY VOLTAGES (5–30 V)**
- **HIGH EFFICIENCY**
- **LOW DISTORTION**



INDEX

INDEX

μA8T13
DUAL SINGLE-ENDED LINE DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 8T13 Dual Line Driver is designed for driving 50 Ω to 500 Ω coaxial cable, strip line, or twisted pair transmission lines. All inputs are TTL or DTL compatible and the emitter-follower outputs enable two or more drivers to operate on the same line in party line applications.

For a dual line driver to meet the IBM System/360 I/O Interface Specification, see 8T23 data sheet.

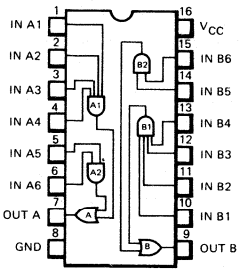
- **HIGH OUTPUT DRIVE CAPABILITY**
- **HIGH SPEED**
- **INPUT CLAMP DIODES**
- **SINGLE 5 V SUPPLY OPERATION**
- **SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Lead Temperatures	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	730 mW

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. For Hermetic DIP and Molded DIP rating applies to ambient temperatures up to 65°C, above 65°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 45°C.

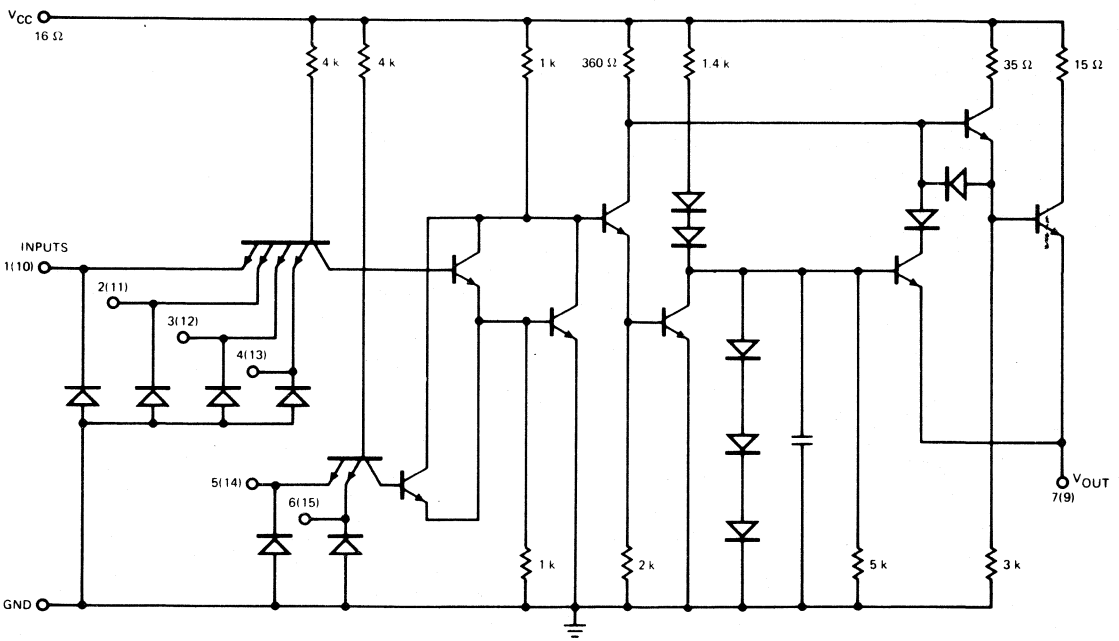
CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
μA8T13	μA8T13DM
μA8T13	μA8T13FM
μA8T13	μA8T13DC
μA8T13	μA8T13PC

EQUIVALENT CIRCUIT (FOR EACH DRIVER)



ELECTRICAL CHARACTERISTICS FOR μA8T13 (V_{CC} = 5.0 V ±5%, T_A = −55°C to +125°C (Note 3)

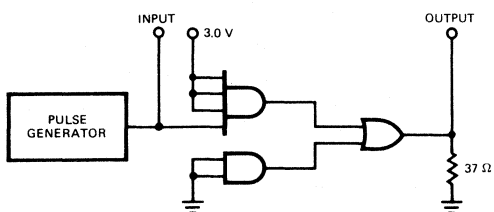
SYMBOL	PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
		AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN	TYP	MAX	
		INPUT UNDER TEST	OTHER INPUTS							
V_{OH}	Output HIGH Voltage	2.0 V	2.0 V	0.8 V	−75 mA	9	2.4			V
I_{OH}	Output HIGH Leakage Current	0 V	0 V	0 V	3.0 V	10			500	μA
I_{OL}	Output LOW Leakage Current	0.8 V	4.5 V	0 V	0.4 V				−800	μA
I_{IL}	Input LOW Current	0.4 V	4.5 V				−0.1		−1.6	mA
I_{IH}	Input HIGH Current	4.5 V	0 V						40	μA

ELECTRICAL CHARACTERISTICS FOR μA8T13DM AND μA8T13DC (V_{CC} = 5.0 V ±5 %, T_A = 25°C)

SYMBOL	PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
		AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN	TYP	MAX	
		INPUT UNDER TEST	OTHER INPUTS							
t_{PLH}	Turn On Delay See AC Test Circuit					11, 15			20	ns
						12, 15		32		ns
t_{PHL}	Turn Off Delay See AC Test Circuit					11, 15			20	ns
						12, 15		22		ns
P_D/I_{CC}	Power/Current Consumption: Output LOW	0.8 V	0.8 V	0.8 V		14, 17			315/60	mW/mA
	Output HIGH	2.0 V	2.0 V	2.0 V		14, 17			150/28	mW/mA
V_L	Input Latch Voltage	10 mA	0 V	0 V		13	5.5			V
I_{OH}	Output HIGH Current	4.5 V	4.5 V	0 V	2.0 V	16	−100		−250	mA
I_{SC}	Output Short Circuit Current	4.5 V	4.5 V	0 V	0 V	16			−30	mA
V_{CD}	Input Clamp Diode Voltage	−12 mA							−1.5	V

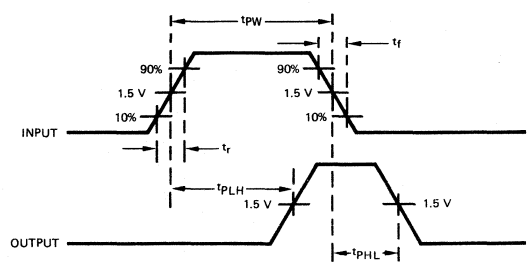
NOTES:
3. Specifications apply V_{CC} = 5.0 V ±5% and 0°C to 70°C for μA8T13.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. All measurements are taken with ground pin tied to zero volts.
6. Positive current is defined as into the terminal referenced.
7. Positive logic definition: "UP" Level = HIGH, "DOWN" Level = LOW.
8. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
9. Output source current is supplied through a resistor to ground.
10. With forced output voltage of 3 V no more than 500 μA will enter the driver when output is in LOW state. V_{CC} = 0 V.
11. R_L = 37Ω to ground.
12. Load is 37 Ω in parallel with 1000 pF.
13. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
14. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition.
15. Reference ac Test Figure and Pulse Requirements.
16. Reference "Typical Output Current as a function of Output Voltage Curve."
17. V_{CC} = 5.25 V. Power Consumption specified for both drivers in package.

AC TEST CIRCUIT



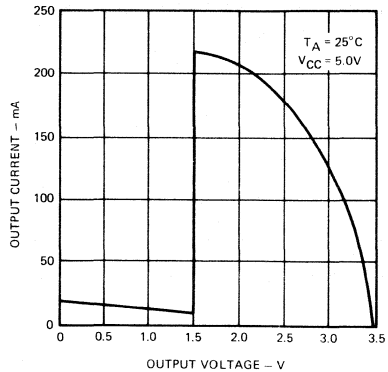
INPUT PULSE:
Amplitude = 3.0 V
t_{PW} = 40 ns (50% Duty Cycle)
$t_r = t_f \leq 5$ ns (10% and 90% measurement points)

VOLTAGE WAVEFORMS



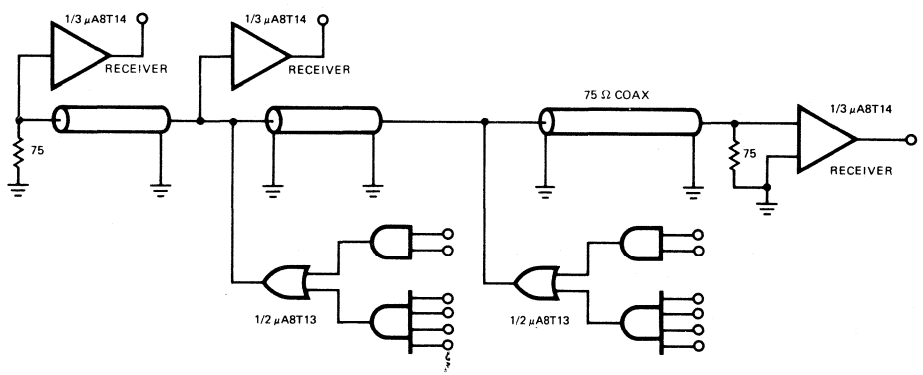
TYPICAL PERFORMANCE CURVE

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



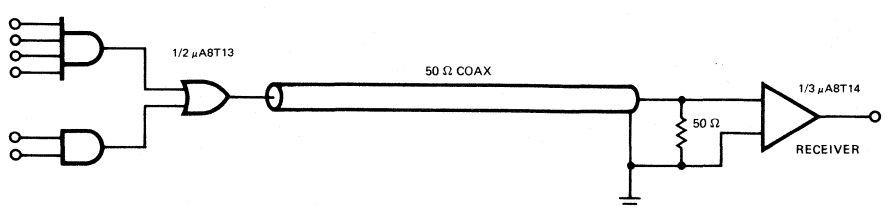
TYPICAL APPLICATIONS

75 Ω PARTY LINE (2 DRIVERS, 3 RECEIVERS)



Note: For party line operation, termination of each physical end of the line is recommended.

SIMPLEX OPERATION (1 DRIVER)



Note: For simplex operation, the line should be terminated only at the distant receiver site.

11

μA8T14
TRIPLE LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 8T14 Triple Line Receiver is designed to receive digital information from coaxial cable, strip line, or twisted pair single ended transmission lines. High input impedance (≈30kΩ) presents minimal loading to the transmission lines in multiple receiver applications. The 8T14 has built in hysteresis which makes it ideal for such applications as Schmitt triggers, one-shots, and oscillators. Use the 8T24 triple line receiver where IBM System/360 I/O Interface Specification must be met.

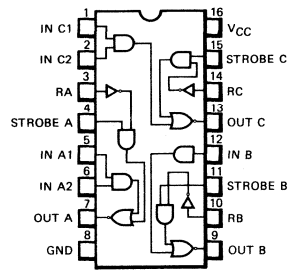
- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5V SUPPLY OPERATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Lead Temperatures	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	730 mW

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. For Hermetic DIP and Molded DIP rating applies to ambient temperatures up to 65°C, above 65°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 45°C.

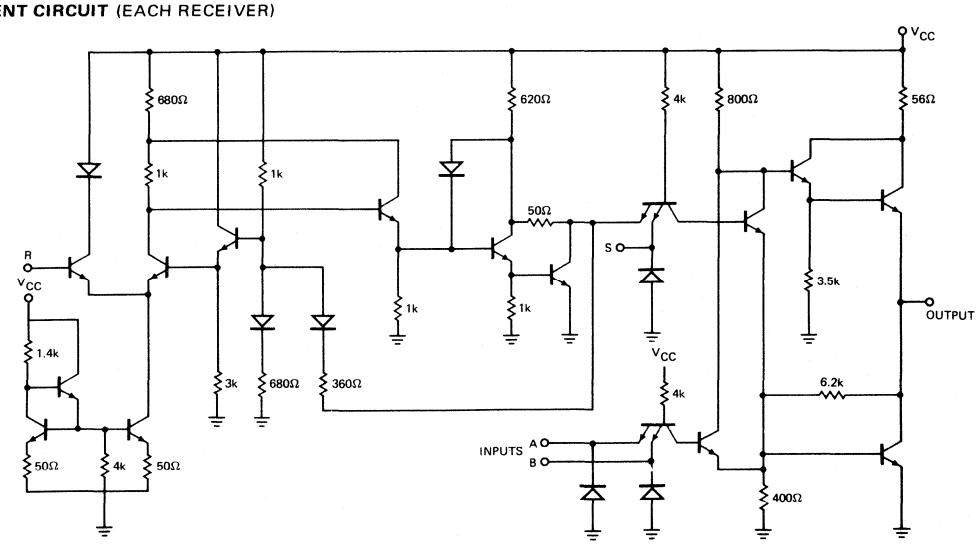
CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
μA8T14	μA8T14DM
μA8T14	μA8T14FM
μA8T14	μA8T14DC
μA8T14	μA8T14PC

EQUIVALENT CIRCUIT (EACH RECEIVER)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%; −55°C ≤ T_A ≤ +125°C for μA8T14DM (Note 3)

SYMBOL	PARAMETER		R	TEST CONDITIONS STROBE	1	2	OUTPUTS	NOTES	LIMITS MIN	TYP	MAX	UNITS
V_{OH}	Output HIGH Voltage		2.0 V	4.5 V	0 V	0 V	−800 μA	10, 16	2.6	3.5		V
			0 V	0.8 V	0 V	0 V	−800 μA	10, 16	2.6	3.5		V
V_{OL}	Output LOW Voltage		0.8 V	2.0 V	0 V	0 V	16 mA	11, 15			0.4	V
			0 V	0 V	2.0 V	2.0 V	16 mA	11, 15			0.4	V
I_{IL}	Input LOW Current	Strobe	0 V	0.4 V					−0.1		−1.6	mA
		N_A	0 V		0.4 V				−0.1		−1.6	mA
		N_B				0.4 V			−0.1		−1.6	mA
I_{IH}	Input HIGH Current	R	3.8 V								0.17	mA
		Strobe	3.8 V	4.5 V							40	μA
		N_A			4.5 V	0 V					40	μA
		N_B			0 V	4.5 V					40	μA
ΔV_{IN}	Hysteresis			4.5 V	0 V	0 V		13, 14	0.30	0.50		V

NOTE

3. Specifications apply from 0°C to 70°C for μA8T14DC, μA8T14PC.

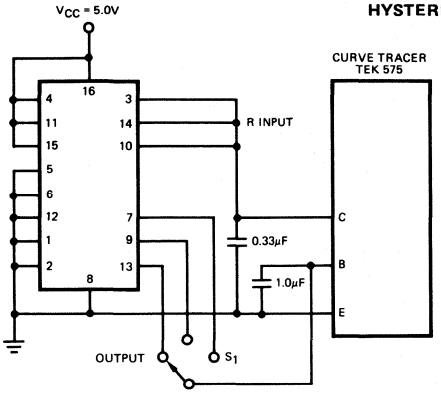
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

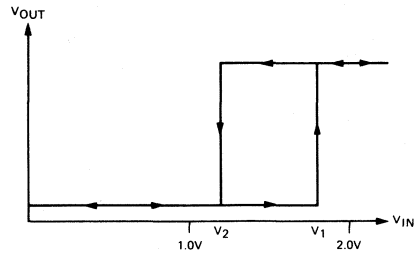
SYMBOL	PARAMETER		R	TEST CONDITIONS STROBE	1	2	OUTPUTS	NOTES	LIMITS MIN	TYP	MAX	UNITS
t_{PLH}	Turn-on Propagation Delay		V_{IN}	5.0 V	0 V	0 V		18		20	30	ns
t_{PHL}	Turn-off Propagation Delay		V_{IN}	5.0 V	0 V	0 V		18		20	30	ns
PD	Power/Current Consumption									315/60	380/72	mW/mA
V_{IN}	Input Voltage Rating	Strobe	3.8 V	10 mA	0 V	0 V			5.5			V
		N_A	0 V	0 V	10 mA	0 V			5.5			V
		N_B	0 V	0 V	0 V	10 mA			5.5			V
I_{SC}	Output Short-Circuit Current		3.8 V	0 V	0 V	0 V	0 V		−50		−100	mA
V_{CD}	Input Clamp Voltage	Strobe		−12 mA							−1.5	V
		N_A			−12 mA						−1.5	V
		N_B				−12 mA					−1.5	V

NOTES

4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. All measurements are taken with ground pin tied to zero volts.
6. Positive current is defined as into the terminal referenced.
7. Positive current flow is defined as into the terminal referenced.
8. Positive Logic Definition: "UP" Level = "HIGH"; "DOWN" Level = "LOW".
9. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the clamp diodes on the S, A, and B inputs become forward biased.
10. Output source current is supplied through a resistor to ground.
11. Output sink current is supplied through a resistor to V_{CC}.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Hysteresis is defined as voltage difference between R input level at which output begins to go from LOW to HIGH state and level at which output begins to go from HIGH to LOW.
14. V_{CC} = 5.0 V.
15. Previous condition is a HIGH output state.
16. Previous condition is a LOW output state.
17. V_{CC} = 5.25 V.
18. Measured as time delay from R input going through 1.5V to the output going through 1.5V. (See 8T24 data sheet ac test circuit).

HYSTERESIS TEST CIRCUIT





Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

1. V_1 and V_2 must be between 0.8V minimum and 2.0V maximum.
2. Hysteresis = $V_1 - V_2 \geq 0.3V$.

Fig. 1 **Fig. 2**

APPLICATIONS

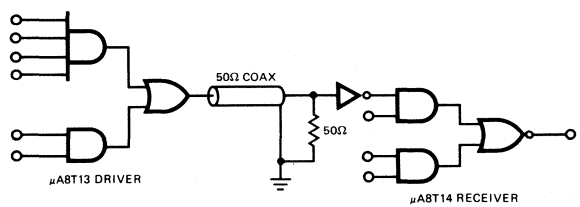
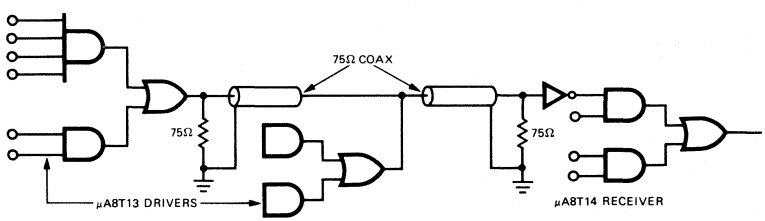


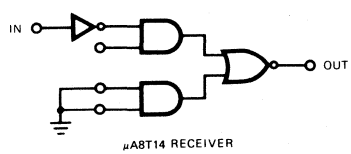
Fig. 3



If more than one driver/receiver pair is to be used on each transmission line, the line should be terminated at both ends as shown in Fig. 4

Fig. 4

SCHMITT TRIGGER APPLICATION



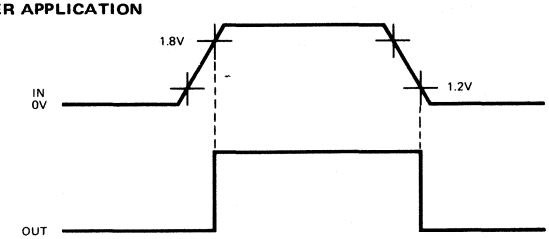


Fig. 5

μA8T23
DUAL SINGLE-ENDED LINE DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 8T23 Dual Line Driver is designed to meet the requirements of the IBM System/360 I/O Interface Specification for interface drivers. All inputs are TTL or DTL compatible. Logic has been incorporated to ensure that no spurious noise is generated on the transmission line during the power-up and power-down sequence. The outputs are protected from short circuits and have uncommitted emitter outputs which allows DOT-OR logic to be performed in party line data bus applications.

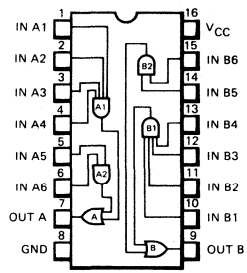
- **I_{OUT} = 59.3 mA AT 3.11 V**
- **UNCOMMITTED EMITTER OUTPUTS FOR PARTY LINE/WIRED-OR APPLICATIONS**
- **SHORT CIRCUIT PROTECTION**
- **SINGLE 5 V SUPPLY OPERATION**
- **AND-OR LOGIC CONFIGURATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperatures	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	730 mW

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 65°C Above 65°C derate linearly at 8.3 mW/°C.

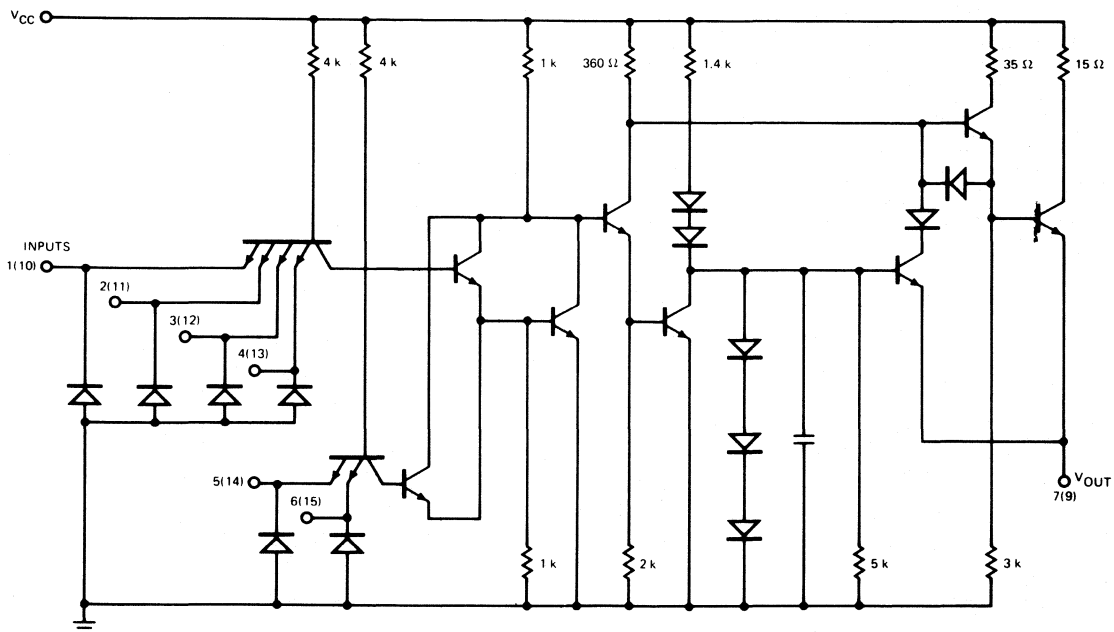
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA8T23	μA8T23DC
μA8T23	μA8T23PC

EQUIVALENT CIRCUIT (FOR EACH DRIVER)



ELECTRICAL CHARACTERISTICS FOR μA8T23 (V_{CC} = 5.0 V ±5%, T_A = 0°C to +70°C.)

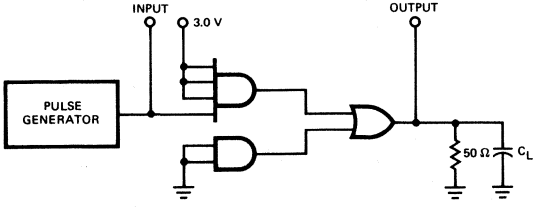
SYMBOL	PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
		AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN	TYP	MAX	
		INPUT UNDER TEST	OTHER INPUTS							
V_{OL}	Output LOW Voltage	0.8 V	4.5 V	0 V	−240 μA	9			+0.15	V
I_{OH}	Output HIGH Leakage Current	0 V	0 V	0 V	3.0 V	3, 16			40	μA
I_{IL}	Input LOW Current	0.4 V	4.5 V				−0.1		−1.6	mA
I_{IH}	Input HIGH Current	4.5 V	0 V						40	μA

ELECTRICAL CHARACTERISTICS FOR μA8T23 (V_{CC} = 5.0 V ±5 %, T_A = 25°C)

SYMBOL	PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
		AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN	TYP	MAX	
		INPUT UNDER TEST	OTHER INPUTS							
V_{OH}	Output HIGH Voltage	2.0 V	2.0 V	0.8 V	59.3 mA		3.11			V
t_{PLH}	Turn-On Delay (See ac test circuit)					10, 14		12	20	ns
						11, 14		15	25	ns
t_{PHL}	Turn-Off Delay (See ac test circuit)					10, 14		12	20	ns
						11, 14		20	35	ns
P_D/I_{CC}	Power/Current Consumption:									
	Output LOW	0.8 V	0.8 V	0.8 V		13, 17			315/60	mW/mA
	Output HIGH	2.0 V	2.0 V	2.0 V		13, 17			150/28	mW/mA
V_L	Input Latch Voltage	10 mA	0 V	0 V		12	5.5			V
I_{OH}	Output HIGH Current	4.5 V	4.5 V	0 V	2.0 V	15	−100		−250	mA
V_{CD}	Input Clamp Diode Voltage	−12 mA				15			−1.5	V

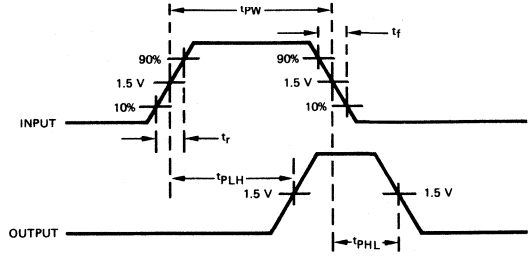
NOTES:
3. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
4. All measurements are taken with ground pin tied to zero volts.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: "UP" Level = HIGH, "DOWN" Level = LOW.
7. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
8. Output source current is supplied through a resistor to ground.
9. With forced output current of 240 μA the output voltage must not exceed 0.15 V.
10. R_L = 50 Ω to ground.
11. Load is 50 Ω in parallel with 100 pF.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. I_+ is dependent upon loading. I_+ limit specified is for no-load test condition for both drivers.
14. Reference ac Test Circuit and Pulse Requirements.
15. Reference "Typical Output Current as a function of Output Voltage Curve".
16. V_{CC} = 0 V.
17. V_{CC} = 5.25 V.

AC TEST CIRCUIT



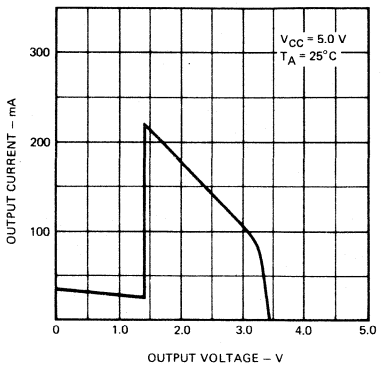
INPUT PULSE:
Amplitude = 3.0 V
t_{PW} = 50 ns (50% Duty Cycle)
$t_r = t_f \leq 5$ ns (10% and 90% measurement points)

WAVEFORMS

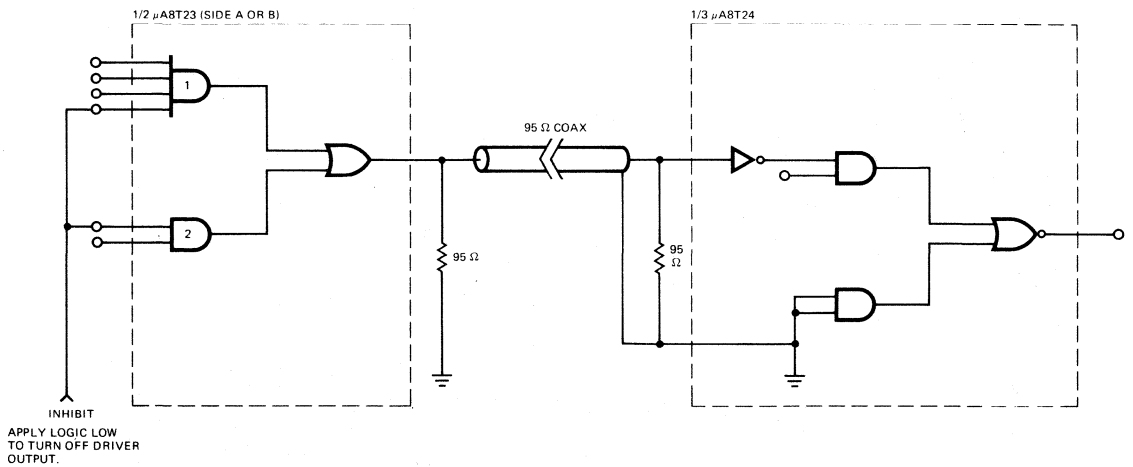


TYPICAL PERFORMANCE CURVE FOR μA8T23

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



TYPICAL APPLICATION



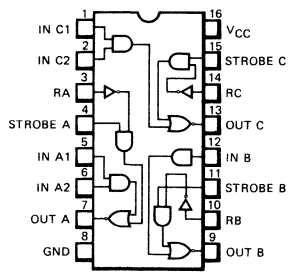
NOTE: To insure proper logic operation, unused inputs should not be left floating. Tie the unused inputs to V_+ through a current limit resistor (2.2kΩ).
To inhibit the driver, apply a logic LOW voltage to one input from gate 1 and 2 as shown above.

μA8T24
TRIPLE LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA8T24 Triple Line Receiver is designed specifically to meet the IBM System/360 I/O Interface Specification (File No. S360-19). The logic inputs (S, A, B) are fully TTL or DTL compatible. The R (Receive) input is designed to withstand a positive dc input of +7.0 V with power on (V_{CC} = 5.0 V) and +6.0 V with power off, (V_{CC} = 0 V) and a negative dc input of 0.15 V with power on or off. This protection allows normal bus operation even if one or more receivers have been powered down.

- **MEETS IBM SYSTEM/360 I/O INTERFACE SPECIFICATION**
- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5.0 V SUPPLY OPERATION**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



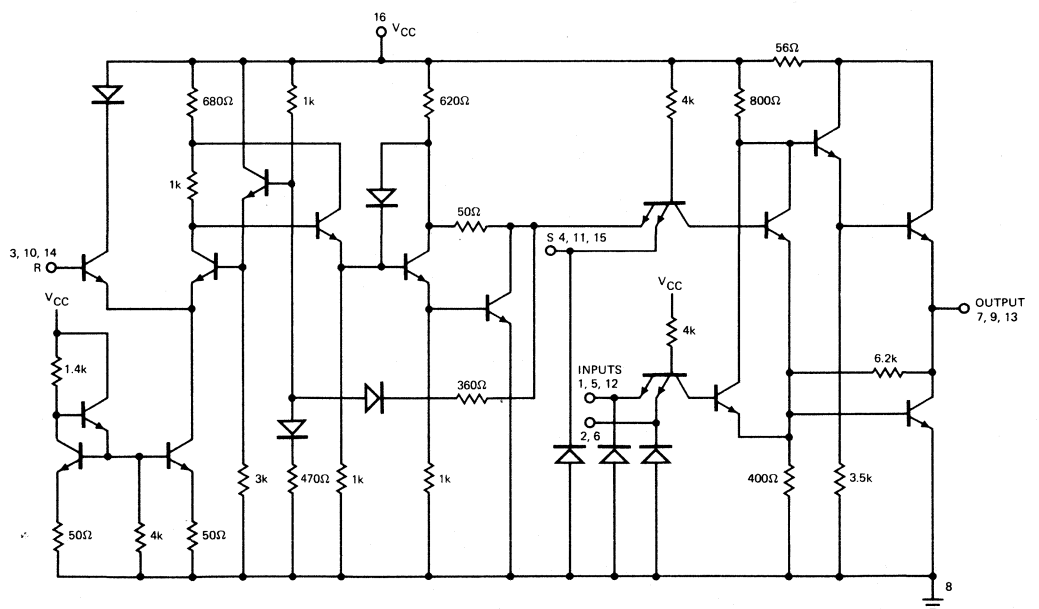
ORDER INFORMATION

TYPE	PART NO.
μA8T24	μA8T24DC
μA8T24	μA8T24PC

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperatures	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation	670 mW

EQUIVALENT CIRCUIT (EACH RECEIVER)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
			R	STROBE	1	2	OUTPUTS		MIN	TYP	MAX	
V_{OH}	Output HIGH Voltage		1.70 V	4.5 V	0 V	0 V	−800 μA	8	2.6	3.4		V
			0 V	0.7 V	0 V	0 V	−800 μA	8	2.6	3.4		V
V_{OL}	Output LOW Voltage		0.70 V	1.7 V	0 V	0 V	16 mA	9		0.2	0.4	V
			0 V	0 V	1.7 V	1.7 V	16 mA	9		0.2	0.4	V
I_{OL}	Input LOW Current	Strobe	0 V	0.4 V					−0.1		−1.6	mA
		N_A	0 V		0.4 V				−0.1		−1.6	mA
		N_B				0.4 V			−0.1		−1.6	mA
I_{IH}	Input HIGH Current	R	3.11 V								0.17	mA
		R	7.0 V								5.0	mA
		R	6.0 V					10			5.0	mA
		Strobe	3.11 V	4.5 V							40	μA
		N_A			4.5 V	0 V					40	μA
		N_B			0 V	4.5 V					40	μA

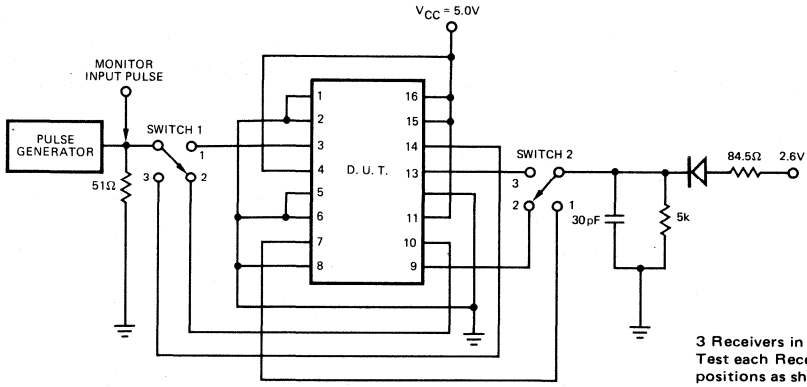
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

SYMBOL	PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
			R	STROBE	1	2	OUTPUTS		MIN	TYP	MAX	
t_{PHL}	Turn-on Propagation Delay		V_{IN}	5.0 V	0 V	0 V		14		20	30	ns
t_{PLH}	Turn-off Propagation Delay		V_{IN}	5.0 V	0 V	0 V		14		20	30	ns
ΔV_{IN}	Hysteresis		V_{IN}	4.5 V	0 V	0 V		12, 13	0.2	0.4		V
PD	Power/Consumption							15		315	380	mW
I_{CC}	Supply Current							15		60	72	mA
V_L	Input Latch Voltage	Strobe	3.11 V	10 mA	0 V	0 V		11	5.5			V
		N_A	0 V	0 V	10 mA	0 V		11	5.5			V
		N_B	0 V	0 V	0 V	10 mA		11	5.5			V
I_{OS}	Output Short Circuit Current		3.11 V	0 V	0 V	0 V			−50		−100	mA
V_{CD}	Input Clamp Diode Voltage	Strobe		−12 mA							−1.5	V
		N_A			−12 mA						−1.5	V
		N_B				−12 mA					−1.5	V

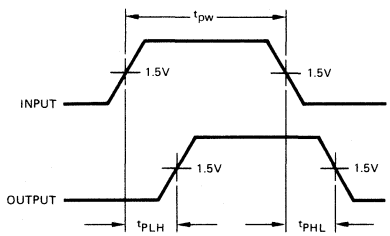
NOTES:

1. Voltages are with respect to ground (pin 8).
2. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
3. All measurements are taken with ground pin tied to zero volts.
4. Positive current is defined as into the terminal referenced.
5. Positive logic definition: "UP" Level = "HIGH", "DOWN" Level = "LOW".
6. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
7. Output source current is applied through a resistor to ground.
8. Output sink Current is supplied through a resistor to V_{CC}.
9. V_{CC} = 0.00V
10. This test guarantees operation free of Input latch up over the specified operating supply voltage range.
11. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "HIGH" to "LOW" state and the level at which the output begins to go from HIGH to LOW.
12. See Hysteresis test circuit.
13. Refer to AC test circuits.
14. V_{CC} = 5.25V.

AC TEST CIRCUIT AND WAVEFORMS



3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.



Input Pulse:
Amplitude = 2.6V
Pulse width = 200ns
(50% Duty Cycle)
$t_r = t_f$ = 5ns (10% to 90%)

TABLE 1		
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

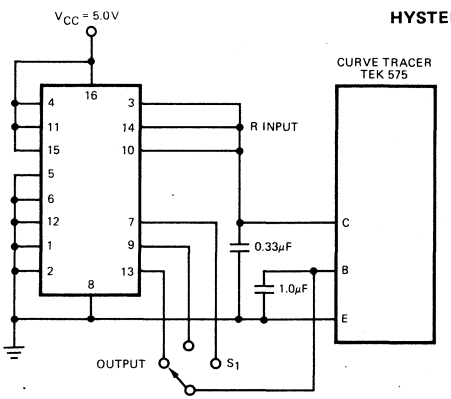
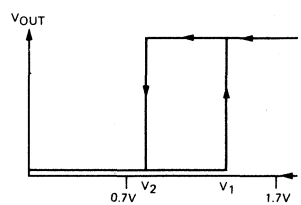


Fig. 1

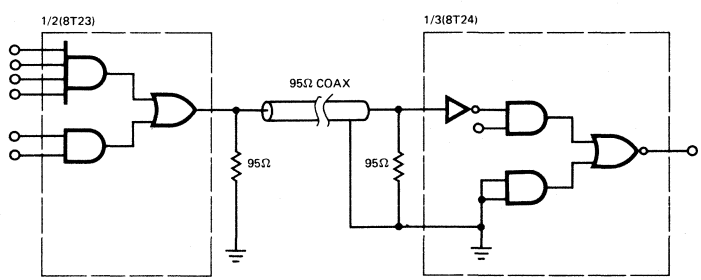


Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

1. V_1x and V_2 must be between 0.7V minimum and 1.7V maximum.
2. Hysteresis = $V_1 - V_2$

Fig. 2

TYPICAL APPLICATION



TTL/MSI 9307
7-SEGMENT DECODER

FOR ADDITIONAL INFORMATION SEE THE FAIRCHILD TTL DATA BOOK

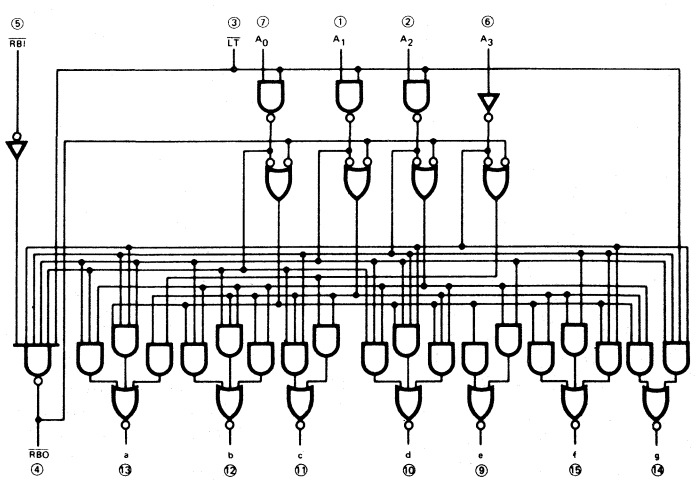
DESCRIPTION — The 9307 is a Seven Segment Decoder designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used with seven segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays. The 9307 is compatible with all other Fairchild TTL devices.

- **TTL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**
- **ALL CERAMIC, HERMETIC 16-LEAD DUAL IN-LINE PACKAGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

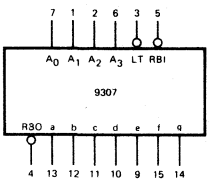
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} value
Input Voltage (dc)	−0.5 V to +5.5 V

LOGIC DIAGRAM



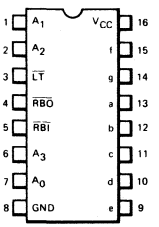
○ = Pin Numbers

LOGIC SYMBOL



V_{CC}=PIN 16
GND=PIN 8

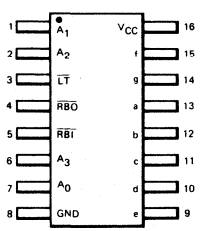
CONNECTION DIAGRAMS
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B



ORDER INFORMATION

TYPE	PART NO.
9307	9307DM
9307C	9307DC

16-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 4L



ORDER INFORMATION

TYPE	PART NO.
9307	9307FM
9307C	9307FC

TTL/MSI 9317B • 9317C

7-SEGMENT DECODER/DRIVERS

FOR ADDITIONAL INFORMATION SEE THE FAIRCHILD TTL DATA BOOK.

DESCRIPTION — The 9317 is a TTL/MSI Seven Segment Decoder/Driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used to directly drive seven segment incandescent lamp displays and light emitting diode indicators (or indirectly drive neon, electro-luminescent, numeric displays). The 9317 is compatible with all members of the Fairchild TTL family.

The 9317 is available in two output current and latch voltage versions, the 9317B and C.

- **TTL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE LOW OUTPUTS**
- **ALL CERAMIC, HERMETIC 16-LEAD DUAL IN-LINE PACKAGE**
- **DRIVE LAMPS DIRECTLY**
- **CODES IN EXCESS OF BINARY NINE DISABLE OUTPUTS**
- **ENHANCED RELIABILITY WITH UNIQUE NUMERIC ONE DISPLAY POSITION**

PIN NAMES

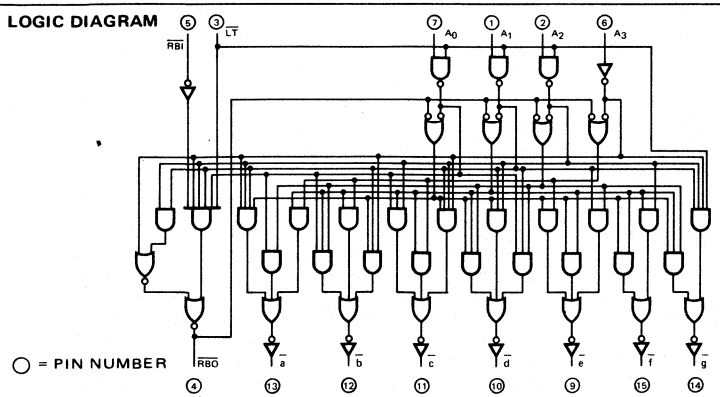
		LOADING	
		HIGH	LOW
A_0, A_1, A_2, A_3	Address Inputs	1.0 U.L.	1.0 U.L.
$\overline{LT}$	Lamp Test (Active LOW) Input	5.0 U.L.	4.0 U.L.
$\overline{RBI}$	Ripple Blanking (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{RBO}$	Ripple Blanking (Active LOW) Output	1.5 U.L.	1.5 U.L.
$\bar{a}$, $\bar{b}$, $\bar{c}$, $\bar{d}$, $\bar{e}$, $\bar{f}$, $\bar{g}$	(Active LOW) Outputs	See Options	

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

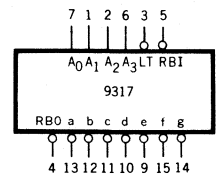
OPTIONS

PARAMETER	9317B	9317C
Latch Voltage	20 V	30 V
Output Current (Pins 9 through 15)	40 mA	20 mA

LOGIC DIAGRAM

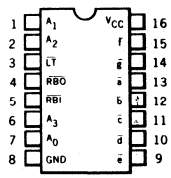


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

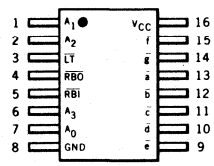
CONNECTION DIAGRAMS
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 7B



ORDER INFORMATION

TYPE	PART NO.
9317B	9317BDM
9317B	9317BDC
9317C	9317CDM
9317C	9317CDC

16-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 4L



ORDER INFORMATION

TYPE	PART NO.
9317B	9317BFM
9317B	9317BFC
9317C	9317CFM
9317C	9317CFC

TTL/MSI 9368

7-SEGMENT DECODER/DRIVER/LATCH

FOR ADDITIONAL INFORMATION SEE SEPARATE DATA SHEET

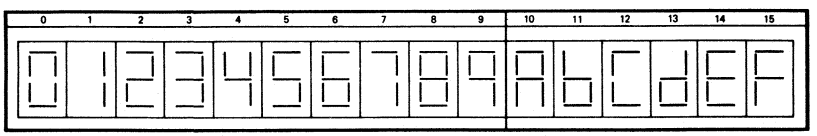
DESCRIPTION – The 9368 is a TTL/MSI Seven Segment Decoder/Driver incorporating input latches, and output circuits to drive common cathode type LED displays directly.

- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **DRIVES COMMON CATHODE LED DISPLAYS DIRECTLY**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **HEXADECIMAL DECODE FORMAT**
- **LATCH SPEED COMPARABLE TO STANDARD MSI LATCHES**
- **DATA INPUT FAN IN ZERO WHEN LATCH NOT ENABLED***
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZERO's**
- **PINOUT COMPARABLE WITH OTHER STANDARD MSI DECODERS SUCH AS 9307, 9317, 9357A (7446), 9357B (7447), 9358 (7448), 9359 (7449)**

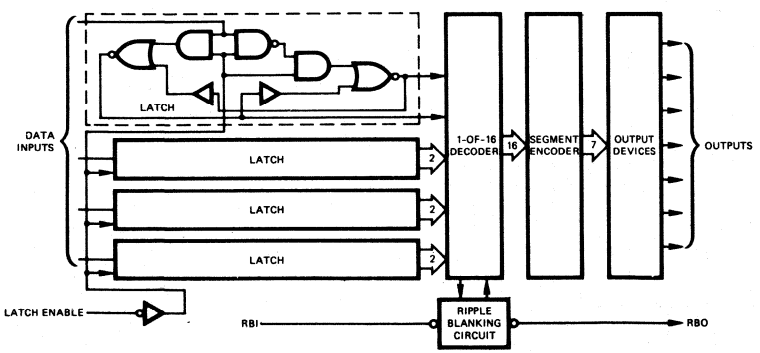
PIN NAMES		LOADING HIGH	LOADING LOW
A_0, A_1, A_2, A_3	Address Inputs	2.0 U.L.	1.0 U.L.*
$\overline{E_L}$	Latch Enable (data in)	1.0 U.L.	1.0 U.L.
$\overline{RBI}$	Ripple Blanking (Active LOW) Input	1.0 U.L.	1.0 U.L.
$\overline{RBO}$	Ripple Blanking (Active LOW) Output	2.0 U.L.	2.0 U.L.
a, b, c, d, e, f, g	(Active HIGH) Outputs	20 mA	"OFF"

*LOW level loading is 1 U.L. only when latch is enabled. When latch is disabled loading is 10 μA.

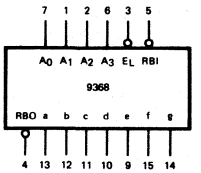
NUMERICAL DESIGNATIONS



BLOCK DIAGRAM

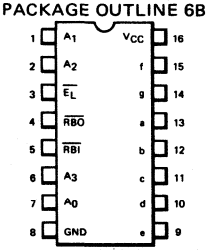


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

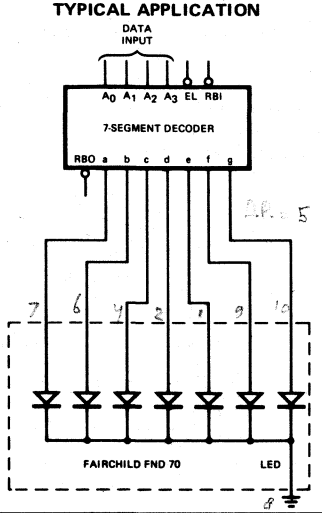
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B



ORDER INFORMATION

TYPE	PART NO.
9368	9368DC

TYPICAL APPLICATION



11

TTL/MSI 9370

7-SEGMENT DECODER/DRIVER/LATCH

FOR ADDITIONAL INFORMATION SEE SEPARATE DATA SHEET

DESCRIPTION — The 9370 is a TTL/MSI Seven Segment Decoder/Driver incorporating input latches and output circuits to drive incandescent displays directly. It can also be used to drive common anode LED displays in either a multiplexed mode or directly with the aid of external current limiting resistors.

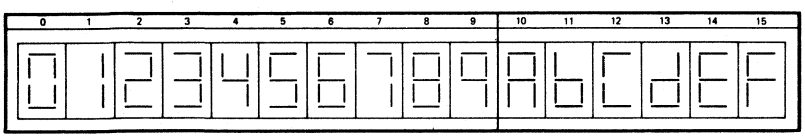
- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **25 mA SINK CAPABILITY TO DRIVE EITHER INCANDESCENT OR COMMON ANODE LED DISPLAYS**
- **HEXADECIMAL DECODE FORMAT**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH IS DISABLED***
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZERO'S AND/OR TRAILING EDGE ZERO's**
- **PINOUT COMPATIBLE WITH OTHER STANDARD MSI DECODERS SUCH AS 9307, 9317, 9357A (7446), 9357B (7447), 9358 (7448)**

PIN NAMES

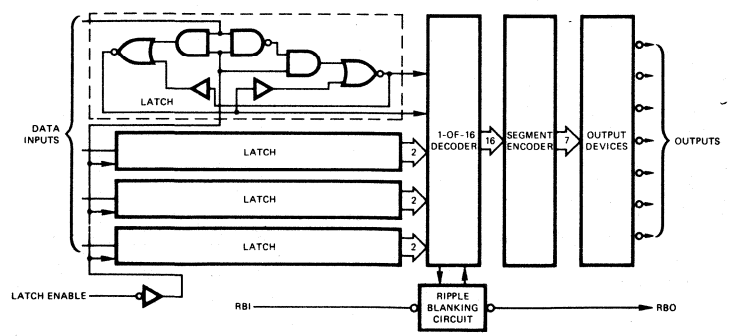
		LOADING HIGH	LOADING LOW
A_0, A_1, A_2, A_3	Address Inputs	2.0 U.L.	1.0 U.L.*
$\overline{E_L}$	Latch Enable	1.0 U.L.	1.0 U.L.
$\overline{RBI}$	Ripple Blanking (Active LOW) Input	1.0 U.L.	1.0 U.L.
$\overline{RBO}$	As an Output	2.0 U.L.	2.0 U.L.
$\overline{RBO}$	As an Input	1.0 U.L.	2.0 U.L.
$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$	(Active LOW) Open Collector Outputs	"OFF"	25 mA

* LOW level loading is 1 U.L. only when latch is enabled. When latch is disabled loading is 10 μA.

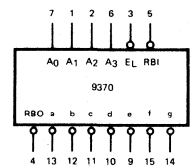
NUMERICAL DESIGNATIONS



BLOCK DIAGRAM

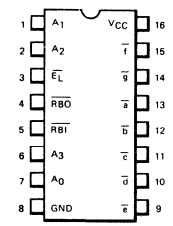


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

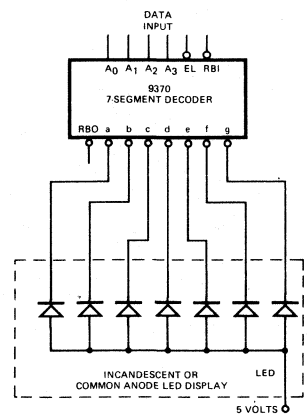
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B



ORDER INFORMATION

TYPE	PART NO.
9370	9370DC

TYPICAL APPLICATION



9612 • 9612E

DUAL DIFFERENTIAL LINE DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9612 Dual Differential Line Driver is designed specifically to drive single ended or differential, back matched or terminated transmission lines. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down, for use in simplex or simplex distribution bus systems. The devices feature a short circuit protected active pull-up. The inputs and outputs have clamp diodes to minimize the effect of line transients. The active pull-up output offers low output impedance allowing back matching or parallel termination of the line. The 9612E and 9612A are specified to drive 50 Ω transmission line at high speed while guaranteeing a maximum skew between outputs of less than 3.5 ns for application requiring high performance line drivers. (9613 is the functional complement).

9612A/9612/9612E

- **SINGLE 5 V SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLEMENTARY OUTPUTS**

9612A/9612E

- **GUARANTEED MAXIMUM OUTPUT SKEW**
- **HIGH OUTPUT DRIVE CAPABILITY FOR 50 Ω TRANSMISSION LINES**

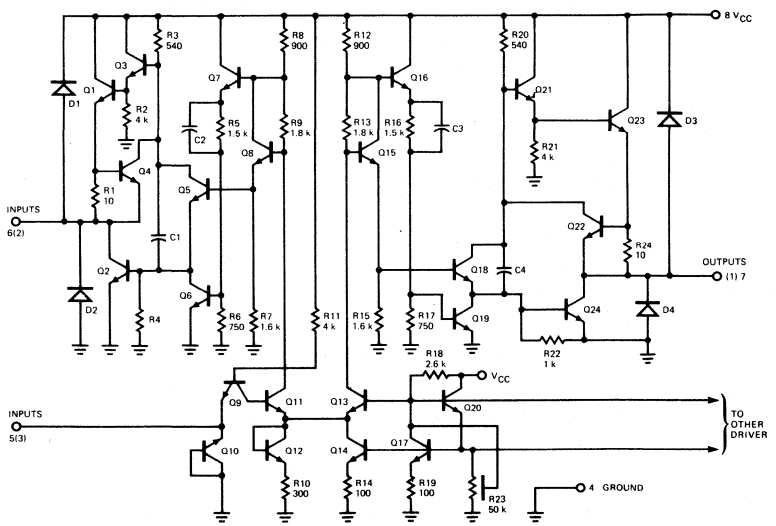
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	
9612A	−55°C to +125°C
9612, 9612E	0°C to +70°C
V_{CC}	+7.0 V
V_{IN}	−0.5 V to +5.5 V
Internal Power Dissipation (Note 1)	800 mW
Lead Temperature (Soldering, 10 s)	
Metal Can, Hermetic Mini DIP (Soldering, 60 s)	300°C
Molded Mini DIP (Soldering, 10 s)	260°C

NOTE:

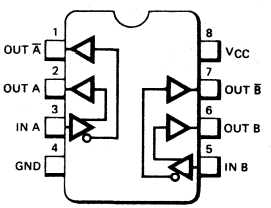
1. For the Hermetic Mini DIP and Molded Mini DIP derate above 30°C at 6.7 mW/°C. For the Metal Can derate above 70°C at 6.3 mW/°C; the rating for Metal Can requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 95°C/W.

EQUIVALENT CIRCUIT (1/2 of 9612)



CONNECTION DIAGRAM
8-LEAD MINIDIP
(TOP VIEW)

PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R

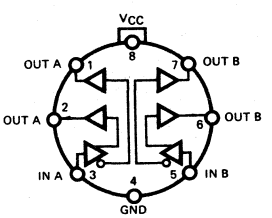


ORDER INFORMATION

TYPE	PART NO.
9612	9612TC
9612E	9612ETC
9612A	9612ARM
9612	9612RC
9612E	9612ERC

8-LEAD METAL CAN
(TOP VIEW)

PACKAGE OUTLINE 5B
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
9612A	9612AHM
9612	9612HC
9612E	9612EHC

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, T_A = −55°C to +125°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{OL}	Output LOW Voltage	I_{OL} = 40 mA		200	400	mV
V_{OLC}	Clamped Output LOW Voltage	I_{OLC} = −40 mA	−1.5	−0.8		V
V_{OH}	Output HIGH Voltage	I_{OH} = −40 mA	2.0	2.75		V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	−140	−77	−42	mA
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.0			V
I_{IL}	Input LOW Current	V_{IL} = 0.4 V	−1.6			mA
I_{IH}	Input HIGH Current	V_{IH} = 2.4 V			40	μA
I_R	Input Reverse Current	V_R = 4.5 V			1.0	mA
V_{CD}	Input Clamp Diode Voltage	V_{CC} = 4.75 V, I_{IC} = −12 mA, T = 25°C	−1.5	−0.8		V
I_{CC}	Supply Current	Inputs = 0 V, T = 25°C		42	50	mA
I_{max}	Max. Supply Current	Inputs = 0 V, V_{max} = 7.0 V, T = 25°C		59	70	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C, unless otherwise specified)

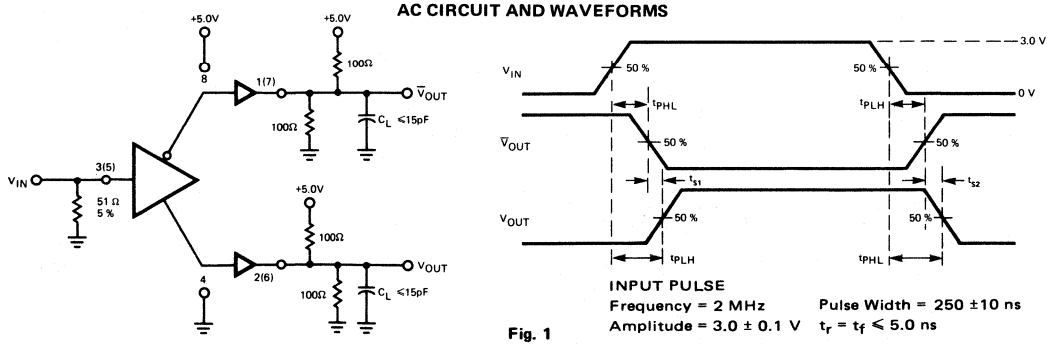
SYMBOL	PARAMETER	CONDITIONS	LIMITS						UNITS
			9612			9612E			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	Output LOW Voltage	I_{OL} = 40 mA		200	400		200	400	mV
		I_{OL} = 50 mA (9612E only)					250	400	mV
V_{OLC}	Clamped Output LOW Voltage	I_{OLC} = −40 mA	−1.5	−0.8		−1.5	−0.8		V
		I_{OLC} = −50 mA (9612E only)				−1.5	−0.9		V
V_{OH}	Output HIGH Voltage	I_{OH} = −40 mA	2.4	2.75		2.4	2.75		V
		I_{OH} = −50 mA (9612E only)				2.4	2.60		V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	−140	−77	−42	−140	−77	−55	mA
V_{IL}	Input LOW Voltage				0.8			0.8	V
V_{IH}	Input HIGH Voltage		2.0			2.0			V
I_{IL}	Input LOW Current	V_{IL} = 0.4 V	−1.6			−1.6			mA
I_{IH}	Input HIGH Current	V_{IH} = 2.4 V			40			40	μA
I_R	Input Reverse Current	V_R = 4.5 V			1.0			1.0	mA
V_{CD}	Input Clamp Diode Voltage	V_{CC} = 4.75 V, I_{IC} = −12 mA	−1.5	−0.8		−1.5	−0.8		V
I_{CC}	Supply Current	Inputs = 0 V		42	50		42	50	mA
I_{max}	Max. Supply Current	Inputs = 0 V, V_{max} = 7.0 V		59	70		59	70	mA

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, R_L = 100 Ω (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LIMITS						UNITS
			9612			9612A/9612E			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Turn Off Time	R_L = 100 Ω (Note 1)			30			20	ns
t_{PHL}	Turn On Time	$C_L \leq$ 15 pF			30			20	ns
t_s	Output Skew	See Fig. 1				−3.5		+3.5	ns

NOTE: 1. R_L must be noninductive.

AC CIRCUIT AND WAVEFORMS

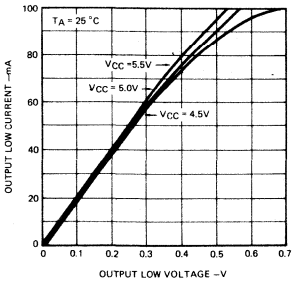


INPUT PULSE
Frequency = 2 MHz Pulse Width = 250 ±10 ns
Amplitude = 3.0 ± 0.1 V $t_r = t_f \leq$ 5.0 ns

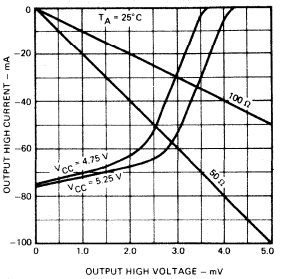
Fig. 1

TYPICAL PERFORMANCE CURVES

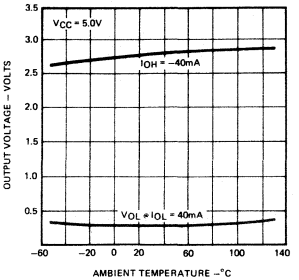
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



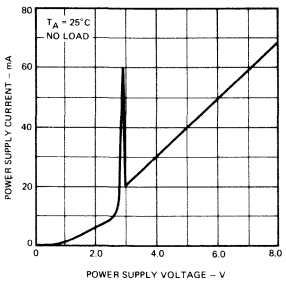
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



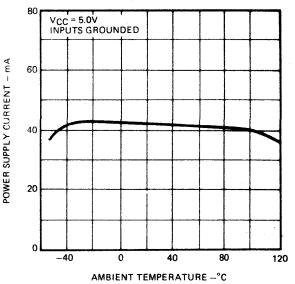
OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



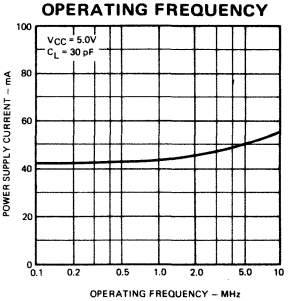
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



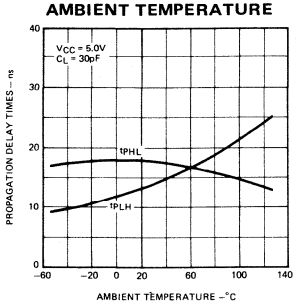
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



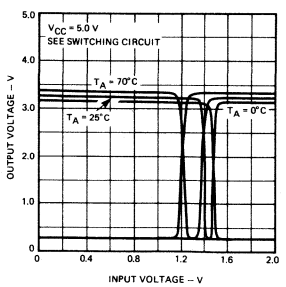
SUPPLY CURRENT AS A FUNCTION OF OPERATING FREQUENCY



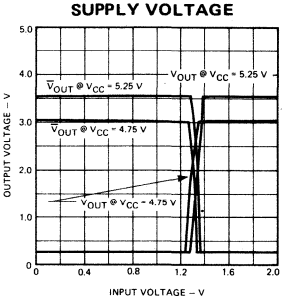
PROPAGATION DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSFER CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



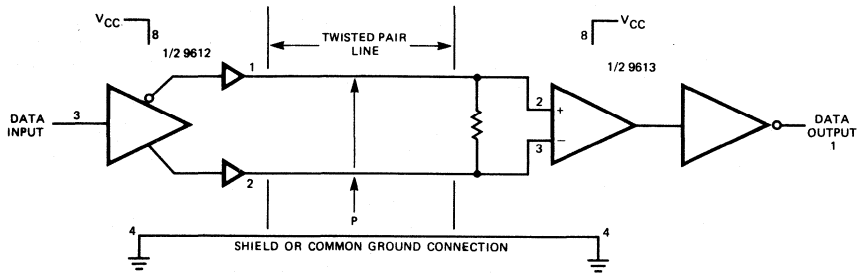
TRANSFER CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



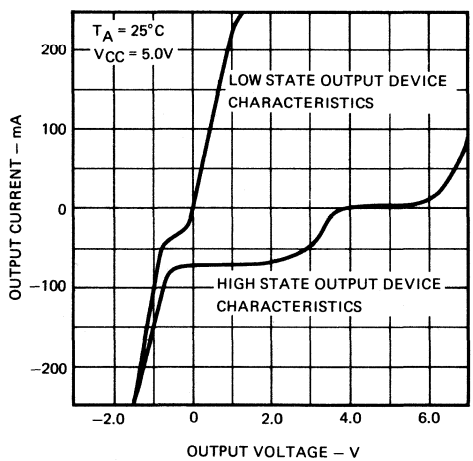
11

TYPICAL APPLICATIONS

SIMPLEX BALANCED DIFFERENTIAL OPERATION



TYPICAL REFLECTION DIAGRAM



9613

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9613 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature range using a single 5.0 V supply. It can receive ± 500 mV of differential data in the presence of high level (± 15 V) common mode voltag es and deliver undistrubed TTL logic to the output.

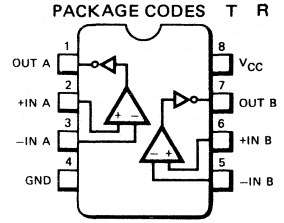
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **SINGLE 5.0 V SUPPLY VOLTAGES**
- **MILITARY TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Supply Voltage (V_{CC} Potential to Ground)	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 2, 3, 5, 6)	±20 V
Differential Input Voltage (+ Input Referred to − Input)	±20 V
Internal Power Dissipation	
Metal Can (Note 1)	500 mW
Molded DIP, Hermetic DIP (Note 2)	800 mW
Operating Temperature	
9613	−55°C to +125°C
9613C	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
9613 Metal Can, Hermetic DIP (Soldering, 60 s)	300°C
9613C Molded DIP (Soldering, 10 s)	260°C

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can.
2. Rating applies to ambient temperatures up to 30°C. Above 30°C ambient derate linearly at 5.4 mW/°C for Molded DIP and 6.7 mW/°C for Hermetic DIP.

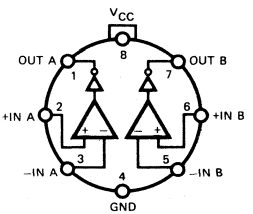
CONNECTION DIAGRAMS
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
9613	9613RM
9613C	9613RC
9613C	9613TC

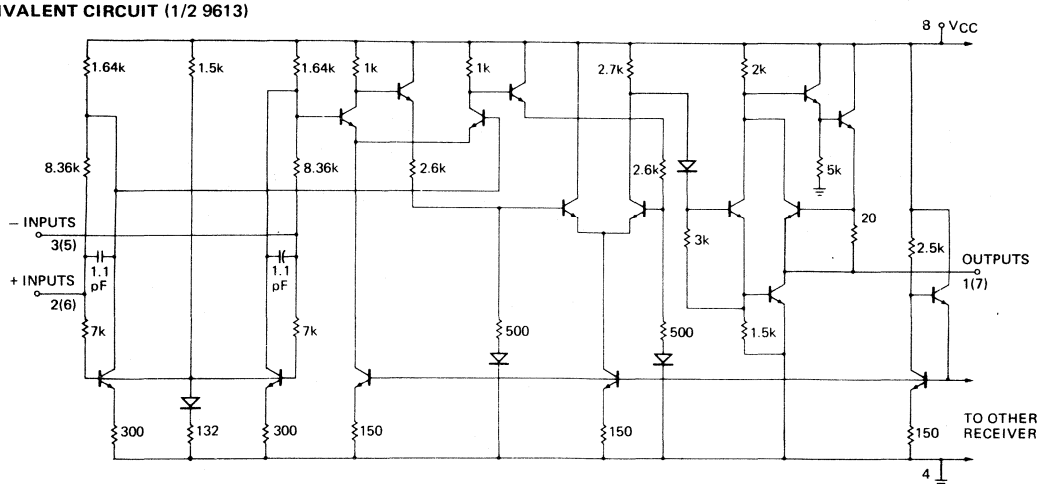
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
9613	9613HM
9613C	9613HC

EQUIVALENT CIRCUIT (1/2 9613)



9613

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, −55°C ≤ T_A ≤ 125°C unless otherwise specified)

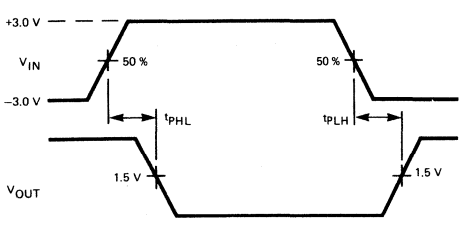
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.28	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4	3.0		V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0 V	−60	−28	−12	mA
R_{IN}	Input Resistance		3.0	4.2		kΩ
V_{CM}	Operating Common Mode Voltage Range	−1.0 V ≤ V_{DIFF} ≤ +1.0 V	−15		+15	V
V_{TH}	Differential Input Threshold Voltage	−5.0 V ≤ V_{CM} ≤ +5.0 V	−0.5		+0.5	V
		−15 V ≤ V_{CM} ≤ +15 V	−1.0		+1.0	V
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		29	50	mA
I_{MAX}	Maximum Supply Current	V_{CC} = 7.0 V		42	70	mA
t_{PLH}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		25	40	ns
t_{PHL}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		23	40	ns

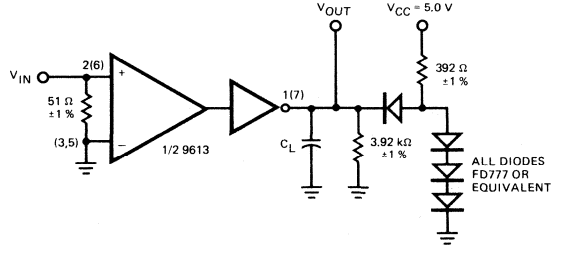
9613C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5 %, 0°C ≤ T_A ≤ 70°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.28	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4	3.0		V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0 V	−60	−28	−12	mA
R_{IN}	Input Resistance		3.0	4.2		kΩ
V_{CM}	Operating Common Mode Voltage Range	−1.0 V ≤ V_{DIFF} ≤ +1.0 V	−15		+15	V
V_{TH}	Differential Input Threshold Voltage	−5.0 V ≤ V_{CM} ≤ +5.0 V	−0.5		+0.5	V
		−15 V ≤ V_{CM} ≤ +15 V	−1.0		+1.0	V
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		29	50	mA
I_{MAX}	Maximum Supply Current	V_{CC} = 7.0 V		42	70	mA
t_{PLH}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		25	40	ns
t_{PHL}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		23	40	ns

AC TEST CIRCUIT AND WAVEFORMS





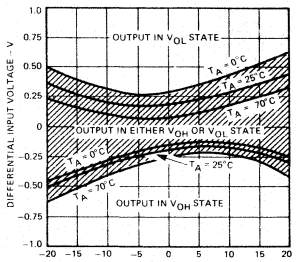
V_{IN}: (PULSE)
Amplitude: 6.0 V
Pulse Width: 100 ns
Duty Cycle: 50 %
t_r = t_f ≤ 5 ns

C_L = 30 pF ±5 % Including jig capacitance.

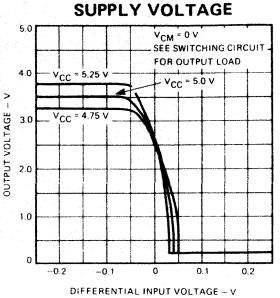
TYPICAL ELECTRICAL CHARACTERISTICS CURVES

9613

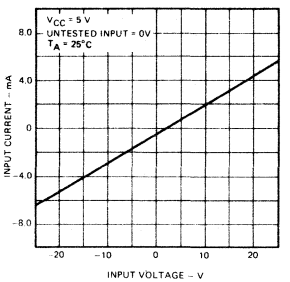
INPUT DIFFERENTIAL THRESHOLD AMBIGUITY AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



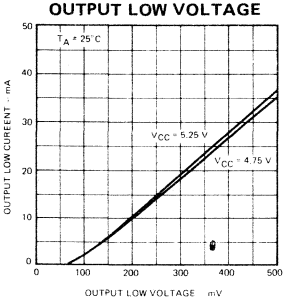
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF POWER SUPPLY VOLTAGE



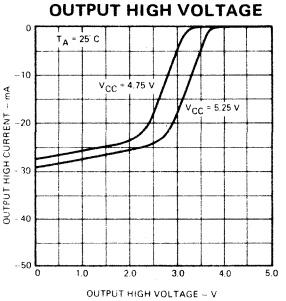
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



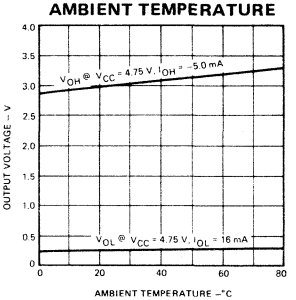
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



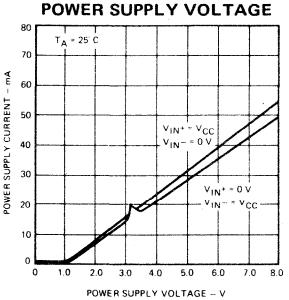
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



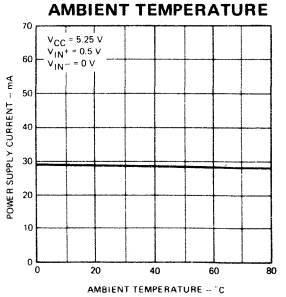
OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



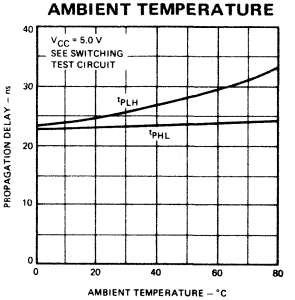
POWER SUPPLY CURRENT AS A FUNCTION OF POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

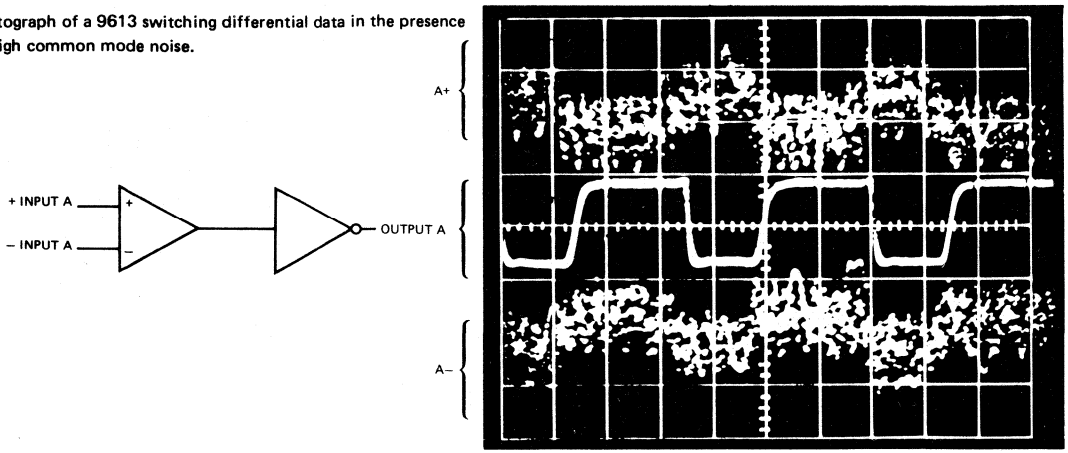


PROPAGATION DELAY AS A FUNCTION OF AMBIENT TEMPERATURE



11

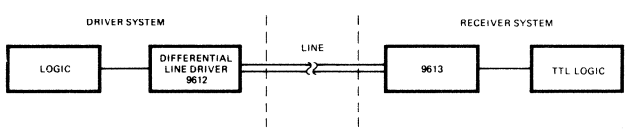
Photograph of a 9613 switching differential data in the presence of high common mode noise.



VERTICAL = 2.0 V DIV. HORIZONTAL = 50 ns/DIV.

Fig. 1

STANDARD USAGE



For example of operation see 9612 data sheet application section.

Fig. 2

9614

DUAL DIFFERENTIAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull up and the pull down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull ups on one side and the uncommitted collectors on the other (See Fig. 5). The active pull up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing NAND and AND functions of the inputs, adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.

- **SINGLE 5 VOLT SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLEMENTARY OUTPUTS FOR NAND, AND OPERATION**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION**
- **MILITARY TEMPERATURE RANGE**

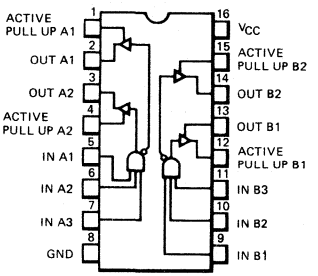
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be imparied)

Storage Temperature Range	−65°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 1)	670 mW
Operating Temperature Range	
Military (9614)	−55°C to +125°C
Commercial (9614C)	0°C to +70°C

NOTE:

1. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

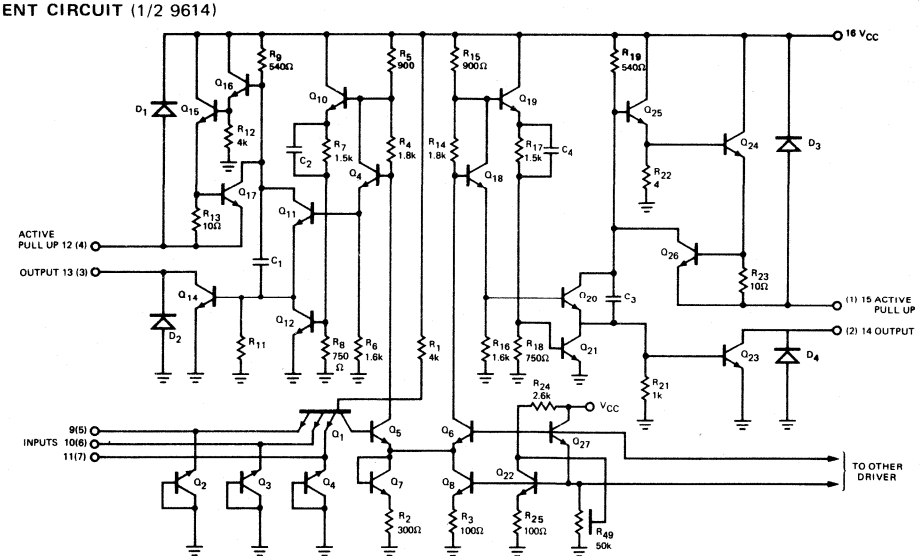
CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
9614	9614DM
9614	9614FM
9614C	9614DC
9614C	9614PC

EQUIVALENT CIRCUIT (1/2 9614)



9614

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%)

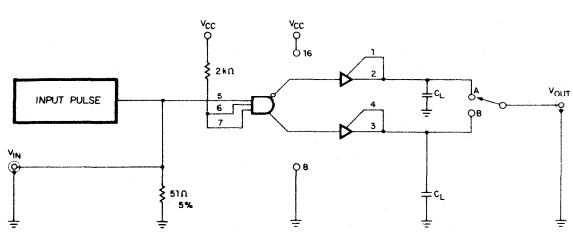
SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS	
		−55°C		+25°C			+125°C				
		MIN	MAX	MIN	TYP	MAX	MIN	MAX			
V_{OL}	Output LOW Voltage		400		200	400		400	mV	I_{OL} = 40 mA	V_{CC} = 4.5 V
V_{OH1}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.5 V
V_{OH2}		2.0		2.0	2.6		2.0		V	I_{OH} = −40 mA	
I_{SC}	Output Short-Circuit Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.5 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 12.0 V	V_{CC} = 5.5 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.4 V	V_{CC} = 5.5 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.5 V
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	V_{CC} = 5.5 V	
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	V_{CC} = 4.5 V	
V_{OLC}	Clamped Output LOW Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.5 V
I_{CC}	Supply Current				34	50			mA	Inputs = 0 V	V_{CC} = 5.5 V
I_{max}	Supply Current				46	65			mA	Inputs = 0 V	V_{max} = 7.0 V
t_{PLH}	Turn-Off Time				14	20			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	20			ns	See Fig. 1	V_M = 1.5 V
V_{CD}	Input Clamp Diode Voltage				−1.0	−1.5			V	V_{CC} = 4.5 V	I_{IC} = −12 mA

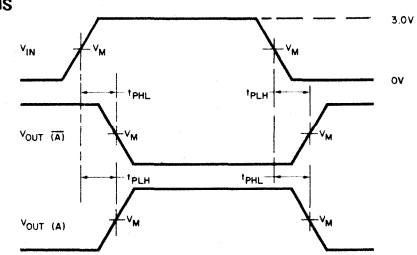
9614C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS	
		0°C		+25°C			+70°C				
		MIN	MAX	MIN	TYP	MAX	MIN	MAX			
V_{OL}	Output LOW Voltage		450		200	450		450	mV	I_{OL} = 40 mA	V_{CC} = 4.75 V
V_{OH1}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.75 V
V_{OH2}		2.4		2.4	2.6		2.4		V	I_{OH} = −40 mA	
I_{SC}	Output Short-Circuit Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.25 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 5.25 V	V_{CC} = 5.25 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.45 V	V_{CC} = 5.25 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.25 V
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	V_{CC} = 5.25 V	
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	V_{CC} = 4.75 V	
V_{OLC}	Clamped Output LOW Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.25 V
I_{CC}	Supply Current				33	50			mA	Inputs = 0 V	V_{CC} = 5.25
I_{max}	Supply Current				46	70			mA	Inputs = 0 V	V_{max} = 7.0 V
t_{PLH}	Turn-Off Time				14	30			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	30			ns	See Fig. 1	V_M = 1.5 V
V_{CD}	Input Clamp Diode Voltage				−1.0	−1.5			V	V_{CC} = 4.75 V	I_{IC} = −12 mA

AC TEST CIRCUIT AND WAVEFORMS



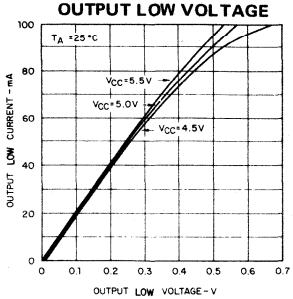


INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

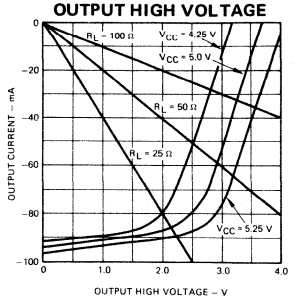
Fig. 1

TYPICAL ELECTRICAL CHARACTERISTICS

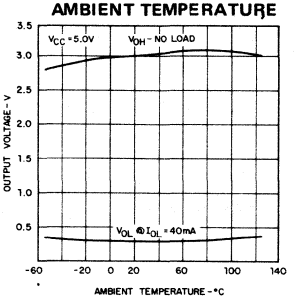
ACTIVE PULL DOWN OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



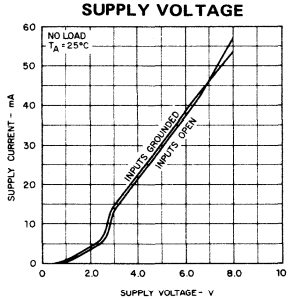
ACTIVE PULL UP OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



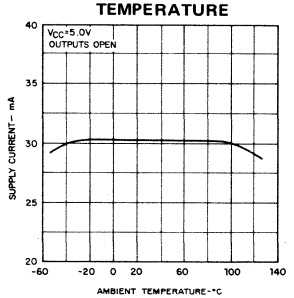
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



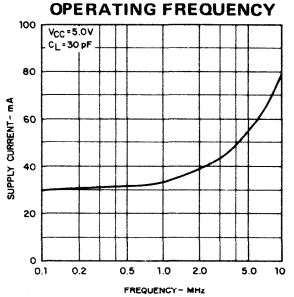
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



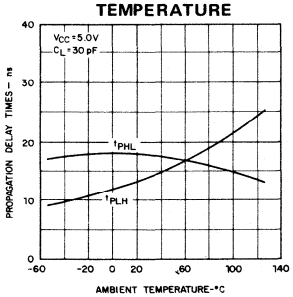
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



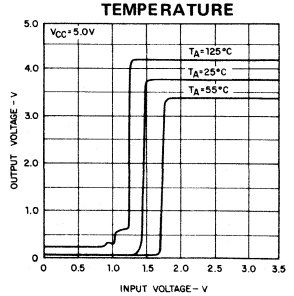
SUPPLY CURRENT AS A FUNCTION OF OPERATING FREQUENCY



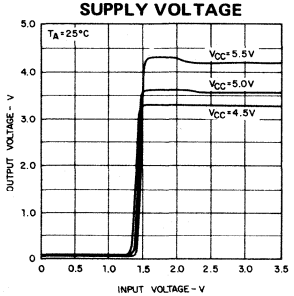
PROPAGATION DELAY TIME AS A FUNCTION OF TEMPERATURE



TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE



TRANSFER CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



11

APPLICATIONS

DIFFERENTIAL MODE EXPANSION
MULTIPLEX OPERATION

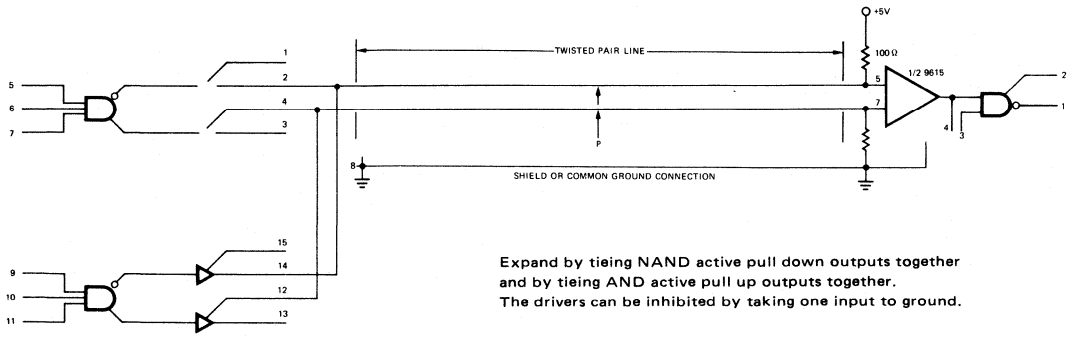
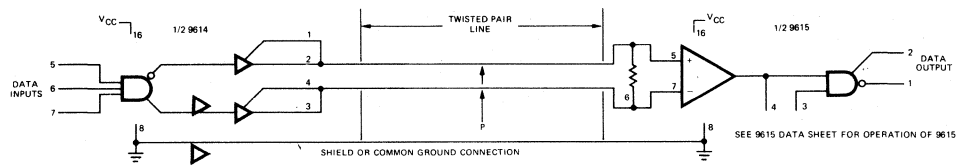


Fig. 2

Note: Only 1 Driver is Enabled At One Time

SIMPLEX – DIFFERENTIAL OPERATION



See 9615 Data Sheet for operation of 9615.

Fig. 3

TYPICAL REFLECTION DIAGRAM

NOTE–SEE 9621 DATA SHEET FOR USAGE OF REFLECTION DIAGRAM

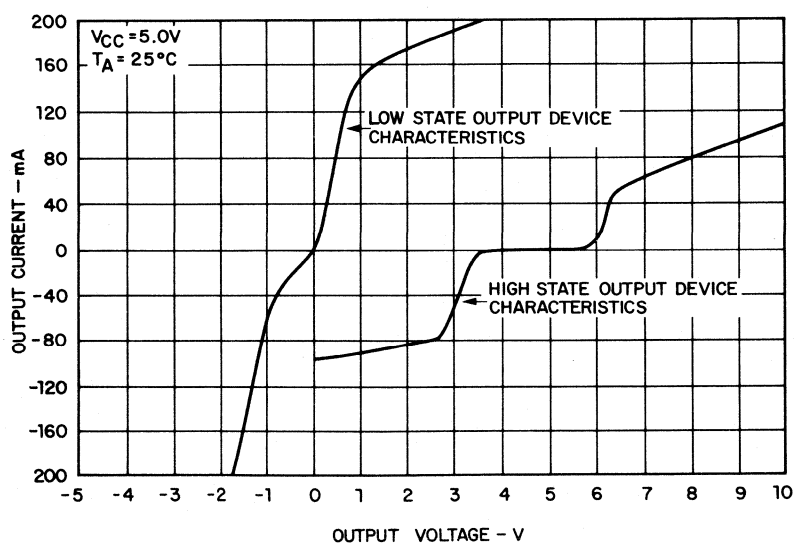


Fig. 4

9615

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9615 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 V supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe and a 130 Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull up available on an adjacent pin to allow either wire-OR or active pull up TTL output configuration.

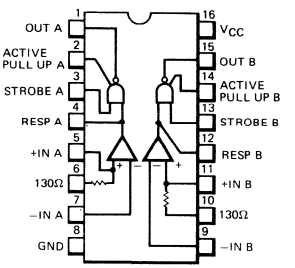
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 V SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130 Ω TERMINATING RESISTOR**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 5, 6, 7, 9, 10, 11)	±20 V
Voltage Applied to Outputs for HIGH output State without Active Pull Up	−0.5 V to +13.2 V
Voltage Applied to Strobe	−0.5 V to +5.5 V
Lead Temperature Range	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 1)	
Operating Temperature Range	670 mW
Military (9615)	−55°C to +125°C
Commercial (9615C)	0°C to +70°C

NOTE:
1. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F

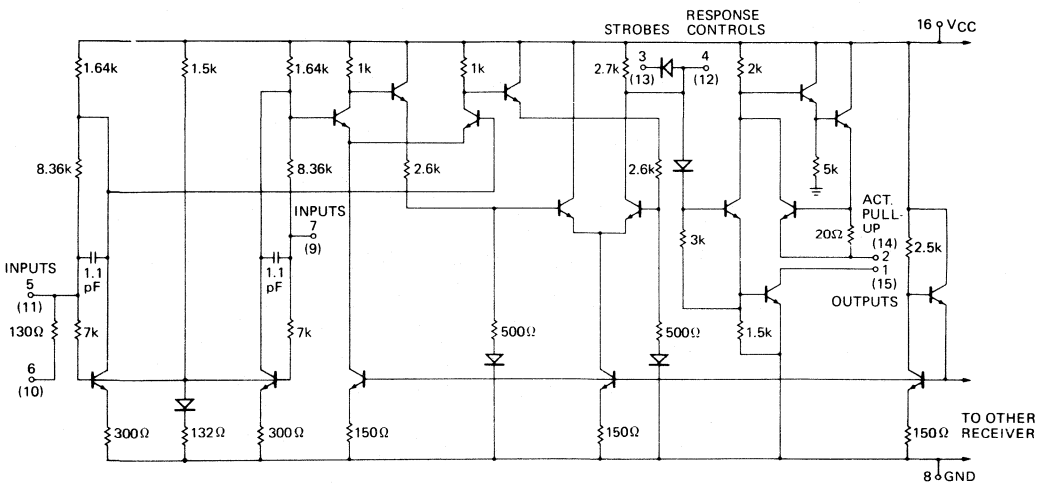


ORDER INFORMATION

TYPE	PART NO.
9615	9615DM
9615	9615FM
9615C	9615DC
9615C	9615PC

11

EQUIVALENT CIRCUIT (1/2 9615)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		0°C		+25°C			+70°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		V	V_{CC} = 4.75 V, V_{OUT} = ** I_{OH} = –5.0 mA, *V_{DIFF} = –0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 5.25 V, *V_{DIFF} = V_{CC} = 4.75 V
I_{SC}	Output Shorted Current			–14		–100			mA	V_{CC} = 5.25 V, **V_{SC} = 0 V, *V_{DIFF} = –0.5 V
I_{IN}	Input Current		–0.9		–0.49	–0.7		–0.7	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V Other Input = 5.25 V
$I_{IN(ST)}$	Strobe Input Current				–1.15	–2.4			mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			–1.2	–3.4				mA	V_{CC} = 5.25 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	–15	+15	–15	±17.5	+15	–15	+15	V	V_{CC} = 5.0 V, *V_{DIFF} = 1.0V
$I_{R(ST)}$	Strobe Input Leakage Current					5.0		10	μA	V_{CC} = 4.75 V, *V_{DIFF} = –0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			74	130	179			Ω	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = GND
V_{TH} ***	Differential Input	–500	500	–500	–80	500	–500	500	mV	V_{CM} = 0V; V_{CC} = 5.0V ± 5%
	Threshold Voltage	–1.0	1.0	–1.0		1.0	–1.0	1.0	V	-15 ≤ V_{CM} ≤ +15V; V_{CC} = 5.0V ± 5%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.25 V, +Inputs = 0.5 V, –Inputs = 0 V
t_{PLH}	Turn-Off Time				30	75			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1
t_{PHL}	Turn-On Time				30	75			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1

*V_{DIFF} is a differential input voltage referred from "+IN A" to "–IN A" and from "+IN B" to "–IN B".
**Connect Output "A" to Active Pull up "A" and Output "B" to Active Pull up "B".
*** See input-output transfer characteristic graphs on following pages.

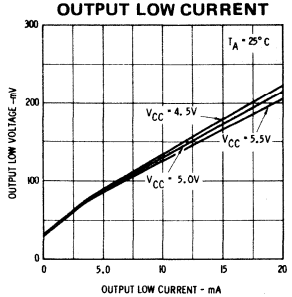
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		-55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		0.40		0.18	0.40		0.40	V	V_{CC} = 4.5 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.2		2.4	3.2		2.4		V	V_{CC} = 4.5 V, V_{OUT} = ** I_{OH} = -5.0 mA, *V_{DIFF} = -0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 12 V, *V_{DIFF} = V_{CC} = 4.5 V
I_{SC}	Output Shorted Current			-15	-39	-80			mA	V_{CC} = 5.5 V, **V_{SC} = 0 V, *V_{DIFF} = -0.5 V
I_{IN}	Input Current		-0.9		-0.49	-0.7		-0.7	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Input = 5.5 V
$I_{IN(ST)}$	Strobe Input Current				-1.15	-2.4			mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			-1.2	-3.4				mA	V_{CC} = 5.5 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	-15	+15	-15	±17.5	+15	-15	+15	V	V_{CC} = 5.0 V, *V_{DIFF} = +1.0V
$I_{R(ST)}$	Strobe Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V, *V_{DIFF} = -0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			77	130	167			Ω	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = GND
V_{TH}***	Differential Input	-500	500	-500	80	500	-500	500	mV	V_{CM} = 0 ; V_{CC} = 5.0V ±10%
	Threshold Voltage	-1.0	1.0	-1.0			-1.0	1.0	V	-15 ≤ V_{CM} ≤ +15V ; V_{CC} = 5.0V ±10%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.5 V, -Inputs = 0 V, +Inputs = 0.5 V
t_{PLH}	Turn-Off Time				30	50			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1
t_{PHL}	Turn-On Time				30	50			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1

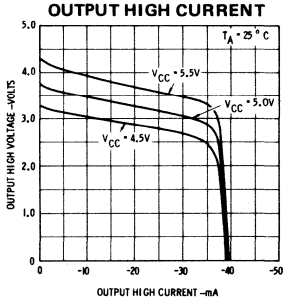
*V_{DIFF} is a differential input voltage referred from "+IN A" to "-IN A" and from "+IN B" to "-IN B".
**Connect Output "A" to Active Pull up "A" and Output "B" to Active Pull up "B".
***See input-output transfer characteristic graphs on following pages.

TYPICAL ELECTRICAL CHARACTERISTICS FOR 9615 AND 9615C

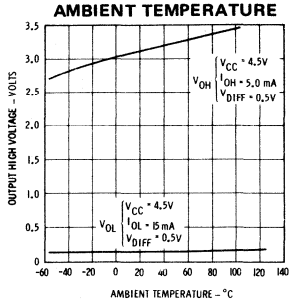
OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT LOW CURRENT



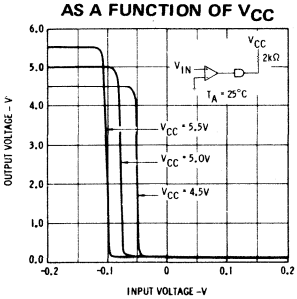
OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



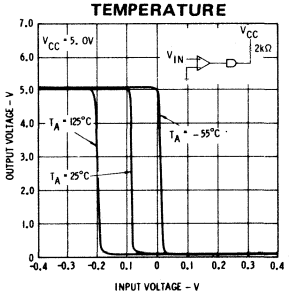
OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



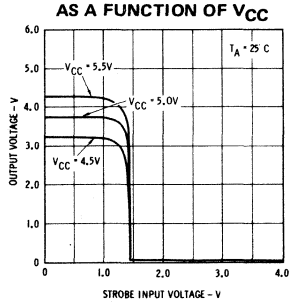
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF V_{CC}



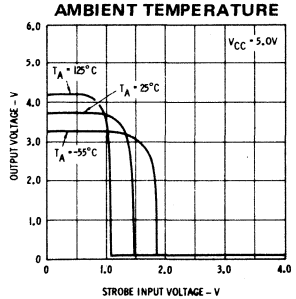
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF TEMPERATURE



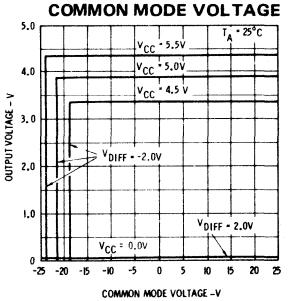
STROBE INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF V_{CC}



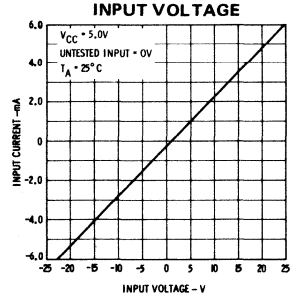
STROBE INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE



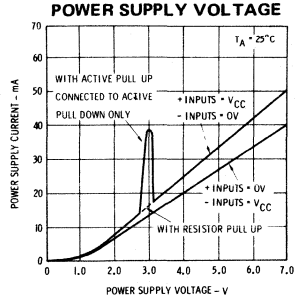
OUTPUT VOLTAGE AS A FUNCTION OF COMMON MODE VOLTAGE



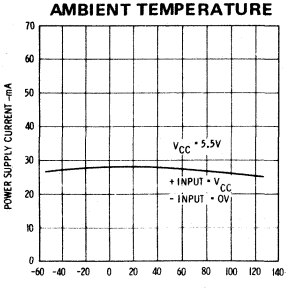
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



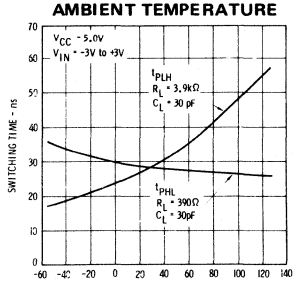
POWER SUPPLY CURRENT AS A FUNCTION OF POWER SUPPLY VOLTAGE



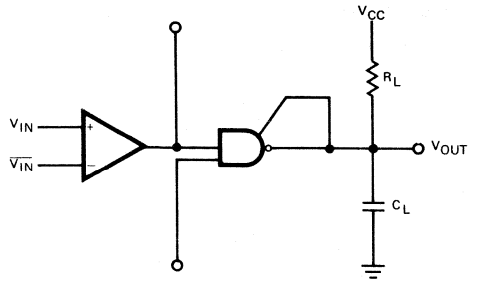
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

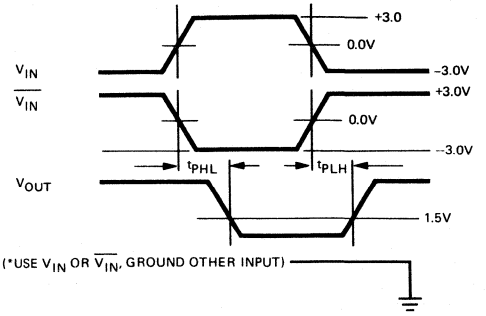
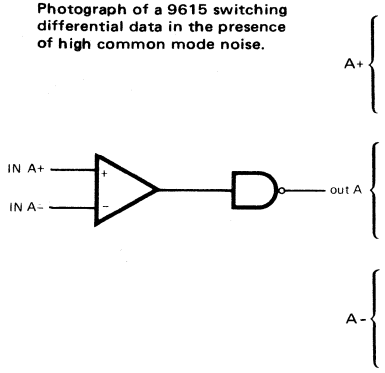
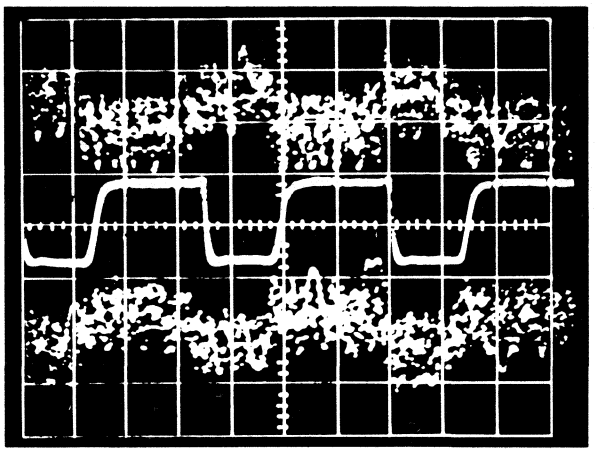


Fig. 1

Photograph of a 9615 switching differential data in the presence of high common mode noise.

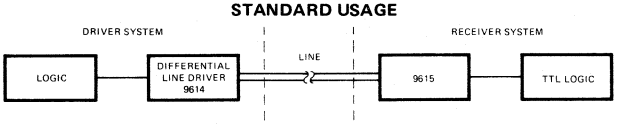




VERTICAL = 2.0 V DIV. HORIZONTAL = 50 ns/DIV.

Fig. 2

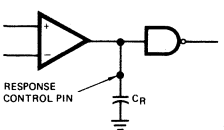
STANDARD USAGE



For example of operation see 9614 data sheet application section.

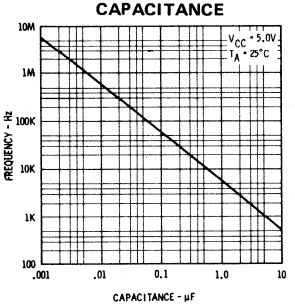
Fig. 3

FREQUENCY RESPONSE CONTROL



Note: 1. C_R>.01 μF may cause slowing of rise and fall times of the output.
2. Due to the mechanism of induction of differential noise, the use of the responce control is not normaly needed.

FREQUENCY RESPONSE AS A FUNCTION OF CAPACITANCE



11

9616
TRIPLE EIA RS-232-C/MIL-STD-188C LINE DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C (by the appropriate device selection). Each driver converts TTL/DTL logic levels to EIA/CCITT and/or MIL-STD-188C logic levels for transmission between data terminal equipment and data communications equipment. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH on the inhibit terminal interrupts signal transfer and forces the output to a V_{OL} (EIA/CCITT MARK) state.

For the complementary function, see the 9617 Triple EIA RS-232-C Line Receiver and the 9627 Dual EIA RS-232-C and MIL-STD-188C Line Receiver.

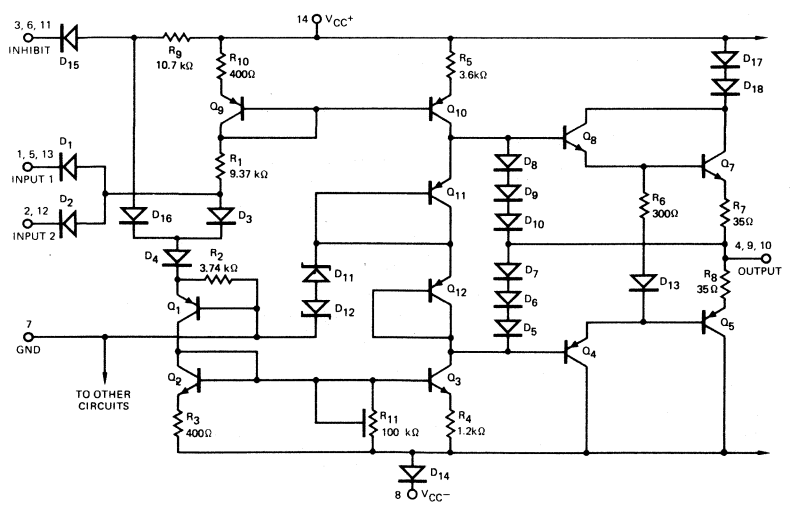
- **INTERNAL SLEW RATE LIMITING**
- **MEETS EIA RS-232-C AND CCITT V.24 AND/OR MIL-STD-188C**
- **LOGIC TRUE INHIBIT FUNCTION**
- **OUTPUT SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT VOLTAGE LEVELS INDEPENDENT OF SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

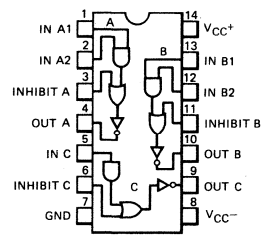
Supply Voltage	±15 V
Input or Inhibit Voltage	−1.5 V to +6.0 V
Output Signal Voltage	±15 V
Internal Power Dissipation (Note 1)	670 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
RS-232 Mil-Std-188 (9616)	−55°C to +125°C
RS-232 (9616C)	0°C to 70°C
RS-232 Mil-Std-188 (9616E)	0°C to 70°C
Lead Temperatures	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

NOTE:
1. For Hermetic DIP rating applies to ambient temperature up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

EQUIVALENT CIRCUIT (One of three channels)



CONNECTION DIAGRAM
14-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
9616	**9616DM**
9616	**9616FM**
9616C	**9616DC**
9616E	**9616EDC**
9616C	**9616PC**
9616E	**9616EPC**

TRUTH TABLE

INPUT 1	INPUT 2	INHIBIT	OUTPUT
All Sections:			
L	L	L	H
H	H	L	L
L	L	H	L
H	H	H	L
For Channels A & B add:			
L	H	L	H
H	L	L	H
L	H	H	L
H	L	H	L

(For Channel C, omit INPUT 2 Column)

*Planar is a patented Fairchild process.

9616 AND 9616E

RS232-C and MIL-STD-188C

ELECTRICAL CHARACTERISTICS (V_{CC} = ±12 V ±10%; $R_L \geq 3$ kΩ, See Test Circuit, unless otherwise specified, Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	Output HIGH Voltage		5.0	6.0	7.0	V
V_{OL}	Output LOW Voltage		−7.0	−6.0	−5.0	V
	Ripple Rejection	Power Supply Ripple = 2.4 Vp-p, f = 400 Hz		0.25		% of V_{OUT}
V_{OH} to V_{OL}	Output HIGH Voltage to Output LOW Voltage Magnitude Matching Error				±10	%
R_{OUT}	Output Resistance, Power On	R_L = 6 kΩ, ΔI_L = 10 mA		75		Ω
I_{SC+}	Positive Output Short Circuit Current			30	100	mA
I_{SC-}	Negative Output Short Circuit Current		−100	−30		mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V			40	μA
		V_{IN} = 5.5 V			1.0	mA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	−1.6			mA
R_{OUT}	Output Resistance, Power Off	−2.0 V ≤ V_{OUT} ≤ +2.0V All Inputs and Supply Pins Grounded	300			Ω
I_+	Positive Supply Current	T_A = +25°C, $V_{IN1} = V_{IN2} = V_{INHIBIT}$ = 0.8 V		15		mA
		T_A = +25°C, $V_{IN1} = V_{IN2} = V_{INHIBIT}$ = 2.0 V		7.5		
I_-	Negative Supply Current	T_A = +25°C, $V_{IN1} = V_{IN2} = V_{INHIBIT}$ = 0.8 V		0		mA
		T_A = +25°C, $V_{IN1} = V_{IN2} = V_{INHIBIT}$ = 2.0 V		−15		

AC CHARACTERISTICS ($0 \leq T_A \leq 70°C$, Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Positive Slew Rate	0 pF ≤ C_L ≤ 2500 pF, $R_L \geq 3$ kΩ	4.0	15	30	V/μs
	Negative Slew Rate	0 pF ≤ C_L ≤ 2500 pF, $R_L \geq 3$ kΩ	−30	−15	−4.0	V/μs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

NOTES:
2. The operating temperature range for the 9616 is −55°C to +125°C and 9616E is 0°C to + 70°C.
3. An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate. No external capacitor is needed to meet RS-232-C over the operating temperature range of 0°C to + 70°C.

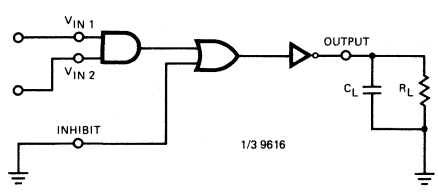
9616C

EIA RS232-C

ELECTRICAL CHARACTERISTICS (V_{CC} = ±12 V ±10 %, over operating temperature range, See Test Circuit, R_L = 3 kΩ, unless otherwise specified)

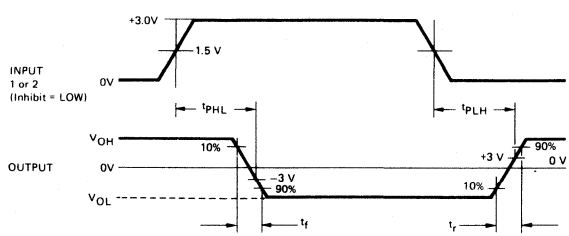
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{OH}	Output HIGH Voltage	V_{IN1} and/or V_{IN2} = $V_{INHIBIT}$ = 0.8V	5.0	6.0	7.5	V
V_{OL}	Output LOW Voltage	V_{IN1} = V_{IN2} = $V_{INHIBIT}$ = 2.0 V	−7.5	−6.0	−5.0	V
I_{SC+}	Positive Output Short-Circuit Current	R_L = 0Ω, V_{IN1} and/or V_{IN2} = $V_{INHIBIT}$ = 0.8 V		−17		mA
I_{SC-}	Negative Output Short-Circuit Current	R_L = 0Ω, V_{IN1} = V_{IN2} = $V_{INHIBIT}$ = 2.0 V		17		mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	V_{IN1} = V_{IN2} = 2.4 V			40	μA
I_{IL}	Input LOW Current	V_{IN1} = V_{IN2} = 0.4 V	−1.6	−1.2		mA
I+	Total Positive Supply Current	V_{IN1} = V_{IN2} = $V_{INHIBIT}$ = 0.8 V		15		mA
		V_{IN1} = V_{IN2} = $V_{INHIBIT}$ = 2.0 V		7.5		mA
I−	Total Negative Supply Current	V_{IN1} = V_{IN2} = $V_{INHIBIT}$ = 0.8 V		0		mA
		V_{IN1} = V_{IN2} = $V_{INHIBIT}$ = 2.0 V		−15		mA
R_{OUT}	Output Resistance, Power Off	−2.0 V ≤ V_{OUT} ≤ +2.0 V. All Inputs and Supplies Grounded.	300			Ω
AC CHARACTERISTICS						
	Positive Slew Rate	0 pF ≤ C_L ≤ 2500 pF, R_L ≥ 3 kΩ	4.0	15	30	V/μs
	Negative Slew Rate	0 pF ≤ C_L ≤ 2500 pF, R_L ≥ 3 kΩ	−30	−15	−4.0	V/μs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

AC TEST CIRCUIT



Note: Omit V_{IN2} for channel "C".

VOLTAGE WAVEFORMS



Frequency = 50 kHz
Pulse Width = 20 μs
t_r & t_f = 10 ± 5 ns

9617

TRIPLE EIA RS-232-C LINE RECEIVER

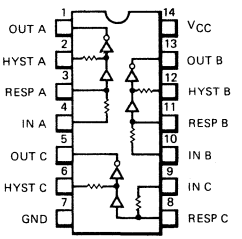
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9617 is a monolithic Triple Line Receiver constructed using the Fairchild Planar* process. It is designed to meet the terminator electrical requirements of EIA RS-232-C and CCITT V.24. It receives line signals produced by the 9616, an EIA/CCITT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground.

For the hysteresis mode connect the RESP pin to the HYST pin, for the slicing mode leave these pins open.

- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



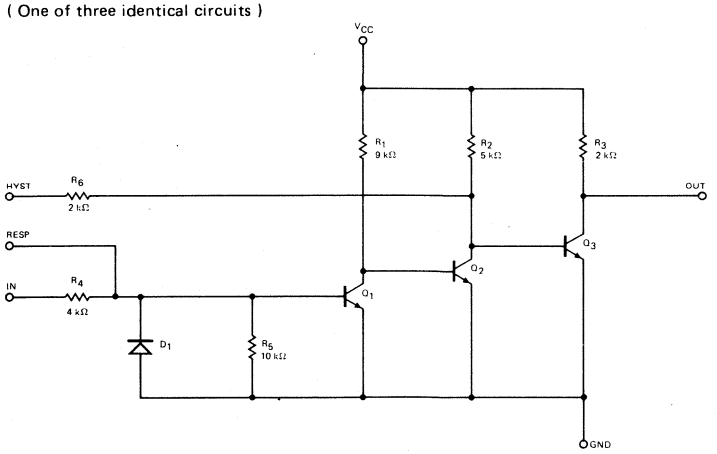
ORDER INFORMATION

TYPE	PART NO.
9617C	9617DC
9617C	9617PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 V
Input Voltage	±25 V
Output Current	25 mA
Internal Power Dissipation	630 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperatures	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Slodering, 10 s)	260°C

EQUIVALENT CIRCUIT (One of three identical circuits)



*Planar is a patented Fairchild process.

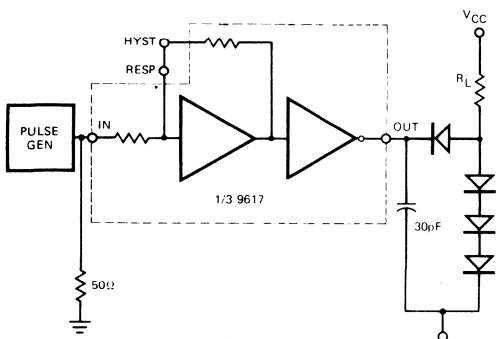
9617C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V ±5%, T_A = 25°C Response Pin Open, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	V_I = ±25V	3.0	4.0	7.0	kΩ
E_L	Input Voltage	Open Circuit		0.2	2.0	V
V_{TH+}	Upper Input Threshold Voltage	RESP – HYST Connected	1.75	2.0	2.25	V
V_{TH-}	Lower Input Threshold Voltage	RESP – HYST Connected	0.75	0.85	1.25	V
V_{THX}	Open Loop Threshold Voltage		0.4	1.0	1.2	V
V_{OH}	Output HIGH Voltage	V_{IN} = –3.0V, 0V or open circuit V_{CC} = 4.5V, I_L = –200μA	2.4	3.0		V
V_{OL}	Output LOW Voltage	V_{IN} = +3.0V V_{CC} = 4.5V, I_L = 8.0mA		0.3	0.4	V
I_{SC}	Output Short Circuit Current	V_O = 0V		2.5		mA
I_{CC}	Supply Current	V_{CC} = +5.5V, V_{IN} = 5.0V		12		mA
t_{PLH}	Propagation Delay Time	R_L = 3.9kΩ, Note 1		60		ns
t_r	Rise Time	R_L = 3.9kΩ, Note 1		150		ns
t_{PHL}	Propagation Delay Time	R_L = 390Ω, Note 1		40		ns
t_f	Fall Time	R_L = 390Ω, Note 1		50		ns

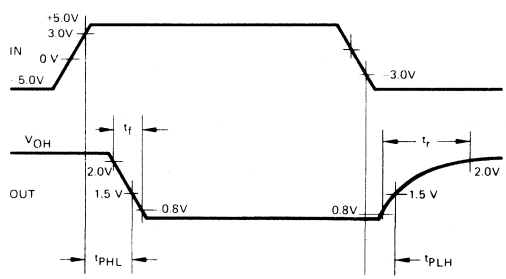
Note 1. V_{CC} = 5.0 V, See AC Test Circuit and waveforms

AC TEST CIRCUIT



All diodes FDH600 or equivalent.

VOLTAGE WAVEFORMS



Input Pulse Characteristics:
PRR = 1 MHz
PW = 500 μs
t_r = t_f = 10 ± 2ns (10% to 90%)

NOTE: Wiring capacitance should be minimized between outputs, hysteresis and response pins.

9620
DUAL DIFFERENTIAL LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9620 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of HIGH level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output. In addition to line reception the 9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including ECL, CTL, HLLDTL, RTL and TTL. HLLDTL output logic levels can be provided by tieing the output to V_{CC2} (+12 V) through a resistor. The outputs can also be wired-OR. The 9620 offers the advantages of logic compatible voltages (+5 V, +12 V), TTL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components. See note 2.

For new designs, the 9615 or 9613 is recomended as a functional equivalent of the 9620.

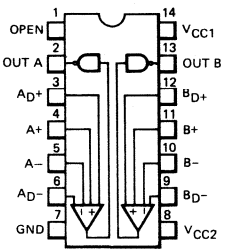
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **WIRED-OR CAPABILITY**
- **DIRECT INPUTS (A_D, B_D)**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature Range	
Military (9620)	−55°C to +125°C
Commercial (9620C)	0°C to +70°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperatures	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 1)	670 mW

NOTE:
1. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

CONNECTION DIAGRAM
14-LEAD
(TOP VIEW)
PACKAGE OUTLINE 6A 9A 3I
PACKAGE CODE D P F

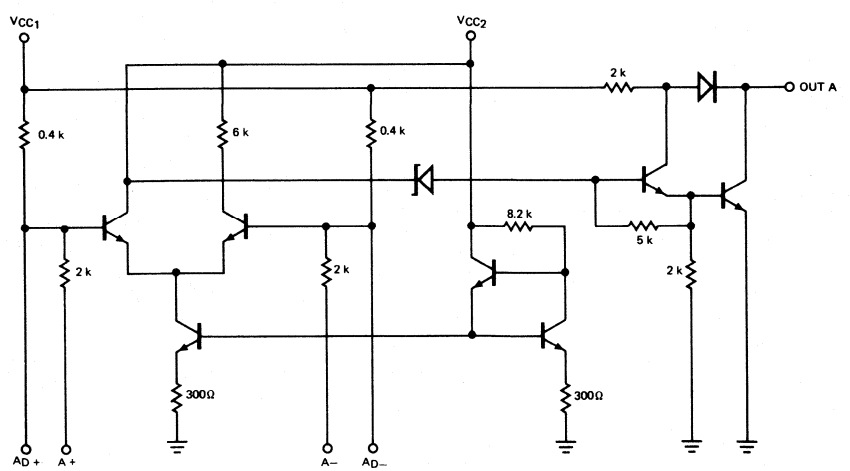


ORDER INFORMATION

TYPE	PART NO.
9620	9620DM
9620C	9620PC
9620C	9620DC
9620	9620FM

11

EQUIVALENT CIRCUIT



9620

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V ±10%, V_{CC2} = 12.0 V ±10%)

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS	
		−55°C		+25°C			+125°C				
		MIN	MAX	MIN	TYP	MAX	MIN	MAX			
V_{OL}	Output LOW Voltage		0.40		0.21	0.40		0.45	V	V_{CC1} = 4.5 V I_{OL} = 15.0 mA	V_{CC2} = 10.8 V *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.8		3.0			2.9		V	V_{CC1} = 4.5 V I_{OH} = −0.2 mA	V_{CC2} = 10.8 V *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CEX} = 13.2 V	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V V_{Input} = 0 V†
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V
†V_{CM}	Common Mode Voltage	−15	15	−15	±17.5	15	−15	15	V	V_{CC1} = 5.0 V *V_{DIFF} = 2.0 V	V_{CC2} = 12.0 V
I_{VCC1}	5 V Supply Current		13		8.2	13		13	mA	V_{CC1} = 5.5 V V_{CC2} = 13.2 V	+Input = 5.5 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.0		5.6	8.0		8.0	mA	V_{CC1} = 5.5 V V_{CC2} = 13.2 V	+Input = 5.5 V −Input = 0 V
t_{PLH}	Turn Off Time				35	50			ns	R_L = 3.9 kΩ, C_L = 3.0 pF, see Fig. 1	
t_{PHL}	Turn On Time				20	50			ns	R_L = 390 Ω, C_L = 30 pF, see Fig. 1	

†All Input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

9620C

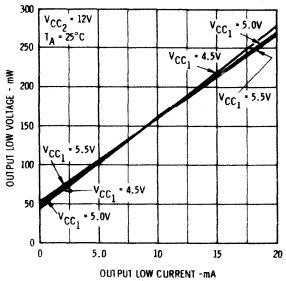
ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V ±5%, V_{CC2} = 12.0 V ±5%)

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS	
		0°C		+25°C			+70°C				
		MIN	MAX	MIN	TYP	MAX	MIN	MAX			
V_{OL}	Output LOW Voltage		0.45		0.25	0.45		0.50	V	V_{CC1} = 4.75 V I_{OL} = 15.0 mA	V_{CC2} = 11.4 V *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.8		3.0	3.3		2.9		V	V_{CC1} = 4.75 V I_{OH} = −0.2 mA	V_{CC2} = 12.6 V *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CEX} = 5.25 V	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V V_{Input} = 0 V†
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	V_{CC1} = 4.75 V	V_{CC2} = 12.6 V
†V_{CM}	Common Mode Voltage	−12	12	−12	±17.5	12	−12	12	V	V_{CC1} = 5.0 V *V_{DIFF} = 2.0 V	V_{CC2} = 12.0 V
I_{VCC1}	5 V Supply Current		13.5		8.2	13.5		13.5	mA	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	+Input = 5.25 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.5		5.6	8.5		8.5	mA	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	+Input = 5.25 V −Input = 0 V
t_{PLH}	Turn Off Time				35	75			ns	R_L = 3.9 kΩ, C_L = 30 pF, See Fig. 1	
t_{PHL}	Turn On Time				20	75			ns	R_L = 390 Ω, C_L = 30 pF, see Fig. 1	

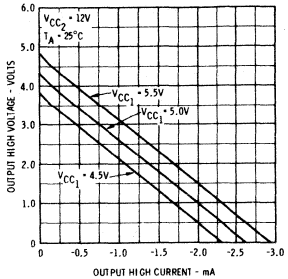
†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

TYPICAL PERFORMANCE CURVES FOR 9620 AND 9620C

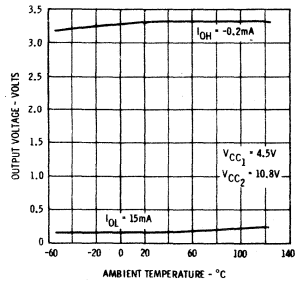
TYPICAL OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT LOW CURRENT



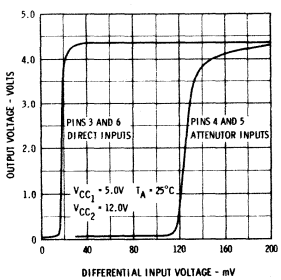
TYPICAL OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



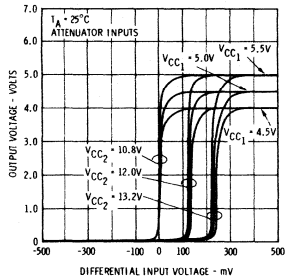
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



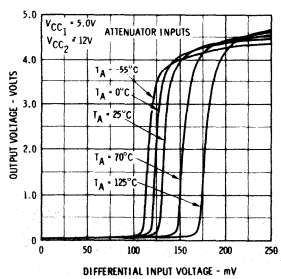
TYPICAL V_{OUT} AS A FUNCTION OF V_{DIFF} TRANSFER CHARACTERISTIC



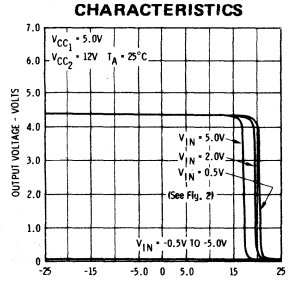
TYPICAL V_{OUT} AS A FUNCTION OF V_{DIFF} TRANSFER CHARACTERISTIC



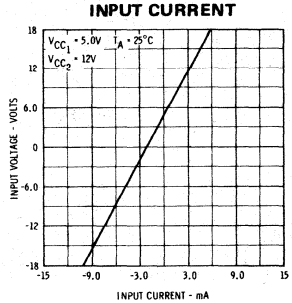
TYPICAL V_{OUT} AS A FUNCTION OF V_{DIFF} TRANSFER CHARACTERISTIC



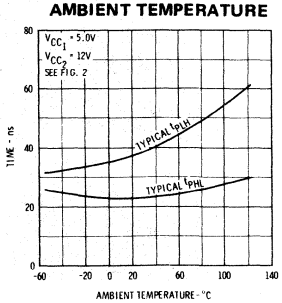
TYPICAL V_{OUT} AS A FUNCTION OF V_{CM} CHARACTERISTICS



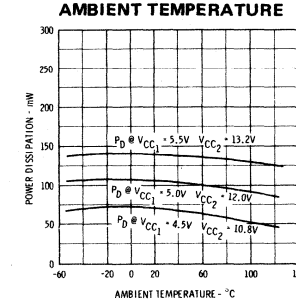
INPUT VOLTAGE AS A FUNCTION OF INPUT CURRENT



SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



STANDARD USAGE

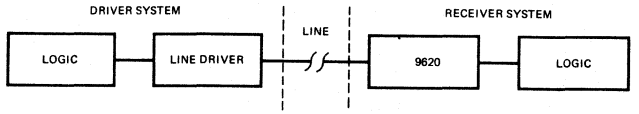
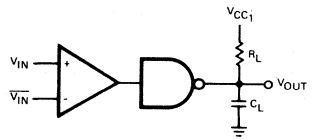
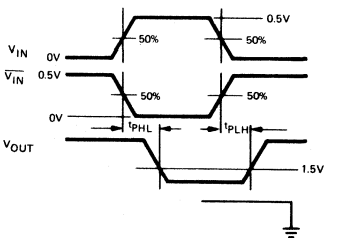


Fig. 1 AC TEST CIRCUIT

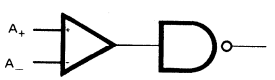


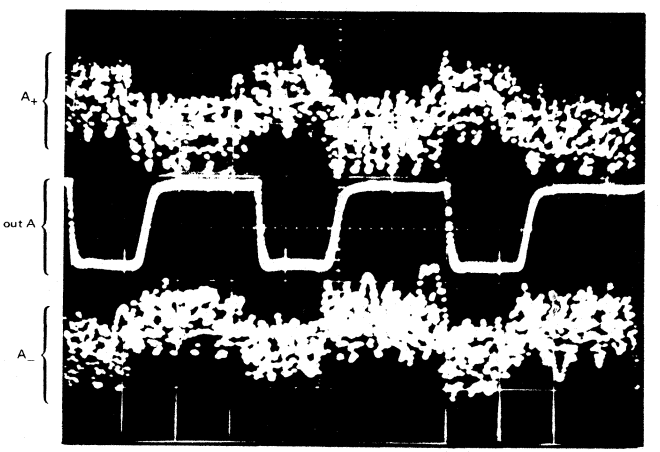
V_{CC1} = 5.0 V
V_{CC2} = 12 V

WAVEFORMS



Photograph of a 9620 switching differential data in the presence of high common mode noise.

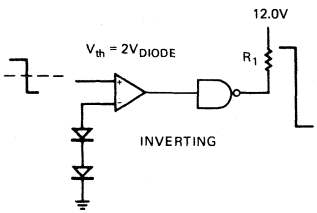




VERT = 2.0 V/div. HORIZ = 50 ns/div.

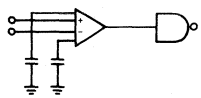
APPLICATIONS (Cont'd)

DIGITAL COMPARATOR WITH DIODE REFERENCE AND HIGH LEVEL LOGIC OUT

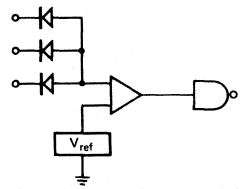


$R_1 \geq 750\ \Omega$

DIGITAL DIFFERENTIAL LINE RECEIVER WITH INPUTS ROLLED OFF

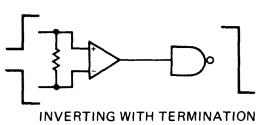


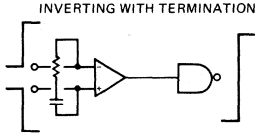
EXPANDED INTERFACE



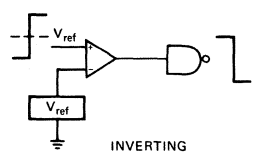
V_{ref} = Resistor, Diodes, or Supply

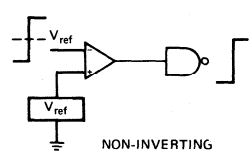
DIGITAL DIFFERENTIAL AMPLIFIER (Line Receiver)



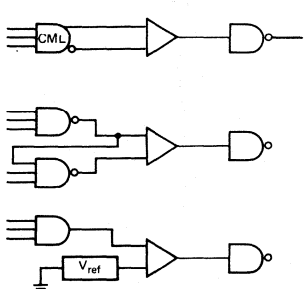


DIGITAL COMPARATOR

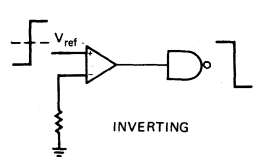


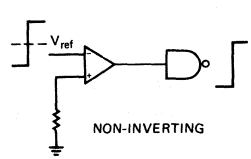


INTERFACING METHODS



DIGITAL COMPARATOR WITH RESISTIVE DIVIDER AS REFERENCE

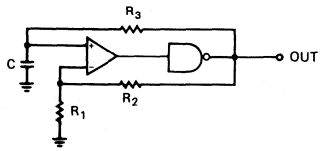




11

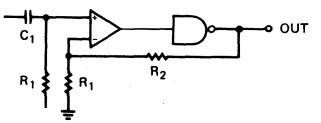
APPLICATIONS

MULTIVIBRATOR



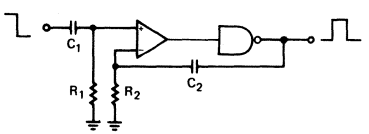
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $T = 1.3\ R_3C$

AC COUPLED DIGITAL AMPLIFIER WITH HYSTERESIS



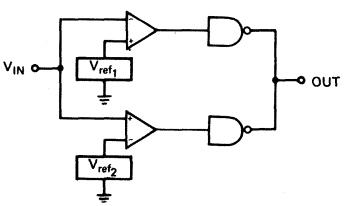
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$

MONOSTABLE MULTIVIBRATOR NEGATIVE EDGE TRIGGERING



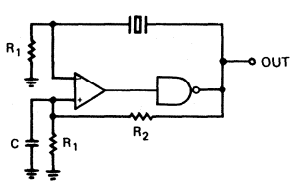
TYPICALLY
$C_1 = 0.1\ \mu F$, $R_1 = 1.2\ k\Omega$, $R_2 = 1.0\ k\Omega$
Pulse Width = 50 ns + $3.15 \times 10^3\ C_2$

DOUBLE-ENDED COMPARATOR



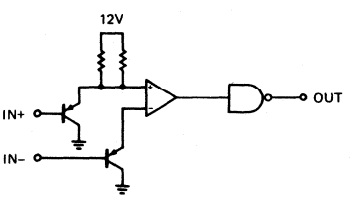
$V_{OH} = V_{Ref_1} < V_{IN} < V_{Ref_2}$

CRYSTAL CONTROLLED MULTIVIBRATOR



TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $C = \frac{R_2}{1000}$

HIGH INPUT IMPEDANCE LINE RECEIVER (Positive Signals Only)



9621
DUAL LINE DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair are provided. The output has the capability of driving high capacitance loads.

For new designs, the 9614 and 9612 are recommended as functional equivalents of the 9621.

- **TTL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

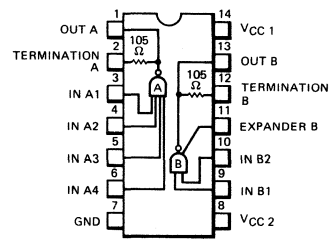
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature Range	
Military (9621)	−55°C to +125°C
Commercial (9621C)	0°C to 70°C
V_{CC1} Pin Potential to Ground Pin	+3.8V to +8V
Input Voltage	−0.5V to +15V
Voltage Applied to Outputs	−2V to +V_{CC1} +1V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15V
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 1)	670 mW

NOTE:
1. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

CONNECTION DIAGRAMS
14-LEAD
(TOP VIEW)

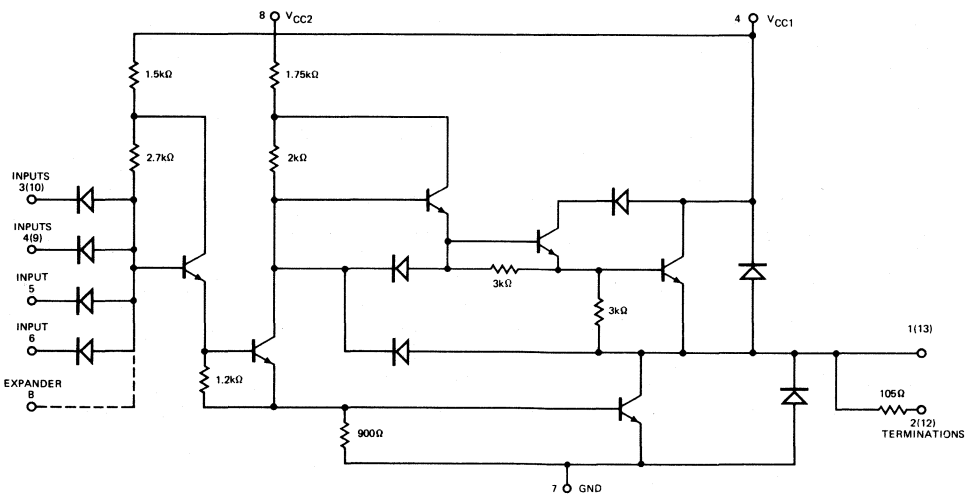
PACKAGE OUTLINE 6A 9A 3I
PACKAGE CODE D P F



ORDER INFORMATION

TYPE	PART NO.
9621	9621DM
9621	9621FM
9621C	9621DC
9621C	9621PC

EQUIVALENT CIRCUIT (ONE SIDE ONLY)



ELECTRICAL CHARACTERISTICS (V_{CC1} = +5.0 V ± 10%, V_{CC2} = +12 V ± 10%)

SYMBOL	NOTES	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS	
			−55°C		+25°C			+125°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output LOW Voltage		350		200	350		400	mV	I_{OL} = 20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
V_{OH}		Output HIGH Voltage	4.0		4.0	4.3		4.0		V	I_{OH} = −20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{SC}	2	Output "Short Circuit" Current			−180	−420				mA	V_{OUT} = 0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{OL}	2	Output LOW Current			150	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_F		Input Forward Current		−1.8		−1.15	−1 8		−1.8	mA	V_F = 0 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_R		Input Reverse Current		2.0		<1.0	2.0		5.0	μA	V_R = 5.5 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
V_{OLR}	3	Resistive Output LOW Voltage				380	500			mV	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	3	Resistive Output HIGH Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	4	Clamped Output LOW Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	4	Clamped Output HIGH Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{PLH}	5	Turn-Off Time				30	150			ns	C_L = 5000 pF See AC Test Circuit	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{PHL}	5	Turn-On Time				80	150			ns		
t_{PLH}		Turn-Off Time				13	25			ns	C_L = 30 pF See AC Test Circuit	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{PHL}		Turn-On Time				9	25			ns		
V_{IL}		Input LOW Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.5 V, V_{CC2} = 10.8 V	
V_{IH}		Input HIGH Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.5 V, V_{CC2} = 13.2 V	

NOTES:

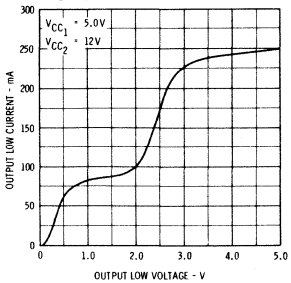
2. Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
3. Test output resistance including 105Ω output resistor.
4. Tests output clamp diodes.
5. With both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for Dual In-line package (θ_{JA} = 95°C/W) or 300 kHz for Flatpak (θ_{JA} = 165°C/W).
6. Maximum frequency = 500 kHz with both sides loaded at T_A = +75°C.

ELECTRICAL CHARACTERISTICS (V_{CC1} = +5.0 V ± 5%, V_{CC2} = +12 V ± 5%)

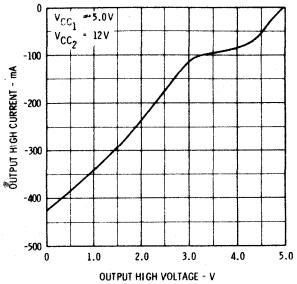
SYMBOL	NOTES	CHARACTERISTIC	LIMITS								
			0°C		+25°C			+75°C			
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}		Output LOW Voltage		400		200	400		450	mV	I_{OL} = 20 mA, V_{CC1} = 4.75 V, V_{CC2} = 11.4 V
V_{OH}		Output HIGH Voltage	4.2		4.2	4.4		4.2		V	I_{OH} = −20 mA, V_{CC1} = 4.75 V, V_{CC2} = 11.4 V
I_{SC}	2	Output "Short Circuit" Current			−100	−420				mA	V_{OUT} = 0 V, V_{CC1} = 4.75 V, V_{CC2} = 11.4 V
I_{OL}	2	Output LOW Current			75	200				mA	V_{OUT} = 5.0 V, V_{CC1} = 4.75 V, V_{CC2} = 11.4 V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V_F = 0 V, V_{CC1} = 5.25 V, V_{CC2} = 12.6 V
I_R		Input Reverse Current		5.0		<1.0	5.0		10.0	μA	V_R = 5.5 V, V_{CC1} = 5.25 V, V_{CC2} = 12.6 V
V_{OLR}	3	Resistive Output LOW Voltage				380	500			mV	I_{OL} = 2.8 mA, V_{CC1} = 5.0 V, V_{CC2} = 12.0 V
V_{OHR}	3	Resistive Output HIGH Voltage			4.0	4.2				V	I_{OH} = −2.3 mA, V_{CC1} = 5.0 V, V_{CC2} = 12.0 V
V_{OLC}	4	Clamped Output LOW Voltage				−1.0	−2.0			V	I_{OL} = −20 mA, V_{CC1} = 5.0 V, V_{CC2} = 12.0 V
V_{OHC}	4	Clamped Output HIGH Voltage				6.0	7.0			V	I_{OH} = 20 mA, V_{CC1} = 5.0 V, V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open, V_{CC1} = 5.25 V, V_{CC2} = 12.6 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA	
t_{PLH}	6	Turn-Off Time				30	200			ns	C_L = 5000 pF, See AC Test Circuit, V_{CC1} = 5.0 V, V_{CC2} = 12.0 V
t_{PHL}	6	Turn-On Time				80	200			ns	
t_{PLH}		Turn-Off Time				13	40			ns	C_L = 30 pF, See AC Test Circuit, V_{CC1} = 5.0 V, V_{CC2} = 12.0 V
t_{PHL}		Turn-On Time				9	40			ns	
V_{IL}		Input LOW Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V
V_{IH}		Input HIGH Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.75 V, V_{CC2} = 11.4 V

TYPICAL ELECTRICAL CHARACTERISTICS FOR 9621 AND 9621C

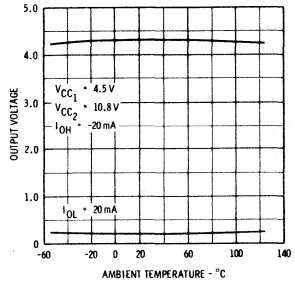
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



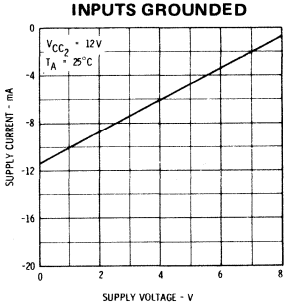
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



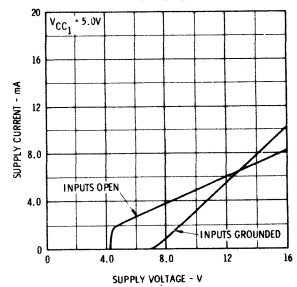
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



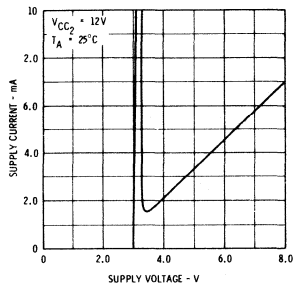
SUPPLY CURRENT AS A FUNCTION OF INPUTS GROUNDED



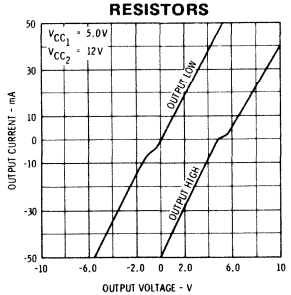
SUPPLY CURRENT AS A FUNCTION OF INPUTS OPEN



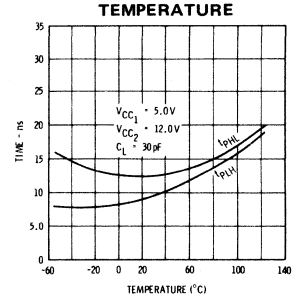
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



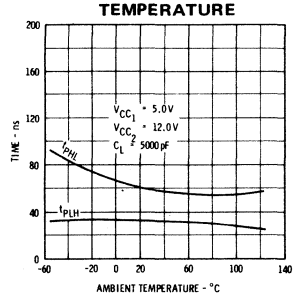
TYPICAL OUTPUT IMPEDANCE WITH BACK MATCHING RESISTORS



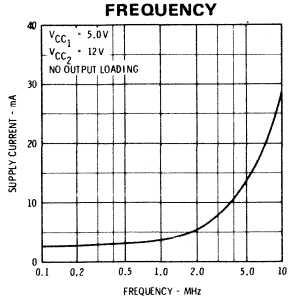
SWITCHING TIME AS A FUNCTION OF TEMPERATURE



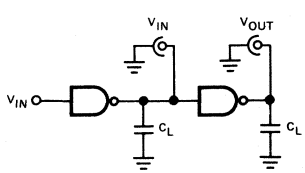
SWITCHING TIME AS A FUNCTION OF TEMPERATURE



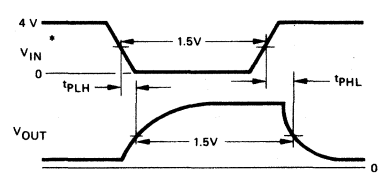
SUPPLY CURRENT AS A FUNCTION OF FREQUENCY



AC TEST CIRCUIT



WAVEFORMS



* Frequency = 100 kHz
Pulse Width = 5 μs
t_r & $t_f \leq$ 10 ns

DESCRIPTION OF REFLECTION DIAGRAM USAGE

The reflections on any line may be found by using the following procedure:

1. Draw the driver output characteristics for both the HIGH state and the LOW state on an I–V graph in the same manner as the reflection diagram.
2. Draw the receiver input characteristic on the same graph. The two points of intersection of the receiver and driver characteristics are the two dc operating points.
3. Choose to analyze either the reflections for the output going LOW or HIGH. In the example chosen the negative transition is analyzed.
4. Draw a line with a slope equal to the impedance of the line to be used, (Z_0 = 100 Ω in the example), from the HIGH state operating point (labeled A on our graph) to the LOW state output device characteristic (B_1). B_1 equals the conditions at the driver output immediately after turn-on.
5. Reverse the slope of Z_0 and sketch it from B_1 to the receiver input characteristic (C_1). C_1 equals the conditions at the receiver when the wavefront B_1 first reaches it.
6. By continuing this procedure of reversing the slope of Z_0 at each node all the reflections (B_1, C_1, B_2, C_2, B_3, C_3 - - - B_N, C_N), where B_X is the voltage at the driver and C_X is the voltage at the receiver, can be found.

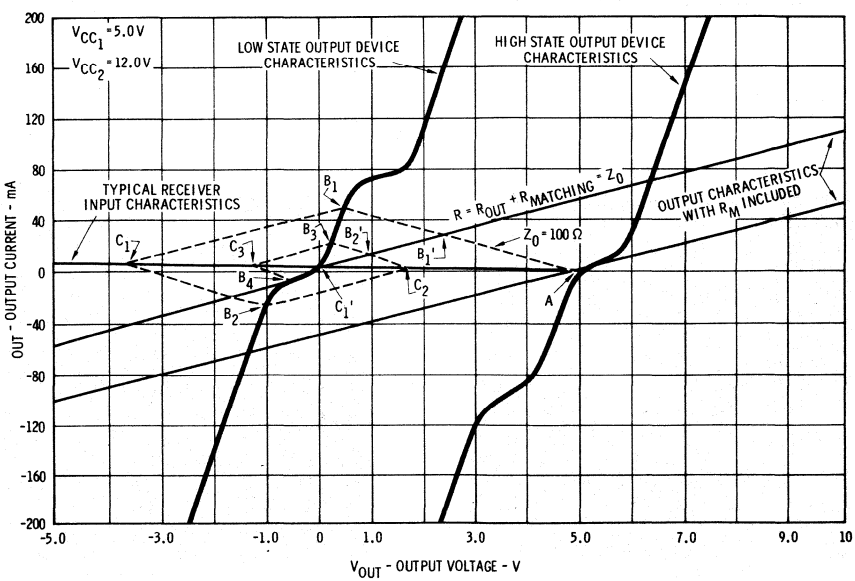
The same procedure is used to check the reflections when switching the output HIGH.

BACK-MATCHING, also referred to as reverse termination, offers several advantages to the user. It reduces the system power by not requiring the high current for resistive termination and it reduces the dc line losses because IR drops in the line become minimum.
To back-match any line (output switching low):

1. Measure the output resistance, R_{out}, from the LOW state operating point to B.
2. Subtract R_{out} from Z. (R_{out} + R_M = Z_0). This value R_M, is the required back-matching resistance.
3. Place R_M in series with the output of driver.
4. The reflections that occur on the line with R_M inserted can be treated in the same manner as the general case. The results are B_1, and C_1, and the receiver will not see any reflections.

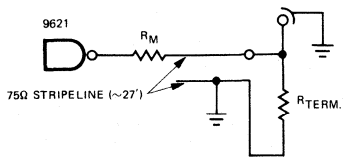
When switching the line differentially R_M + R_{out} = $Z_{0/2}$. The matched output characteristics of the 9621 make it possible to back-match effectively and require analysis of switching only one state.

TYPICAL REFLECTION DIAGRAM*



* GRAPHICAL ANALYSIS
First Presented by John B. James of I.C.T. (Eng.) LTD.

REFLECTION TEST CIRCUIT

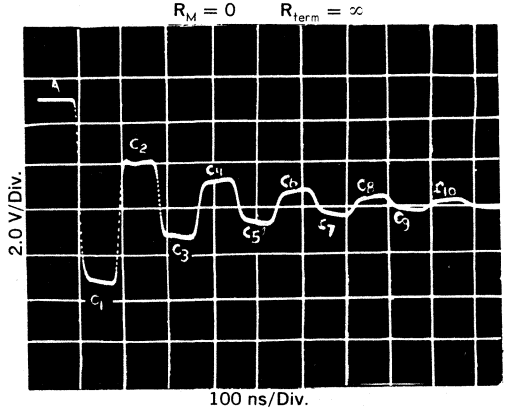


The reflections are two delay's of the line wide. R_{term} is the total impedance seen at the receiving end.

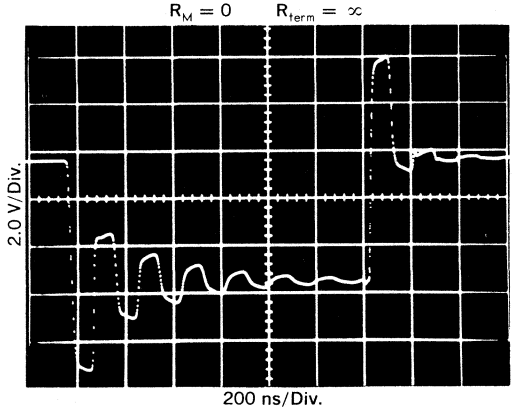
BACK MATCHING TABLE

Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

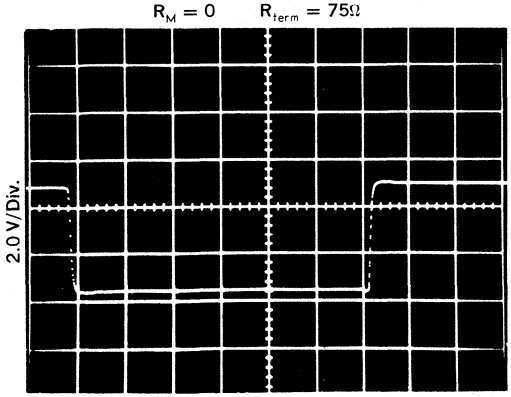
$R_M = 0$ $R_{term} = \infty$



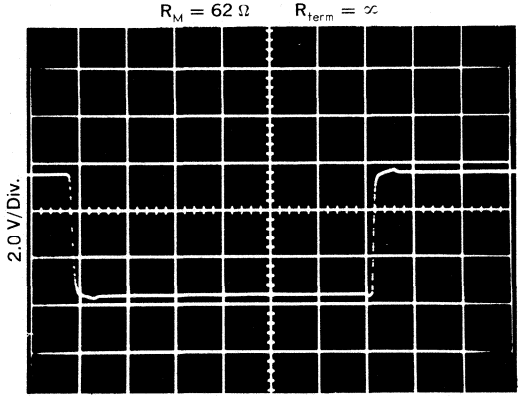
$R_M = 0$ $R_{term} = \infty$



$R_M = 0$ $R_{term} = 75\Omega$



$R_M = 62\ \Omega$ $R_{term} = \infty$



9622
DUAL LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9622 is a Dual Line Receiver designed to discriminate a worst case logic swing of 2.0V from a ±10V common mode noise signal or ground shift. A 1.5V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ±5% (75 mV) over the military and industrial temperature ranges.

The 9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S_3 (Note 1). A 130Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output HIGH level can be increased to +12V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.

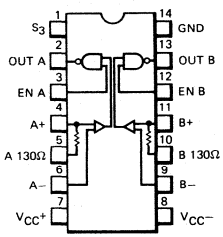
- **TTL COMPATIBLE THRESHOLD VOLTAGE**
- **INPUT TERMINATING RESISTORS**
- **CHOICE OF OUTPUT STATE WITH INPUTS OPEN**
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE**
- **WIRE-OR CAPABILITY**
- **ENABLE INPUTS**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Operating Temperature	
Military (9622)	−55°C to +125°C
Commercial (9622C)	0°C to +70°C
Internal Power Dissipation (Note 2)	
Hermetic DIP, Molded DIP	670 mW
Flatpak	570 mW
V_{CC}+ Pin Potential to Ground Pin	−0.5V to +7V
Input Voltage	±15V
Voltage Applied to Outputs for Output HIGH State	−0.5V to +13.2V
V_{CC}− Pin Potential to Ground Pin	−0.5V to −12V
Enable Pin Potential to Ground Pin	−0.5V to +15V
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP, (Soldering, 10 s)	260°C

NOTE
1. S_3 connected to V_{CC}−open inputs causes output to be HIGH.
   S_3 connected to Ground−open inputs causes output to be LOW.
2. Rating applies to ambient temperature up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for teh Hermetic DIP and 7.1 mW/°C for the Flatpak.

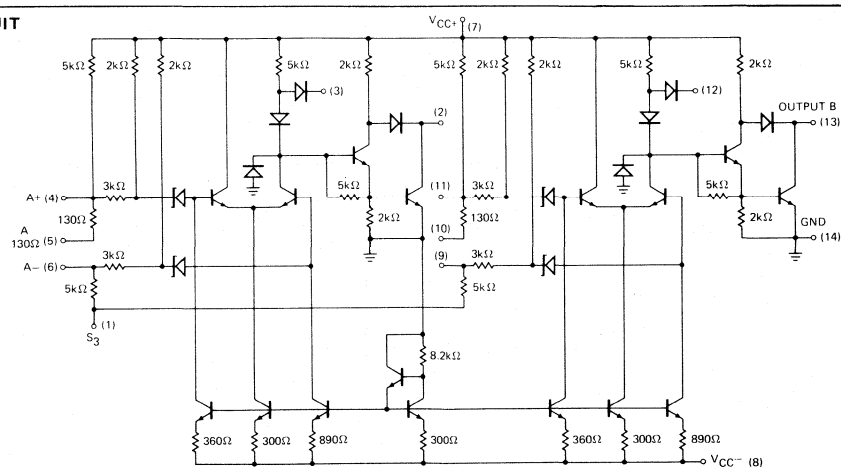
CONNECTION DIAGRAMS
14-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
9622	**9622DM**
9622	**9622FM**
9622C	**9622DC**
9622C	**9622PC**

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{CC}+ = 5.0\ V \pm 10\%$, $V_{CC}- = -10\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		−55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		0.40		0.17	0.40		0.40	Volts	$V_{CC+} = 4.5\ V$ $V_{CC-} = -11\ V$ $*V_{DIFF} = 2.0\ V$ $I_{OL} = 12.4\ mA$
V_{OH}	Output HIGH Voltage	2.8		3.0	3.3		2.9		Volts	$V_{CC+} = 4.5\ V$ $V_{CC-} = -9.0\ V$ $*V_{DIFF} = 1.0\ V$ $I_{OH} = -0.2\ mA$
I_{CEX}	Output Leakage Current		50			100		200	μA	$V_{CC+} = 4.5\ V$ $V_{CC-} = -11\ V$ $*V_{DIFF} = 1.0\ V$ $V_{CEX} = 12\ V$
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.1	−1.3	−3.1	mA	$V_{CC+} = 5.0\ V$ $V_{CC-} = -10\ V$ $*V_{DIFF} = 1.0\ V$ $V_{SC} = 0\ V$
$I_{R\,(ENABLE)}$	Enable Input Leakage Current					2.0		5.0	μA	$V_{CC+} = 4.5\ V$ $V_{CC-} = -11\ V$ $S_3 = 4.5\ V$ $V_R = 4.0\ V$
$I_{F\,(ENABLE)}$	Enable Input Forward Current		−1.5		−0.96	−1.5		−1.5	mA	$V_{CC+} = 5.5\ V$ $V_{CC-} = -9.0\ V$ $S_3 = 0\ V$ $V_F = 0\ V$
$I_{F\,(+Input)}$	+Input Forward Current		−2.3		−1.67	−2.1		−2.0	mA	$V_{CC+} = 5.0\ V$ $V_{CC-} = -10\ V$ −Input = GND $V_F = 0\ V$
$I_{F\,(-Input)}$	−Input Forward Current		−2.6		−1.87	−2.4		−2.3	mA	V_{CC+}, $S_3 = 5.0\ V$ $V_{CC-} = -10\ V$ +Input = GND $V_F = 0\ V$
$V_{IL\,(ENABLE)}$	Input LOW Voltage		1.3		1.4	1.0		0.7	Volts	$V_{CC+} = 5.0\ V \pm 10\%$ $V_{CC-} = -10\ V \pm 10\%$
V_{TH}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	Volts	$V_{CC+} = 5.0\ V \pm 10\%$ $V_{CC-} = -10\ V \pm 10\%$
V_{CM}	Common Mode Voltage			−10	±12	+10			Volts	$V_{CC+} = 5.0\ V$ $V_{CC-} = -10\ V$ $*V_{DIFF} = 1.0\ V$ or $2.0\ V$
$R_{130\Omega}$	Terminating Resistance			100	130	175			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	$V_{CC+} = 5.5\ V$ $V_{CC-} = -11\ V$ S_3, +Inputs = 5.5 V, −Inputs = 0 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	$V_{CC+} = 5.5\ V$ $V_{CC-} = -11\ V$ S_3, +Inputs = 5.5 V, −Inputs = 0 V
t_{PLH}	Turn-Off Time				38	50			ns	$V_{CC+} = 5.0\ V$ $V_{CC-} = -10\ V$ V_{IN} 0→3 V, $R_L = 3.9\ k\Omega$, $C_L = 30\ pF$ See AC Test Circuit
t_{PHL}	Turn-On Time				35	50			ns	$V_{CC+} = 5.0\ V$ $V_{CC-} = -10\ V$ V_{IN} 0→3.0 V, $R_L = 0.39\ k\Omega$, $C_L = 30\ pF$ See AC Test Circuit

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

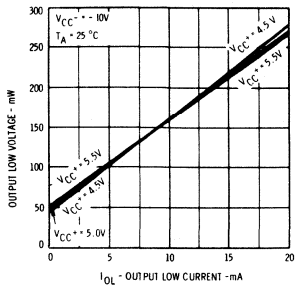
ELECTRICAL CHARACTERISTICS ($V_{CC}+$ = 5.0 V ± 5%, $V_{CC}-$ = −10 V ± 5%)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	70°C MIN.	70°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output LOW Voltage		0.45		0.17	0.45		0.45	Volts	$V_{CC}+$ = 4.75 V $V_{CC}-$ = −10.5 V *V_{DIFF} = 2.0 V I_{OL} = 14.1 mA
V_{OH}	Output HIGH Voltage	2.9		3.0	3.3		2.9		Volts	$V_{CC}+$ = 4.75 V $V_{CC}-$ = −9.5 V *V_{DIFF} = 1.0 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		80			100		200	μA	$V_{CC}+$ = 4.75 V $V_{CC}-$ = −10.5 V *V_{DIFF} = 1.0 V V_{CEX} = 5.25 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.2	−1.3	−3.1	mA	$V_{CC}+$ = 5.0 V $V_{CC}-$ = −10 V *V_{DIFF} = 1.0 V V_{SC} = 0 V
$I_{R(ENABLE)}$	Enable Input Leakage Current					5		10	μA	$V_{CC}+$ = 4.75 V $V_{CC}-$ = −10.5 V S_3 = 4.75 V V_R = 4.0 V
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−.96	−1.5		−1.5	mA	$V_{CC}+$ = 5.25 V $V_{CC}-$ = −9.5 V S_3 = 0 V V_F = 0 V
$I_{F(+Input)}$	+Input Forward Current		−2.6		−1.67	−2.4		−2.3	mA	$V_{CC}+$ = 5.0 V $V_{CC}-$ = −10 V −Input = GND V_F = 0 V
$I_{F(-Input)}$	−Input Forward Current		−2.9		−1.87	−2.7		−2.6	mA	$V_{CC}+$, S_3 = 5.0 V $V_{CC}-$ = −10 V +Input = GND V_F = 0 V
$V_{IL(ENABLE)}$	Input LOW Voltage		1.2		1.4	1.0		0.85	Volts	$V_{CC}+$ = 5.0 V ±5 % $V_{CC}-$ = −10 V ±5 %
V_{TH}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	Volts	$V_{CC}+$ = 5.0 V ±5 % $V_{CC}-$ = −10 V ±5 %
V_{CM}	Common Mode Voltage			−7.5	±12	+7.5			Volts	$V_{CC}+$ = 5.0 V $V_{CC}-$ = −10 V *V_{DIFF} = 1.0 V or 2.0 V
$R_{130\Omega}$	Terminating Resistance			91	130	185			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	$V_{CC}+$ = 5.25 V $V_{CC}-$ = −10.5 V S_3, +Inputs = 5.25 V, −Inputs = 0 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	$V_{CC}+$ = 5.25 V $V_{CC}-$ = −10.5 V S_3, +Inputs = 5.25 V, −Inputs = 0 V
t_{PLH}	Turn-Off Time				38	100			ns	$V_{CC}+$ = 5.0 V $V_{CC}-$ = −10 V V_{IN} 0→3.9 V, R_L = 3.9 kΩ, C_L = 30 pF See AC Test Circuit
t_{PHL}	Turn-On Time				35	100			ns	$V_{CC}+$ = 5.0 V $V_{CC}-$ = −10 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF See AC Test Circuit

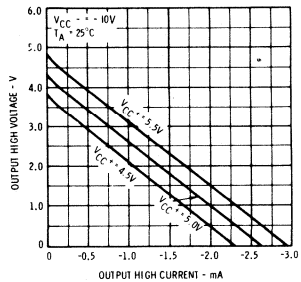
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−

TYPICAL PERFORMANCE CURVES FOR 9622 AND 9622C

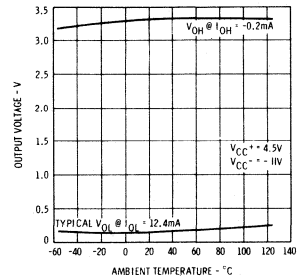
OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT LOW CURRENT



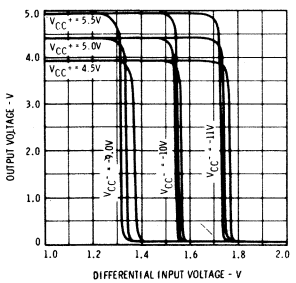
OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



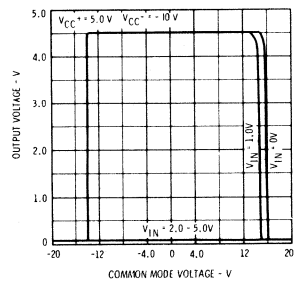
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



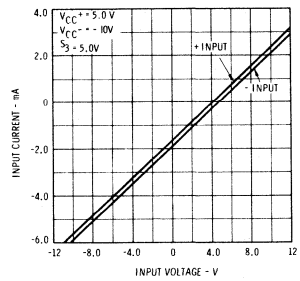
$V_{OUT} - V_{DIFF}$ TRANSFER CHARACTERISTICS



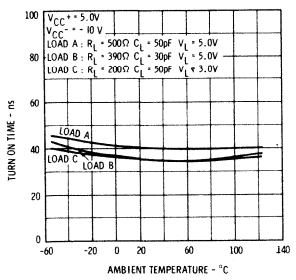
OUTPUT VOLTAGE AS A FUNCTION OF COMMON MODE VOLTAGE



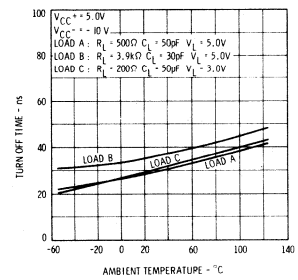
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



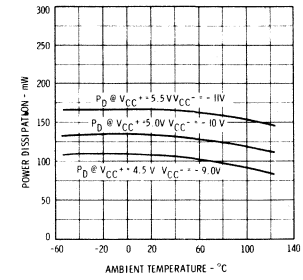
TURN ON TIME AS A FUNCTION OF AMBIENT TEMPERATURE



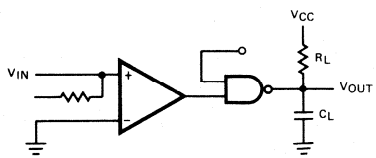
TURN OFF TIME AS A FUNCTION OF AMBIENT TEMPERATURE



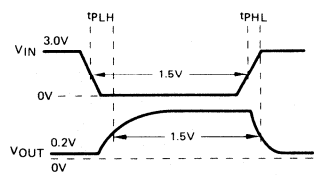
POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



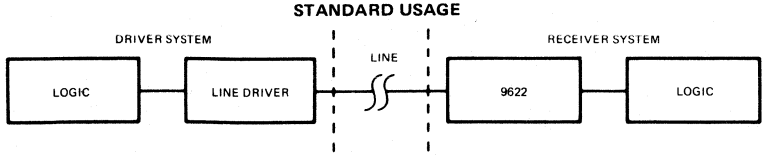
AC TEST CIRCUIT



WAVEFORMS



STANDARD USAGE



9624•9625
DUAL TTL, MOS INTERFACE ELEMENT
FAIRCHILD LINEAR INTEGRATED CIRCUIT

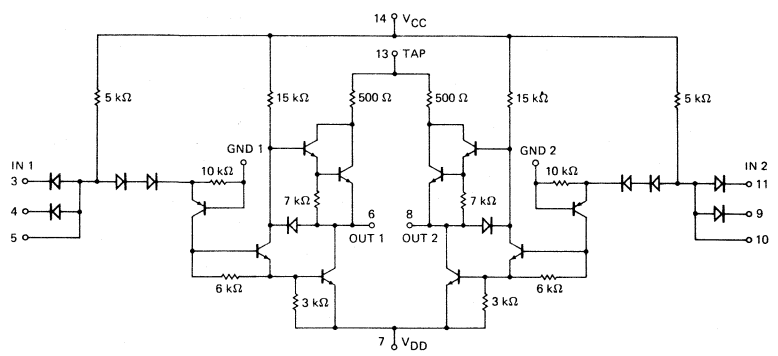
GENERAL DESCRIPTION – The 9624 is a Dual 2-Input TTL Compatible Interface Gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The 9625 is a dual MOS to TTL level converter. It is designed to convert standard negative MOS logic levels to TTL levels. The 9625 features a high input impedance which allows preservation of the driving MOS logic level.

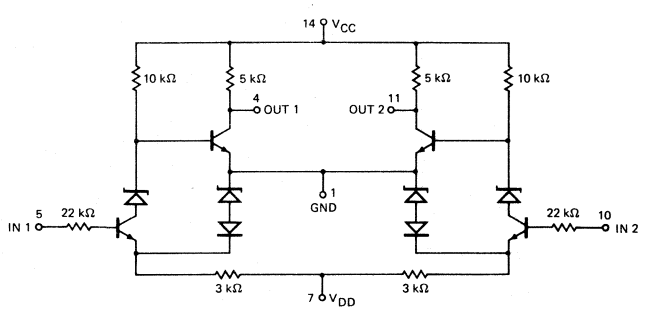
NOTE: The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the 9624 is represented as a NAND gate and the 9625 as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state "1" or TRUE), the 9624 acts as an AND gate and the 9625 as an inverter.

- **TTL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

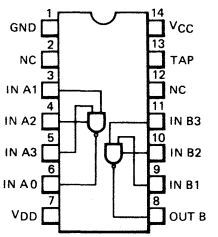
9624 EQUIVALENT CIRCUIT



9625 EQUIVALENT CIRCUIT



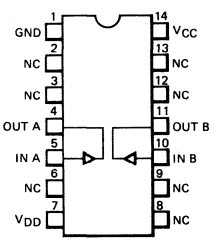
CONNECTION DIAGRAMS
9624
14-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
9624	9624DM
9624C	9624DC
9624	9624FM
9624C	9624PC

9625
14-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
9625	9625DM
9625C	9625DC
9625	9625FM
9625C	9625PC

11

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for HIGH Output State (9624)	V_{DD} to +V_{CC} value
Voltage Applied to Outputs for HIGH Output State (9625)	−0.5 V to V_{CC} value
Input Voltage (dc) (9624)	−0.5 V to +5.5 V
Input Voltage (dc) (9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (9624)	−30 V to +0.5 V
V_{TAP}	V_{CC} +0.5 V
Internal Power Dissipation (Note 3)	670 mW
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Operating Temperature Range	
Military (9624 and 9625)	−55°C to +125°C
Commercial (9624C and 9625C)	0°C to +70°C

9624

ELECTRICAL CHARACTERISTICS: (V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
V_{OH1}	Output HIGH Voltage	−1.0		−1.0	−0.5		−1.0		V	V_{CC} = 4.5 V, V_{DD} = −28 V, V_{TAP} = 0 V, I_{OH} = −10 μA
V_{OH2}	Output HIGH Voltage	+3.5		+3.5	+4.0		+3.5		V	V_{CC} = 5.5 V, V_{DD} = −20 V, V_{TAP} = 5.5 V, Inputs at V_{IL}, I_{OH} = −10 μA
V_{OL}	Output LOW Voltage (Note 1)								V	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{DD} = −15 to 28 V @ V_{IH}, 0 ≤ V_{TAP} ≤ V_{CC} (Note 2)
V_{IH}	Input HIGH Voltage	2.1		1.9			1.7		V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage		1.4			1.1		0.8	V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		−1.40			−1.25		−1.13	mA	V_{CC} = 5.5 V, V_F = 0.4 V, V_{DD} = −11 to −28 V
I_R	Input Leakage Current		2.0			2.0		5.0	μA	V_{CC} = 5.5 V, V_R = 4.0 V, V_{DD} = −11 to −28 V
I_{CEX}	Output Leakage Current					50			μA	V_{CC} = 5.5 V, V_{TAP} = 0 V, V_{DD} = −28 V, V_{OUT} = 0 V
I_{SC}	Output Short Circut Current	−12	−31	−14		−32	−11	−28	mA	V_{CC} = 4.5 V, V_{TAP} = 0 V, V_{IN} = 0 V, V_{DD} = −11 V, V_{OUT} = −11 V
I_{VCC}	V_{CC} Supply Current					6.1			mA	V_{CC} = 5.5 V, V_{DD} = −15 V, V_{TAP} = 0 V, Inputs Open
I_{MAX}	Max, Current					10			mA	V_{CC} = 10 V, V_{DD} = −30 V, V_{TAP} = 0 V, Inputs Open
t_{PLH}	Propagation Delay				190	250			ns	V_{CC} = 5.0 V, See Figure 1
t_{PHL}	Propagation Delay				50	100			ns	V_{DD} = −13 V, V_{TAP} = 0 V

9624C

ELECTRICAL CHARACTERISTICS: (V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		0°C		+25°C			+70°C			
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
V_{OH1}	Output HIGH Voltage	−1.0		−1.0	−0.5		−1.0		V	V_{CC} = 4.75 V, V_{DD} = −28 V, V_{TAP} = 0 V, I_{OH} = −10 μA
V_{OH2}	Output HIGH Voltage	+3.25		+3.25	+3.75		+3.25		V	V_{CC} = 5.25 V, V_{DD} = −20 V, V_{TAP} = 5.25 V, Inputs at V_{IL}, I_{OH} = −10 μA
V_{OL}	Output LOW Voltage (Note 1)								V	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{DD} = −11 to −28 V @ $0 \leq V_{TAP} \leq V_{CC}$ (Note 2)
V_{IH}	Input HIGH Voltage	2.0		1.9			1.8		V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage		1.2			1.1		0.95	V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		−1.32			−1.25		−1.20	mA	V_{CC} = 5.25 V, V_F = 0.45 V
I_R	Input Leakage Current		5.0			5.0		10	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = 5.25 V, V_{TAP} = 0 V, V_{DD} = −28 V, V_{OUT} = 0 V
I_{SC}	Output Short-Circut Current	−12	−31	−14		−32	−12	−31	mA	V_{CC} = 4.75 V, V_{TAP} = 0 V, V_{IN} = 0 V, V_{DD} = −11 V, V_{OUT} = −11 V
I_{VCC}	V_{CC} Supply Current					6.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{TAP} = 0 V, Inputs Open
I_{MAX}	Max, Current					10			mA	V_{CC} = 8.0 V, V_{DD} = −30 V, V_{TAP} = 0 V, Inputs Open
t_{PLH}	Propagation Delay				190	250			ns	V_{CC} = 5.0 V, See Figure 1
t_{PHL}	Propagation Delay				50	100			ns	V_{DD} = −13 V, V_{TAP} = 0 V

11

9625

ELECTRICAL CHARACTERISTICS: (V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	Output HIGH Voltage	2.5		2.6			2.5		V	V_{CC} = 4.5 V, I_{OH} = −60 μA, V_{DD} = −11 V, Inputs at V_{IH}
V_{OL}	Output LOW Voltage		0.5			0.5		0.5	V	V_{CC} = 5.5 V, I_{OL} = 1.5 mA V_{CC} = 4.5 V, I_{OL} = 1.2 mA V_{DD} = −11 V, Inputs at V_{IL}
V_{IH}	Input HIGH Voltage		−3.0			−3.0		−3.0	V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage	−9.0		−9.0			−9.0		V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		210			210		210	μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					50			μA	V_{CC} = V_{CEX} = 4.5 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8			mA	V_{CC} = 5.5 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1			mA	V_{CC} = 5.5 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0			mA	V_{CC} = 5.5 V, V_{DD} = −15 V, Input Open or GND
I_{MAX}	Max, V_{DD} Supply Current					−25			mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{PLH}	Propagation Delay				55	100			ns	V_{CC} = 5.0 V, V_{DD} = −13 V
t_{PHL}	Propagation Delay				90	150			ns	See Figure 2

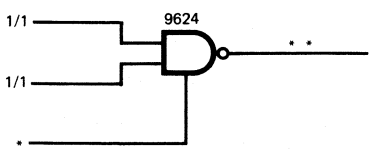
9625C

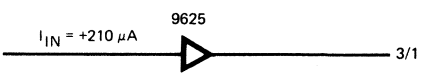
ELECTRICAL CHARACTERISTICS: (V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		0°C		+25°C			+70°C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	Output HIGH Voltage	2.5		2.6			2.5		V	V_{CC} = 4.75 V, I_{OH} = −60 μA, V_{DD} = −11 V, Inputs at V_{IH}
V_{OL}	Output LOW Voltage		0.5			0.5		0.5	V	V_{CC} = 5.25 V, I_{OL} = 1.52 mA V_{CC} = 4.75 V, I_{OL} = 1.33 mA Inputs at V_{IL}
V_{IH}	Input HIGH Voltage		−3.0			−3.0		−3.0	V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage	−9.0		−9.0			−9.0		V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		210			210		210	μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 4.75 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0			mA	V_{CC} = 5.5 V, V_{DD} = −15 V, Input Open or GND
I_{MAX}	Max, V_{DD} Supply Current					−25			mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{PLH}	Propagation Delay				55	100			ns	V_{CC} = 5.0 V, V_{DD} = −13 V
t_{PHL}	Propagation Delay				90	150			ns	See Figure 2

NOTES

1. Max = V_{DD} +1.0 V over Temperature Range. Typ = V_{DD} +0.2 V over Temperature Range.
2. At no time shall the voltage from V_{DD} to V_{TAP} exceed 30 V. See Absolute Maximum Ratings.
3. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For Flatpak derate linearly at 7.1 mW/°C above 60°C.



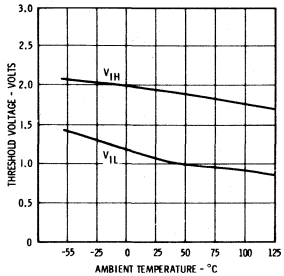


*The extender pin allows the number of inputs to be extended by adding diodes or the DTμL 933 extender.
**Fan out into MOS is limited only by MOS leakage currents.

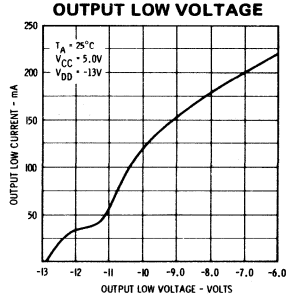
11

TYPICAL PERFORMANCE CURVES FOR 9624 AND 9624C

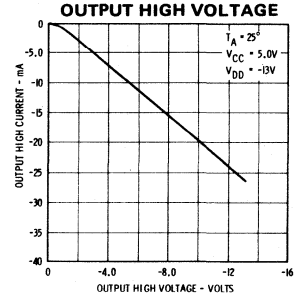
THRESHOLD VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



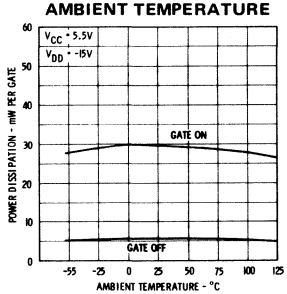
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



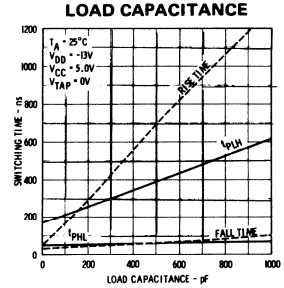
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



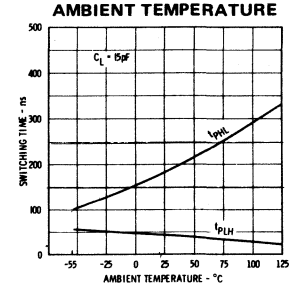
POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME AS A FUNCTION OF LOAD CAPACITANCE

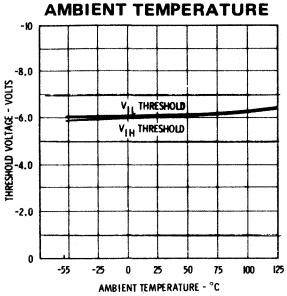


SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE

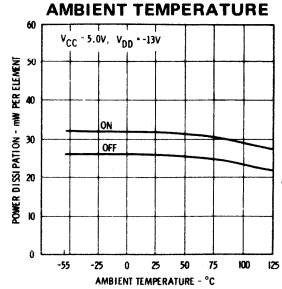


TYPICAL PERFORMANCE CURVES FOR 9625 AND 9625C

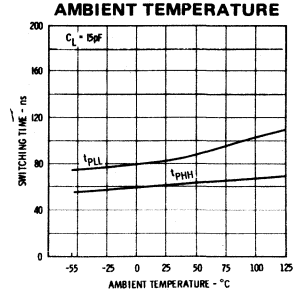
THRESHOLD VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



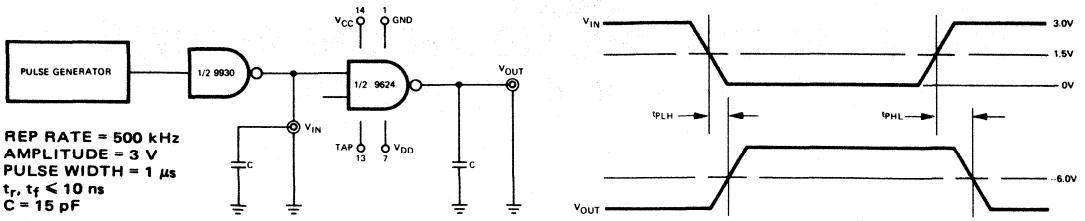
POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



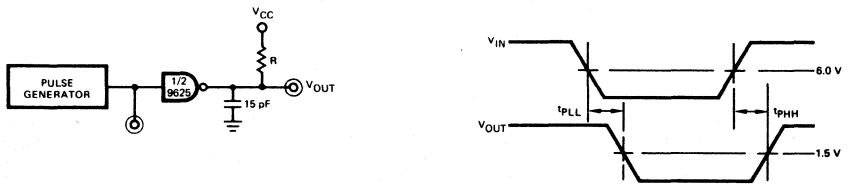
9624 AC TEST CIRCUIT AND WAVEFORMS



TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	Tap Voltage
t_{PLH}, t_{PHL}	25	5.0	−13	0

Fig. 1

9625 AC TEST CIRCUIT AND WAVEFORMS



Rep Rate = 500 kHz
Amplitude = −10 V
Pulse Width = 1.0 μs
t_r, t_f = 20 ns

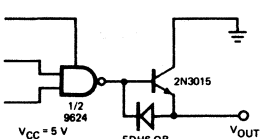
TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	R (kΩ)
t_{PLL}, t_{PHH}	25	5.0	−13	3.75

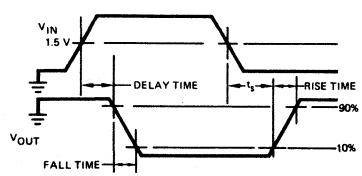
Fig. 2

APPLICATIONS

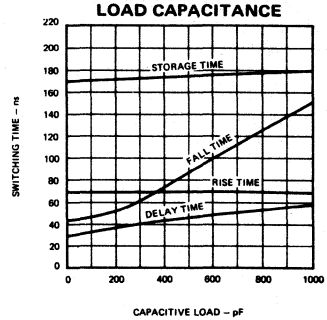
9624 Clock Driving

(using a high capacitance drive scheme)

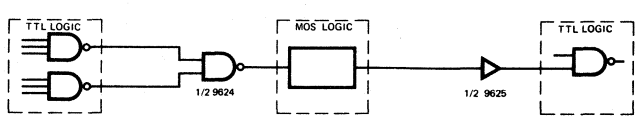




TYPICAL SWITCHING TIMES AS A FUNCTION OF LOAD CAPACITANCE



TYPICAL SYSTEM APPLICATION



9627
DUAL EIA RS-232-C/MIL-STD-188C LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9627 is a Dual Line Receiver which meets the electrical interface specifications of EIA RS-232-C and MIL-STD-188C. The input circuitry accomodates ±25V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The 9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V_{EE}, the switching points are at +2.6V and –2.6V, thus meeting RS-232-C requirements. When pin 1 is open, the switching points are at +0.45V and –0.45V, thus satisfying the requirements fo MIL-STD-188C LOW level interface. Connecting the R_{IN} pin to the (–) input yields an input impedance in the range of 3kΩ to 7kΩ and satisfies RS-232-C requirements; leaving R_{IN} unconnected, the input resistance will be greater than 6kΩ to satisfy MIL-STD-188C.

The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wire-AND function. A TTL/DTL strobe is also provided for each receiver. The EIA failsafe mode of operation is shown in the application section of this data sheet.

For the complementary function, see the 9616 triple EIA RS-232C/MIL-STD-188 line driver.

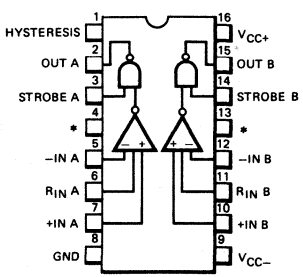
- **EIA RS-232-C INPUT STANDARDS**
- **MIL-STD-188C INPUT STANDARDS**
- **VARIABLE HYSTERESIS CONTROL**
- **HIGH COMMON MODE REJECTION**
- **R_{IN} CONTROL (5kΩ OR 10kΩ)**
- **WIRED-OR CAPABILITY**
- **CHOICE OF INVERTING AND NON-INVERTING INPUTS**
- **OUTPUTS AND STROBE TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

V_{CC+} to Ground	0V to +15V
V_{CC-} to Ground	0V to –15V
Input Voltage Referred to Ground Pin	±25V
Strobe to Ground Voltage	–0.5V to +5.5V
Maximum Applied Output Voltage	–0.5V to +15V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	
Military (9627)	–55°C to +125°C
Commercial (9627C)	0°C to +70°C
Internal Power Dissipation (Note 1)	730mW
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

NOTE:
1. For Hermetic DIP and Molded DIP rating applies to ambient temperatures up to 65°C, above 65°C derate linearly at 8.3 mW/°C. For the Flatpack, derate linearly at 7.1 mW/°C above 45°C.

CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F

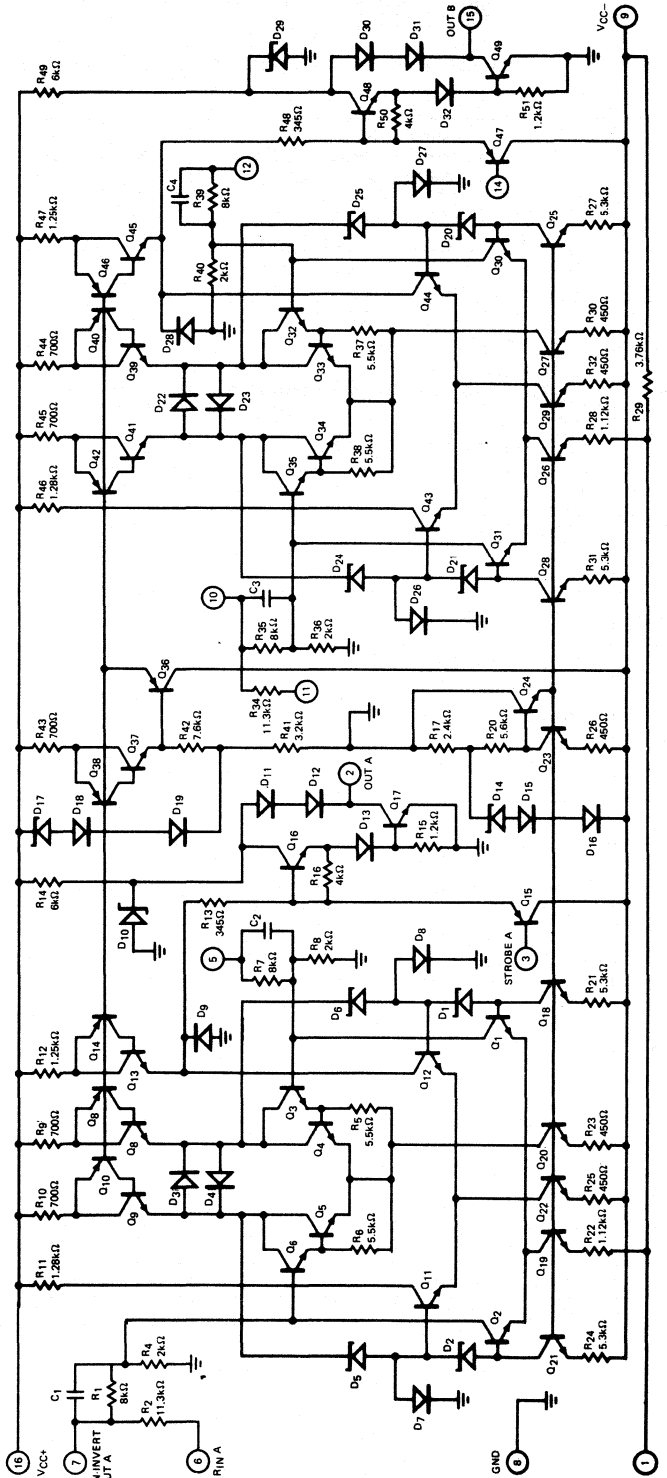


*Internal Connection – make no connection to this pin.

ORDER INFORMATION

TYPE	PART NO.
9627	9627DM
9627	9627FM
9627C	9627DC
9627C	9627PC

EQUIVALENT CIRCUIT



$C_1 = C_2 = C_3 = C_4 = 1.1$ pF

Pin 4 and 13 = Internal Connection.

11

9627 • 9627C

ELECTRICAL CHARACTERISTICS (V_{CC+} = 12 V ±10%, V_{CC-} = −12 V ±10% over Operating Temperature Range, unless otherwise specified)

MIL-STD-188C

SYMBOL	PARAMETER	CONDITIONS (Pins 6 and 11 Open. Inverting Inputs Open. Pin 1 Open).	MIN	TYP	MAX	UNITS
V_{OL}	Output LOW Voltage	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V Non-Inverting Input = −0.6 V, I_{OL} = 6.4 mA			0.4	V
V_{OH}	Output HIGH Voltage	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V Non-Inverting Input = +0.6 V, I_{OH} = −0.5 mA	2.4			V
I_{SC}	Output Shorted Current	V_{CC+} = +13.2 V, V_{CC-} = −10.8 V Non-Inverting Input = +0.6 V Outputs Grounded			3.0	mA
I_{IH} (Strobe)	Input HIGH Current (Strobe)	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V, V_S = 2.4 V			40	µA
		Non-Inverting Input = +0.6 V, V_S = 5.5 V			1.0	mA
R_{IN}	Input Resistance	V_{CC+} = +13.2 V, V_{CC-} = −13.2 V Non-Inverting Input = +3.0 V or −3.0 V	6.0			kΩ
I_{TH+}	Positive Threshold Current	V_{OUT} = 2.4 V			100	µA
I_{TH-}	Negative Threshold Current	V_{OUT} = 0.4 V	−100			µA
	I_{TH+} and I_{TH-} Magnitude Matching Error			±10		%
V_{IL} (Strobe)	Input LOW Voltage (Strobe)	$V_{Non\text{-}Inverting\ Input}$ = −0.6 V			0.8	V
V_{IH} (Strobe)	Input HIGH Voltage (Strobe)	$V_{Non\text{-}Inverting\ Input}$ = +0.6 V V_{CC+} = +13.2 V, V_{CC-} = −10.8 V	2.0			V
I_+	Positive Supply Current	$V_{Non\text{-}Inverting\ Input}$ = −0.6 V			18	mA
		T_A = +125°C (9627)			12.4	
I_-	Negative Supply Current	$V_{Non\text{-}Inverting\ Input}$ = +0.6 V	−16			mA
		T_A = +125°C (9627)	−11.4			

RS-232C

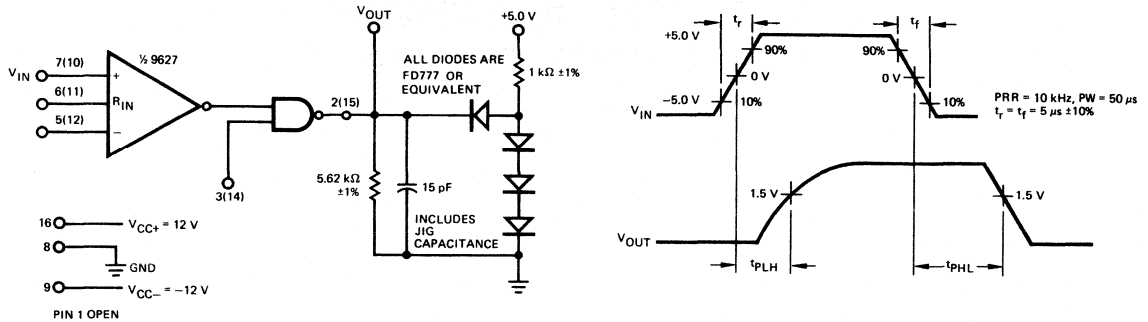
SYMBOL	PARAMETER	CONDITIONS (Non-Inverting Inputs Connected to Ground, R_{IN} Inputs Connected to Inverting Inputs)	MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	V_{IN} = +3.0 V to +25 V	3.0		7.0	kΩ
		V_{IN} = −3.0 V to −25 V	3.0		7.0	kΩ
V_{IN}	Input Voltage	Open Circuit	−2.0		2.0	V
V_{TH+}	Positive Threshold Voltage				0.6	V
V_{TH-}	Negative Threshold Voltage		−0.6			V

AC CHARACTERISTICS (T_A = +25°C, V_{CC+} = +12 V, V_{CC-} = −12 V)

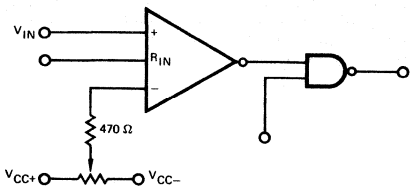
MIL-STD-188C • RS-232-C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time	See AC Test Circuit, R_L = 3.9 kΩ		60	250	ns
t_{PHL}	Propagation Delay Time	See AC Test Circuit, R_L = 390 Ω		84	250	ns

AC TEST CIRCUIT AND WAVEFORMS

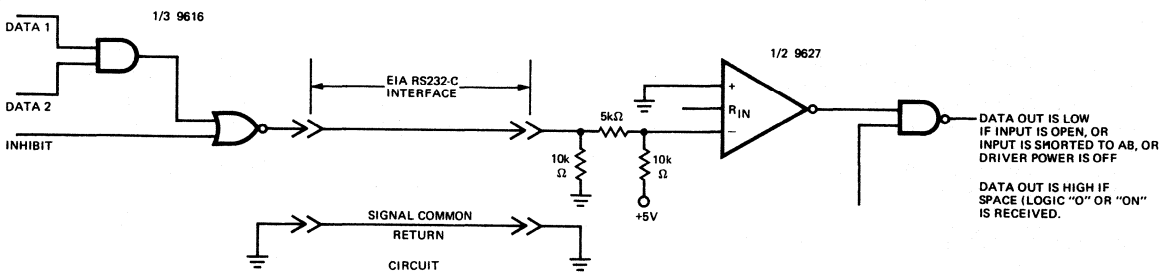


THRESHOLD CURRENT MATCHING CIRCUIT

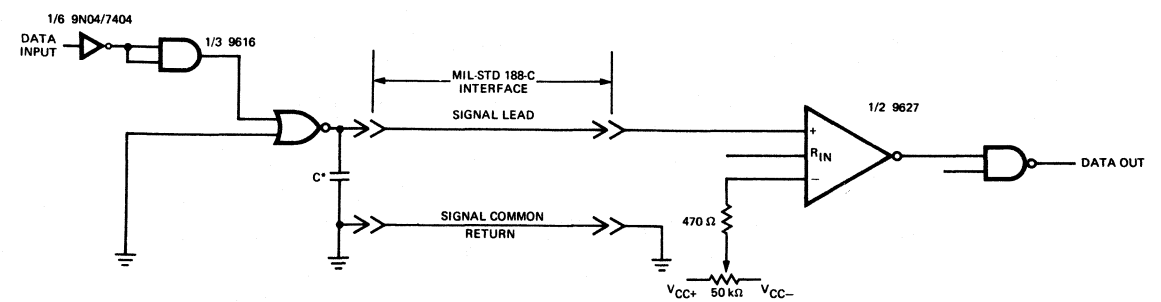


ADJUST POT TO ACHIEVE POSITIVE THRESHOLD CURRENT AND NEGATIVE THRESHOLD CURRENT MATCHING

EIA RS-232-C INTERFACE WITH FAILSAFE RECEIVER (PIN 1 OPEN)



MIL-STD-188C INTERFACE (PIN 1 OPEN)



* Capacitor for Transmitter Waveshaping at Applicable Modulation Rate.

9664 • 9664A

MOS TO LED DIGIT DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

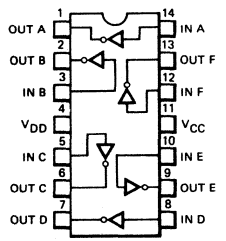
GENERAL DESCRIPTION — The 9664/9664A HEX LED/LAMP Drivers convert MOS signals to high output currents for LED display digit select, lamp select or other applications where high output drive current is important. Six drivers convert MOS signals to high output currents in time multiplex systems using the segment address or the digit scan method of driving LED displays. This results in reduced board space and system cost in multidigit displays. The 9664A is selected for 20 V operation for those applications where higher breakdown voltage is required.

- **150 mA SINK CAPABILITY**
- **MOS COMPATIBLE INPUTS**
- **VERY LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**
- **10 V AND 20 V OPERATION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) 9664	10 V
9664A	20 V
Input Voltage (Note 3)	−5.0 V to V_{CC}
Collector Voltage (Note 2) 9664	10 V
9664A	20 V
Collector to Input Voltage 9664	10 V
9664A	20 V
Continuous Collector Current — Each Collector	150 mA
Continuous V_{DD} Current — Sum of all Collector Currents	600 mA
Continuous Total Power Dissipation (Note 4)	800 mW
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

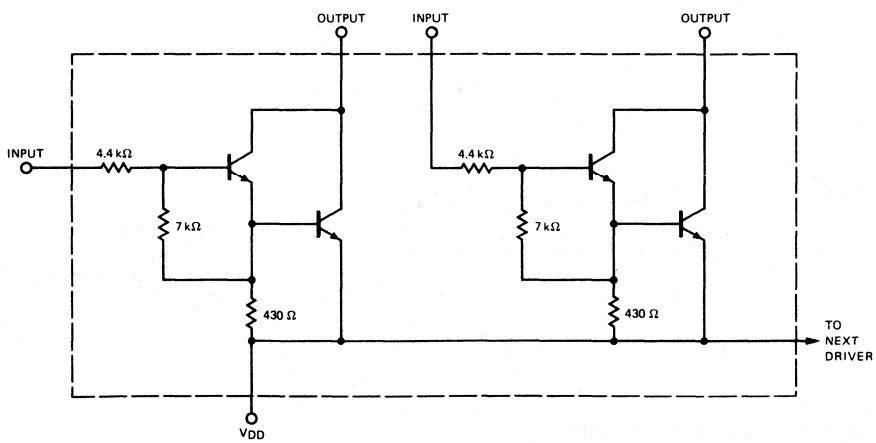
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
9664	9664DC
9664	9664PC
9664A	9664ADC
9664A	9664APC

EQUIVALENT CIRCUIT (1/3 of 9664/9664A)



ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V for 9664; V_{CC} = 20 V for 9664A; T_A = 0°C to 70°C unless otherwise specified)

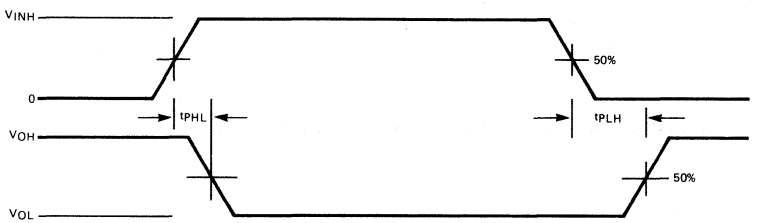
SYMBOL	PARAMETER	CONDITION		MIN	TYP *	MAX	UNITS
V_{OL}	Output Low Voltage	V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 150 mA, T_A = 25°C			0.9	1.2	V
		V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 150 mA			0.9	1.5	V
I_{OH}	Output High Current	I_{IN} = 40 μA	9664, V_{OH} = 10 V			200	μA
			9664A, V_{OH} = 20 V				
		V_{IN} = 0.5 V	9664, V_{OH} = 10 V			200	μA
			9664A, V_{OH} = 20 V				
I_I	Input Current at Maximum Input Voltage	I_{OL} = 20 mA	9664, V_{IN} = 10 V			3.3	mA
			9664A, V_{IN} = 20 V			6.6	mA
I_{SS}	Supply Current					200	μA
AC CHARACTERISTICS (V_{CC} = 7.5 V, T_A = 25°C)							
t_{PHL}	Propagation Delay Time	R_L = 39 Ω, V_{INH} = 7.5 V C_L = 15 pF			30		ns
t_{PLH}					300		ns

NOTES

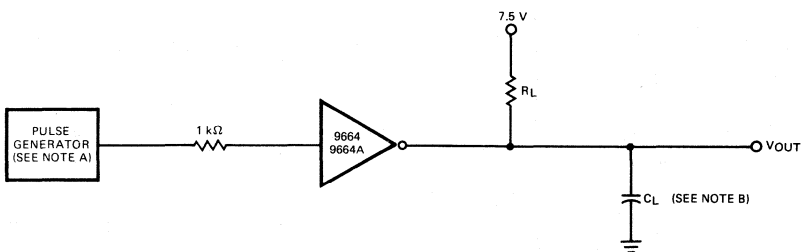
1. V_{CC} terminal voltage is with respect to any other device terminal.
2. Voltage values are with respect to V_{DD} terminal unless otherwise noted.
3. With the exception of the inputs, the V_{DD} terminal must always be the most negative device voltage for proper operation.
4. Above 60°C ambient temperature derate linearly at 8.3 mW/°C.

* All typical values are at T_A = 25°C.

SWITCHING WAVEFORMS



TEST CIRCUIT

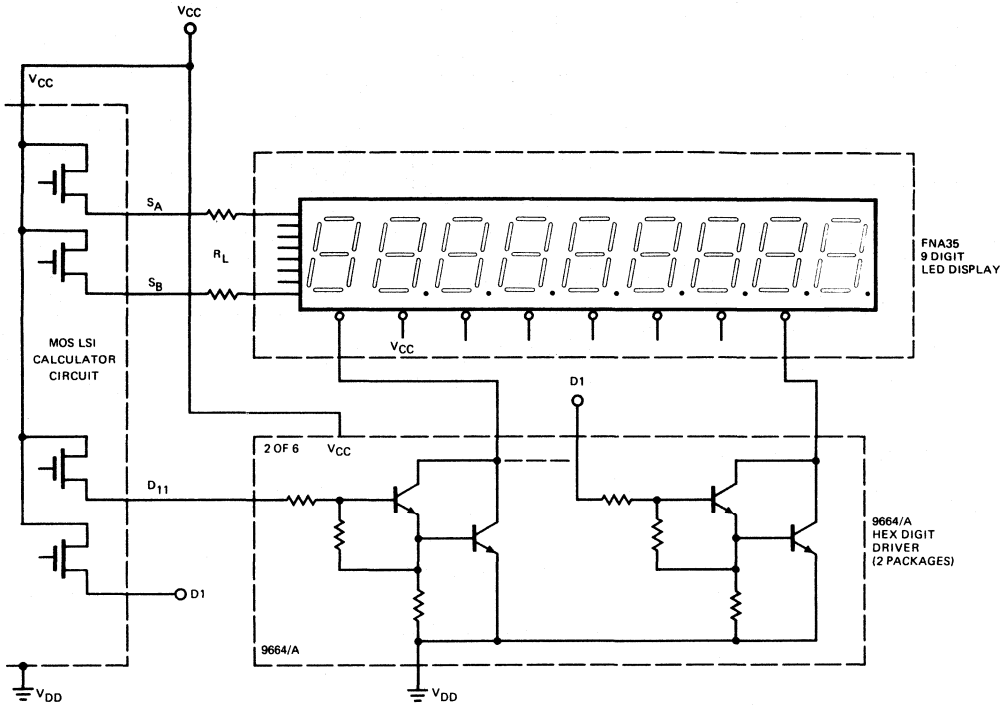


NOTES:

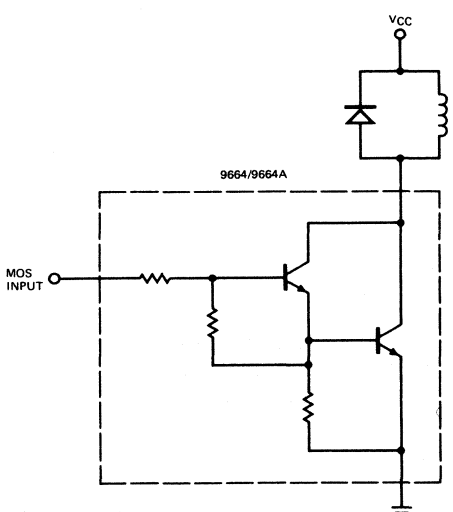
A. The pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.
B. C_L includes probe and jig capacitance switching.

11

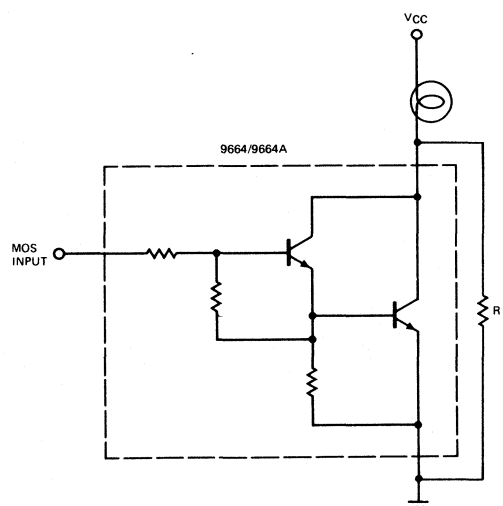
TYPICAL APPLICATION



INTERFACING BETWEEN MOS CALCULATOR CIRCUIT AND LED MULTI-DIGIT DISPLAY



MOS RELAY DRIVER



NOTE:
Bleeder resistor (R) reduces the surge current through the lamp when the filament is cold.

MOS LAMP DRIVER

5520/7520 SERIES

CORE MEMORY SENSE AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 5520/7520 Series Dual Memory Sense Amplifiers are designed for use in high speed core memory systems. These sense amplifiers detect the mV memory signals and transform them into logic levels compatible with TTL and DTL circuits. Independent strobes for each channel provide the capability for performing time discrimination, resulting in the detection of the input signal when the signal to noise ratio is at maximum. A common reference amplifier simultaneously sets the threshold of each sense amplifier, and the reference amplifier and sense amplifier are compensated to reduce the effect of power supply voltage or temperature variation. All gate inputs are compatible with TTL and DTL circuits.

- **HIGH SPEED AND FAST RECOVERY TIME**
- **NARROW THRESHOLD UNCERTAINTY REGION**
- **ADJUSTABLE INPUT THRESHOLD VOLTAGE**
- **TTL COMPATIBLE**
- **VARIOUS LOGIC CONFIGURATIONS**

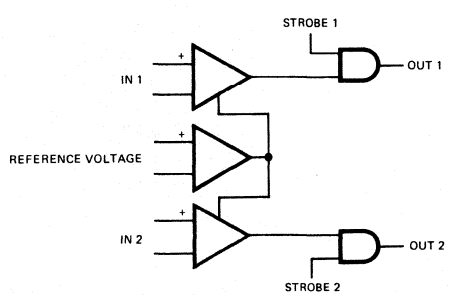
COMPARISON CHART

The 7520 series of sense amplifiers provides a wide number of options which allow this device to be adapted to a variety of special applications. Differences between the various sense amplifier devices are summarized in the table below. 55XX numbers refer to military grade devices, while the corresponding 75XX number refers to the identical circuit specified for commercial grade. Even numbered devices refer to sense amplifiers specified for a tight threshold voltage distribution.

DEVICE	DECOUPLING CAPACITOR	OUTPUT STAGE	AMPLIFIER TEST POINTS
5524/7524/5525/7525	External		
5528/7528/5529/7529	External		Yes
5534/7534/5535/7535	External	Inverted with Open Collector	
5538/7538/5539/7539	External	Inverted with Open Collector	Yes
55224/75224/55225/75225	Internal		
55232/75232/55233/75233	Internal	Inverted with Open Collector	
55234/75234/55235/75235	Internal	Inverted	
55238/75238/55239/75239	Internal	Inverted	Yes

11

FUNCTIONAL BLOCK DIAGRAM



5520/7520 SERIES ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7.0 V
Differential Input Voltage	±5.0 V
Logic Input Voltage	±5.5 V
Strobe and Gate Input Voltage	+5.0 V
Off State Output Voltage	+5.5 V
Operating Ambient Temperature Range	
5520 Series	−55°C to +125°C
7520 Series	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	+300°C
Molded DIP (Soldering, 10 s)	+260°C
Internal Power Dissipation (Note 1)	730 mW

5520/7520 SERIES RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
V_{CC+}	4.75	5.0	5.25	V
V_{CC-}	−4.75	−5.0	−5.25	V
V_{REF}	15		40	mV

ELECTRICAL CHARACTERISTICS

All electrical characteristics and test conditions for the 5520 devices are identical to those of the corresponding 7520 device, with the exception of the Differential Input Threshold Voltage and Differential Input Bias Circuit. Limits for these parameters are detailed in the table below. All limits which apply to the 7520 circuits for temperatures of 0° C to 70° C apply to the 5520 circuits for the range of −55° C to +125° C.

All ac switching characteristics are guaranteed at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V and T_A = 25° C.

For details of the full electrical characteristics and test circuitry please refer to the corresponding 7520 data.

5520 SERIES V_{TH} AND I_{IB} LIMITS

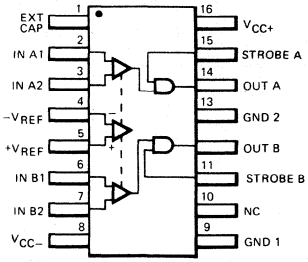
SYMBOL	PARAMETER	TEST CONDITIONS		EVEN NUMBERED 5520 SERIES DEVICES			ODD NUMBERED 5520 SERIES DEVICES			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Differential Input Threshold Voltage (Note 2)	V_{ref} = 15 mV	T_A = −55° C to 0° C and 70° C to 125° C	10	15	20	8.0	15	22	mV
			T_A = 0° C to 70° C	11	15	19	8.0	15	22	
		V_{ref} = 40 mV	T_A = −55° C to 0° C and 70° C to 125° C	35	40	45	33	40	47	
			T_A = 0° C to 70° C	36	40	44	33	40	47	
I_{IB}	Differential Input Bias Current	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55° C to 0° C			100			100	μA
			T_A = 0° C to 125° C		30	75		30	75	

NOTES:

1. Derate Hermetic DIP and Molded DIP above 60° C at 8.3 mW/° C. Derate Flatpak above 50° C at 7.1 mW/° C.
2. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic-gate threshold voltage level.

7524/7525
SENSE AMPLIFIERS

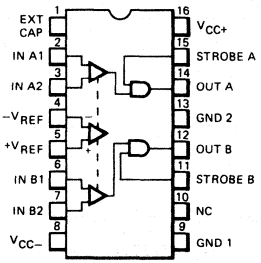
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
5524	5524FM
5525	5525FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
5524	5524DM
5525	5525FM
7524	7524DC
7525	7525DC
7524	7524PC
7525	7525PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	H
L	X	L
X	L	L

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	7524	11	15	19	mV
				7525	8.0	15	22	
			V_{ref} = 40 mV	7524	36	40	44	
				7525	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
V_{OH}	Output HIGH Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4.0		V
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

7524/7525
SENSE AMPLIFIERS

AC CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, $C_{ext} \geq 100$ pF, T_A = 25°C

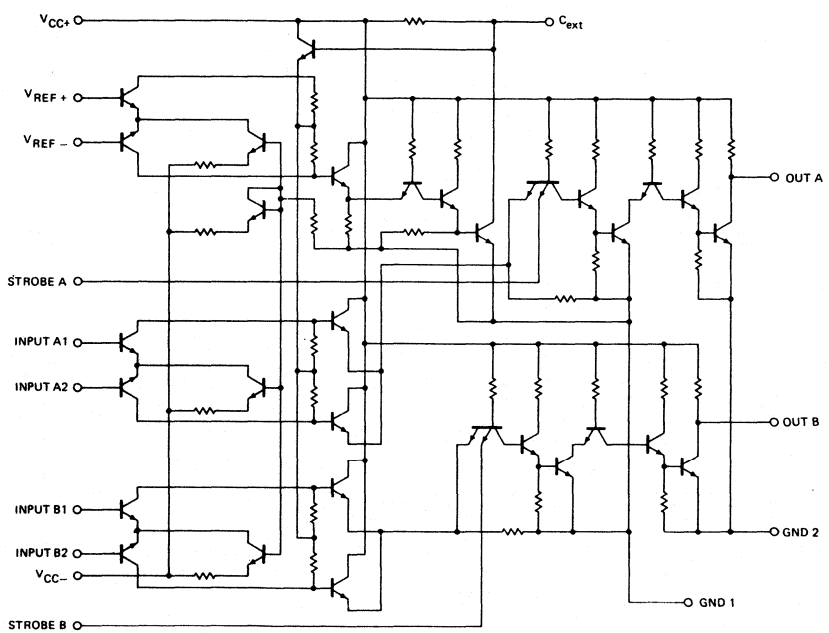
PROPAGATION DELAY TIMES			TEST					
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	A1-A2	A	7	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PHL(D)}$	STROBE	A	7	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, $C_{ext} \geq 100$ pF, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: V_{ID} = 2.0 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: V_{IC} = ±2.0 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

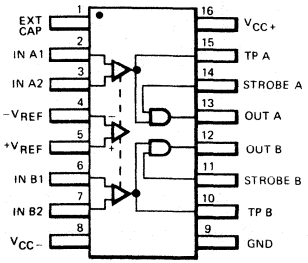
NOTES:
5. Differentail input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe-enable signal.

EQUIVALENT CIRCUIT



7528/7529
SENSE AMPLIFIERS

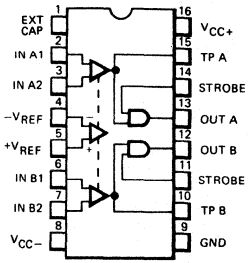
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
5528	5528FM
5529	5529FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
5528	5528DM
5529	5529DM
7528	7528DC
7529	7529DC
7528	7528PC
7529	7529PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	H
L	X	L
X	L	L

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	7528	11	15	19	mV
				7529	8.0	15	22	
			V_{ref} = 40 mV	7528	36	40	44	
				7529	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
V_{OH}	Output HIGH Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4.0		V
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

7528/7529
SENSE AMPLIFIERS

AC CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

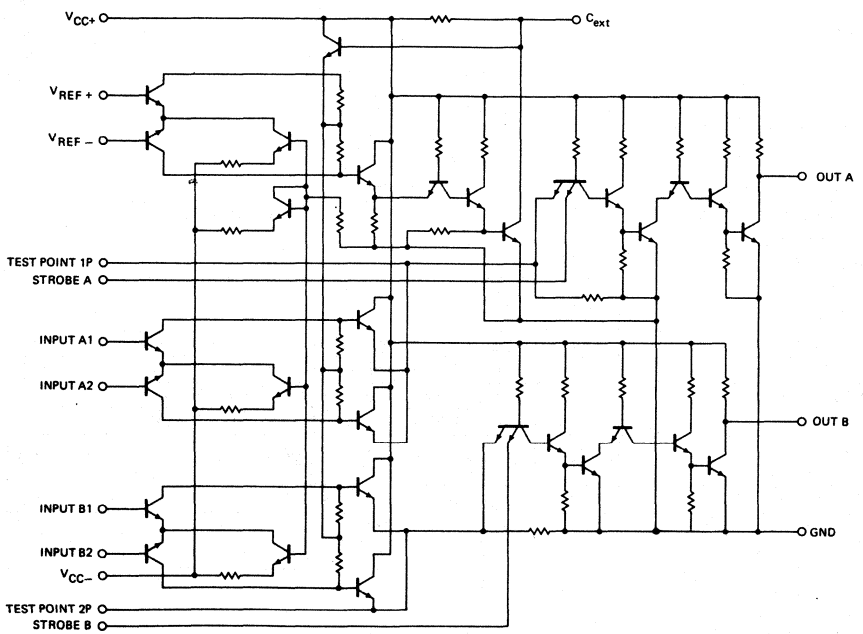
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1-A2	A	8	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PHL(D)}$	STROBE	A	8	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: V_{ID} = 2.0 V, t_f = 20 ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: V_{IC} = ±2.0 V, t_r = t_f = 20 ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

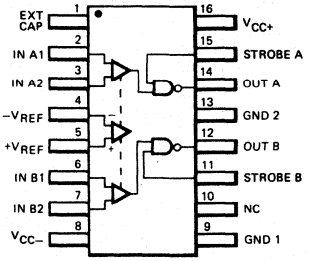
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

EQUIVALENT CIRCUIT



7534/7535
SENSE AMPLIFIERS

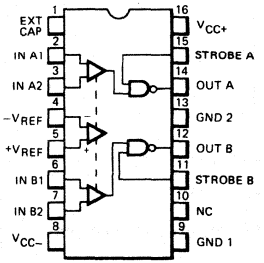
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
5534	5534FM
5535	5535FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
5534	5534DM
5534	5535DM
7534	7534DC
7535	7535DC
7534	7534PC
7535	7535PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	7534	11	15	19	mV
				7535	8.0	15	22	
			V_{ref} = 40 mV	7534	36	40	44	
				7535	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_W = 50 ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
I_{OH}	Output HIGH Current	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{OH} = 5.25 V				250	μA
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			28	38	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−13	−18	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

7534/7535
SENSE AMPLIFIERS

AC CHARACTERISTICS: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

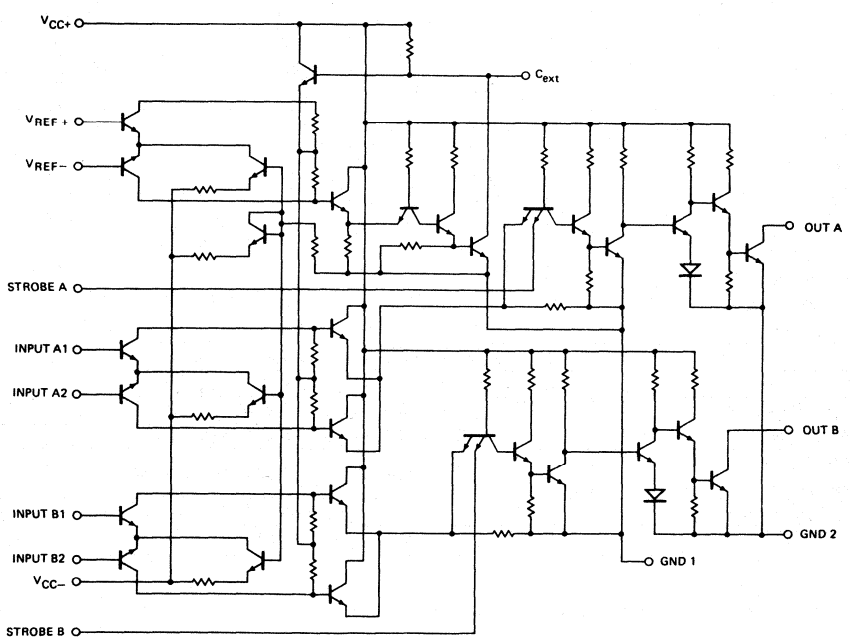
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1-A2	A	7	$C_L = 15$ pF, $R_L = 230\ \Omega$		25		ns
$t_{PHL(D)}$						25	40	
$t_{PHL(D)}$	STROBE	A	7	$C_L = 15$ pF, $R_L = 230\ \Omega$		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: $V_{ID} = 2.0$ V, $t_r = t_f = 20$ ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: $V_{IC} = \pm 2.0$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

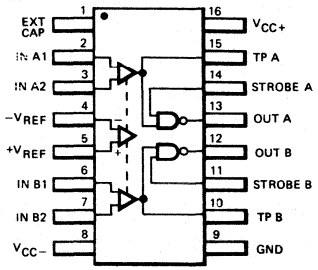
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

EQUIVALENT CIRCUIT



7538/7539
SENSE AMPLIFIERS

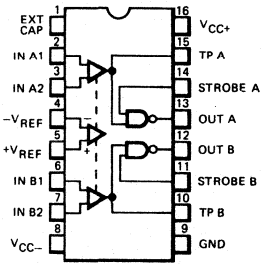
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
5538	5538FM
5539	5539FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
5538	5538DM
5539	5539DM
7538	7538DC
7539	7539DC
7538	7538PC
7539	7539PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	7538	11	15	19	mV
				7539	8.0	15	22	
			V_{ref} = 40 mV	7538	36	40	44	
				7539	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
I_{OH}	Output HIGH Current	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{OH} = 5.25 V				250	μA
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

7538/7539
SENSE AMPLIFIERS

AC CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

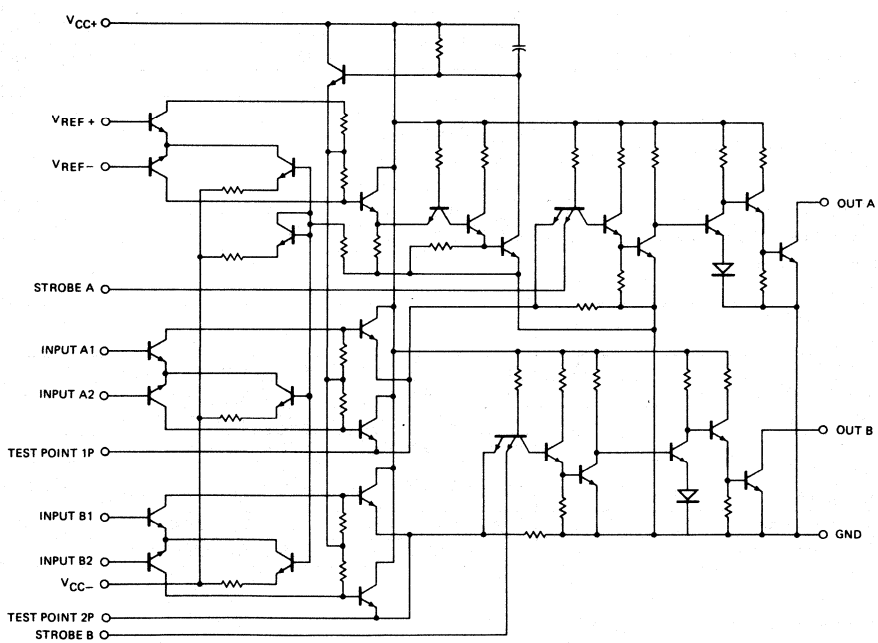
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1-A2	A	8	C_L = 15 pF, R_L = 230 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PHL(D)}$	STROBE	A	8	C_L = 15 pF, R_L = 230 Ω		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: V_{ID} = 2.0 V, t_f = 20 ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: V_{IC} = ±2.0 V, t_r = t_f = 20 ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

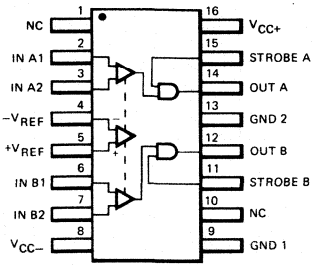
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

EQUIVALENT CIRCUIT



75224/75225
SENSE AMPLIFIERS

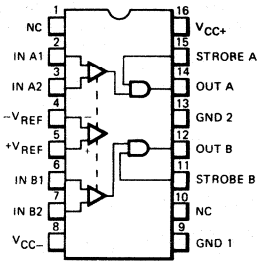
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
55224	55224FM
55225	55225FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
55224	55224DM
55225	55225DM
75224	75224DC
75225	75225DC
75224	75224PC
75225	75225PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	H
L	X	L
X	L	L

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I > V_{IH(MIN)}$	$V_I < V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	75224	11	15	19	mV
				75225	8.0	15	22	
			V_{ref} = 40 mV	75224	36	40	44	
				75225	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
V_{OH}	Output HIGH Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4.0		V
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

75224/75225
SENSE AMPLIFIERS

AC CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, $C_{ext} \geq 100$ pF, T_A = 25°C

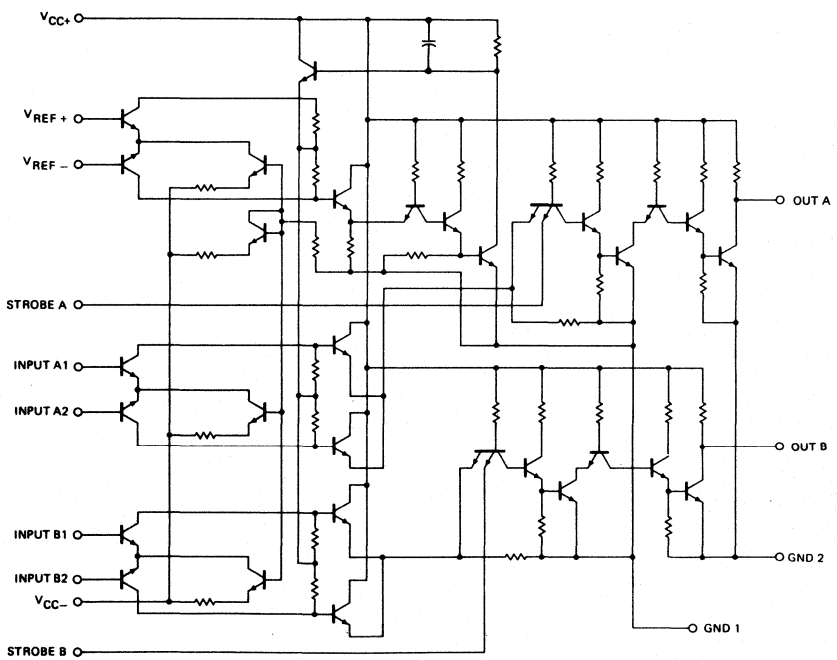
PROPAGATION DELAY TIMES			TEST					
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	A1-A2	A	7	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PHL(D)}$	STROBE	A	7	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, $C_{ext} \geq 100$ pF, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: V_{ID} = 2.0 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: V_{IC} = ±2.0 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

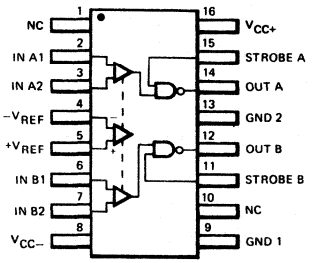
NOTES:
5. Differentail input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

EQUIVALENT CIRCUIT



75232/75233
SENSE AMPLIFIERS

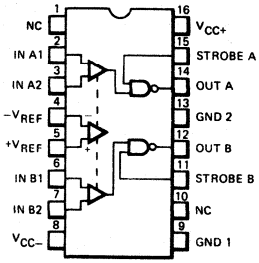
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
55232	55232FM
55233	55233FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
55232	55232DM
55233	55233DM
75232	75232DC
75233	75233DC
75232	75232PC
75233	75233PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	75232	11	15	19	mV
				75233	8.0	15	22	
			V_{ref} = 40 mV	75232	36	40	44	
				75233	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_w = 50$ ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
I_{OH}	Output HIGH Current	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{OH} = 5.25 V				250	μA
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

75232/75233
SENSE AMPLIFIERS

AC CHARACTERISTICS: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

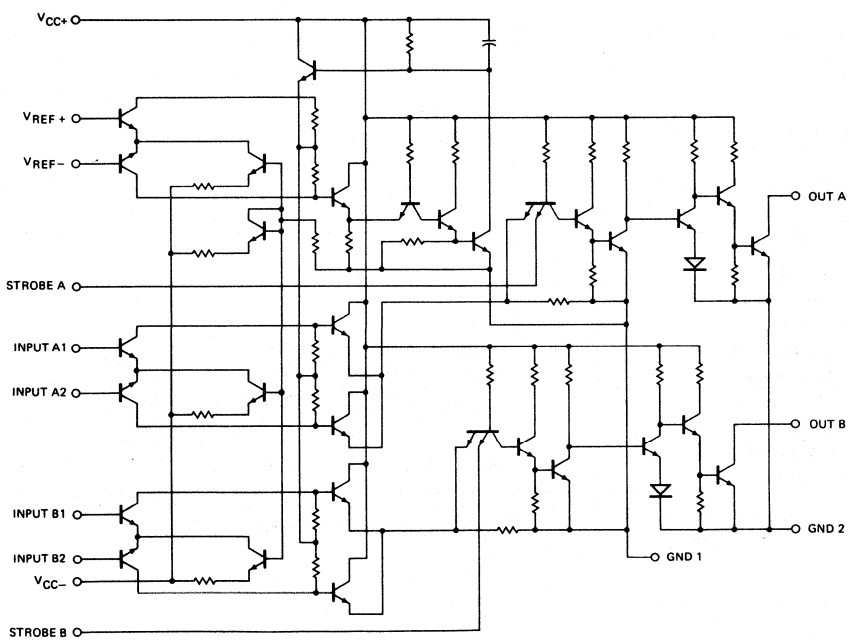
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1-A2	A	7	$C_L = 15$ pF, $R_L = 230\ \Omega$		25		ns
$t_{PHL(D)}$						25	40	
$t_{PHL(D)}$	STROBE	A	7	$C_L = 15$ pF, $R_L = 230\ \Omega$		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: $V_{ID} = 2.0$ V, $t_r = t_f = 20$ ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: $V_{IC} = \pm 2.0$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

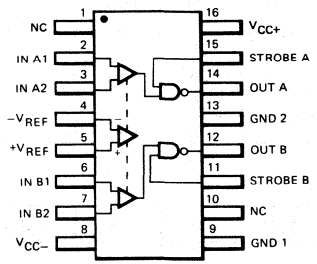
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

EQUIVALENT CIRCUIT



75234/75235
SENSE AMPLIFIERS

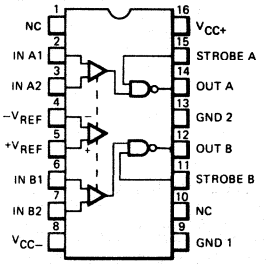
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
55234	55234FM
55235	55235FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
55234	55234DM
55235	55235DM
75234	75234DC
75235	75235DC
75234	75234PC
75235	75235PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	75234	11	15	19	mV
				75235	8.0	15	22	
			V_{ref} = 40 mV	75234	36	40	44	
				75235	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
V_{OH}	Output HIGH Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4.0		V
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

75234/75235
SENSE AMPLIFIERS

AC CHARACTERISTICS: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

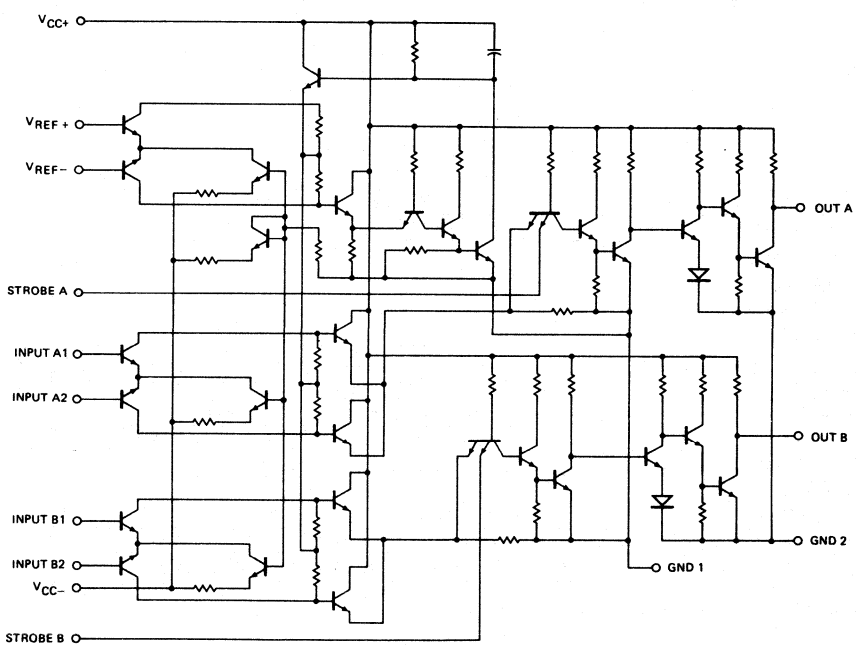
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1-A2	A	7	$C_L = 15$ pF, $R_L = 288\ \Omega$		25		ns
$t_{PHL(D)}$						25	40	
$t_{PHL(D)}$	STROBE	A	7	$C_L = 15$ pF, $R_L = 288\ \Omega$		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: $V_{ID} = 2.0$ V, $t_r = t_f = 20$ ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: $V_{IC} = \pm 2.0$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

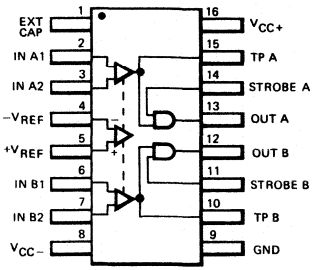
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

EQUIVALENT CIRCUIT



75238/75239
SENSE AMPLIFIERS

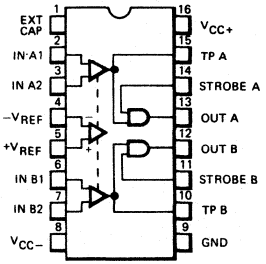
CONNECTION DIAGRAM
16-LEAD FLATPAK
PACKAGE OUTLINE 4L
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
55238	55238FM
55239	55239FM

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
55238	55238DM
55239	55239DM
75238	75238DC
75239	75239DC
75238	75238PC
75239	75239PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{ref} = 15 mV	75238	11	15	19	mV
				75239	8.0	15	22	
			V_{ref} = 40 mV	75238	36	40	44	
				75239	33	40	47	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_W = 50 ns			±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0			0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3			2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3					0.8	V
V_{OH}	Output HIGH Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA		2.4	4.0		V
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA			0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V			−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V		−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C			−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

75238/75239
SENSE AMPLIFIERS

AC CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

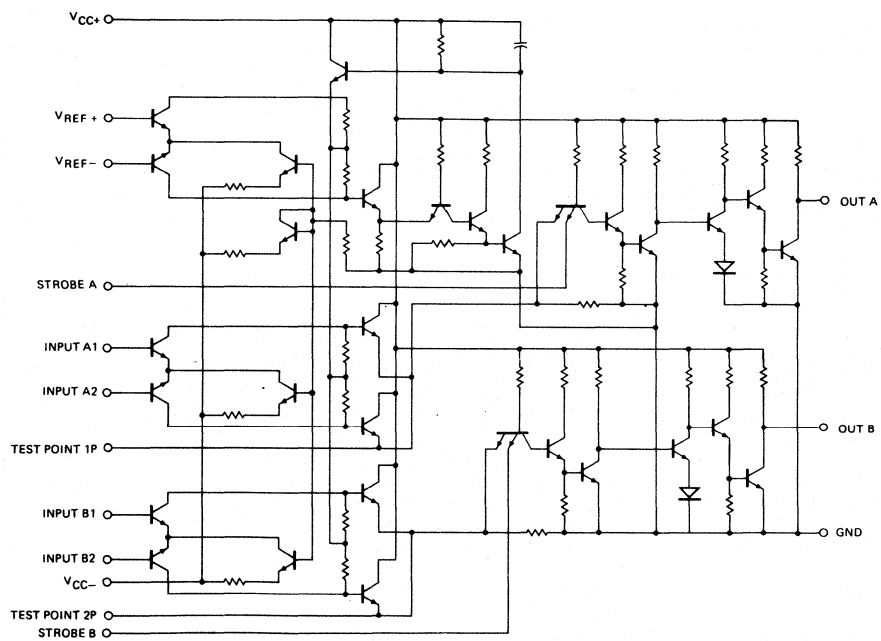
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1-A2	A	8	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PHL(D)}$	STROBE	A	8	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: V_{ID} = 2.0 V, t_f = 20 ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: V_{IC} = ±2.0 V, t_r = t_f = 20 ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

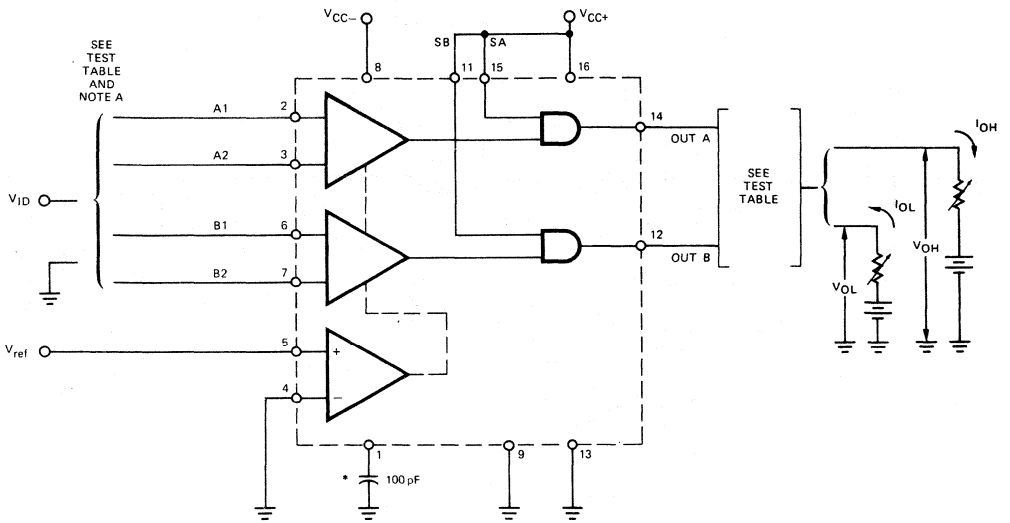
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

EQUIVALENT CIRCUIT



DC TEST CIRCUITS

7524/25, 75224/225



*Required for 7524/25

11

TEST TABLE

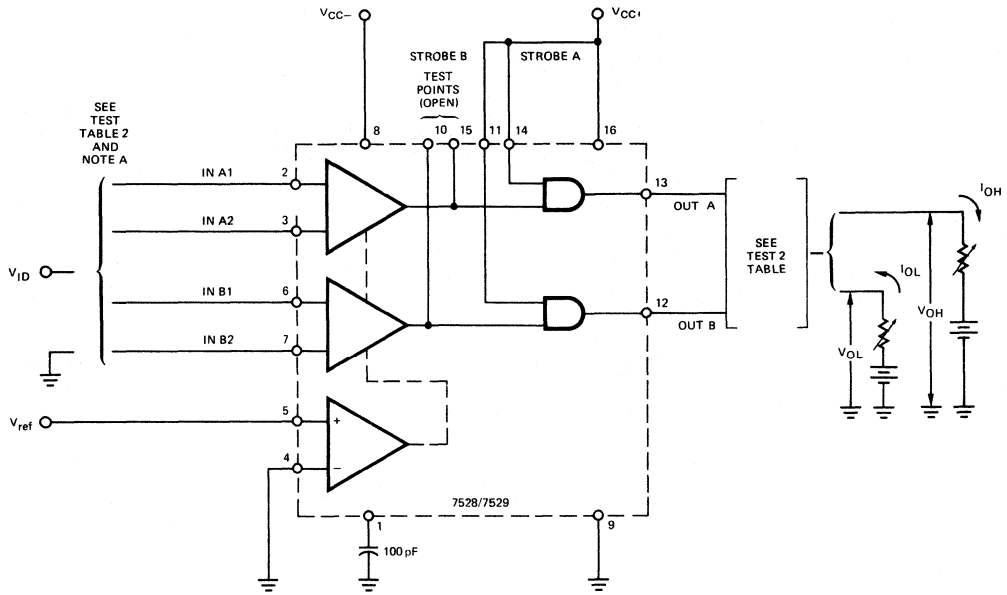
CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS		
				V_O	I_{OH}	I_{OL}
7524, 75224	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
7525, 75225	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output. Each pair of differential inputs is tested separately with the other pair grounded.

Fig. 1a – V_T

DC TEST CIRCUITS (Cont'd)

7528/28



TEST TABLE 2

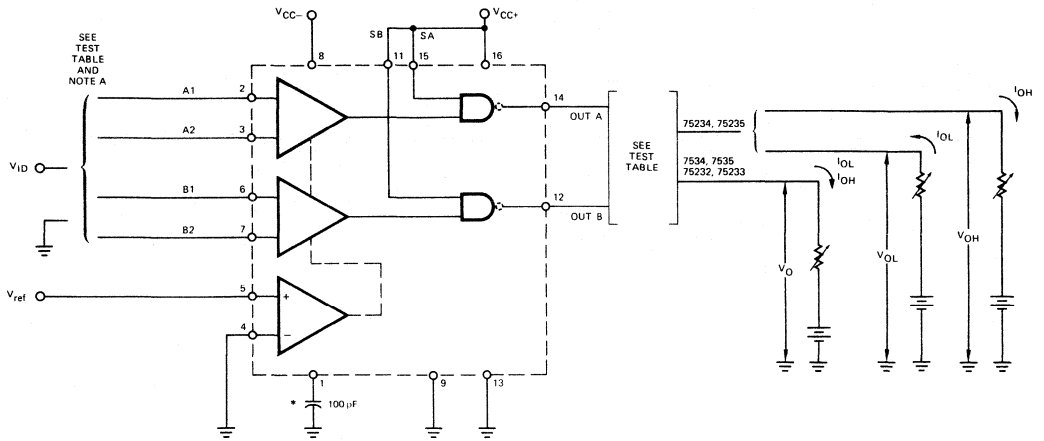
CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS		
				V_O	I_{OH}	I_{OL}
7528	A1-A2 AND B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA
		15 mV	≥19 mV	≥2.4 V	−400 μA	
		40 mV	≤36 mV	≤0.4 V		16 mA
		40 mV	≥44 mV	≥2.4 V	−400 μA	
7529	A1-A2 AND B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mV
		15 mV	≥22 mV	≥2.4 V	−400 μA	
		40 mV	≤33 mV	≤0.4 V		16 mA
		40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.
Each pair of differential inputs is tested separately with the other pair grounded.

Fig. 1b – V_T

DC TEST CIRCUITS (Cont'd)

7534/35, 75232/233, 75234/235
PARAMETER MEASUREMENT INFORMATION



*Required for 7534/7535

TEST TABLE

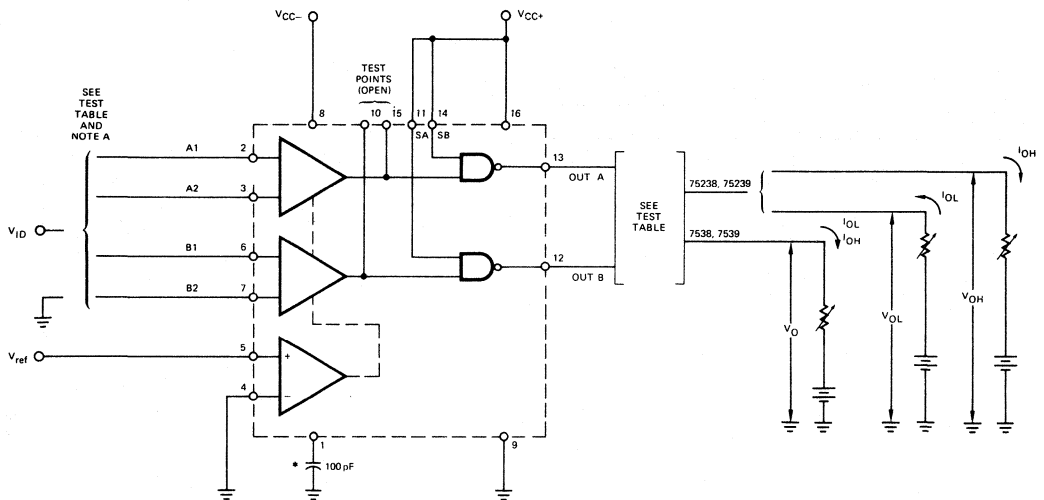
CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS					
				7534, 7535, 75232, 75233			75234, 75235		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
7534, 75232, 75234	A1-A2	15 mV	≤11 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA	≤0.4 V		16 mA
7535, 75233, 75235	A1-A2	15 mV	≤ 8 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤0.4 V		16 mA	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤0.4 V		16 mA	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

Fig. 1c – V_T

DC TEST CIRCUITS (Cont'd)

7538/39, 75238/239



*Required for 7538/7539

TEST TABLE

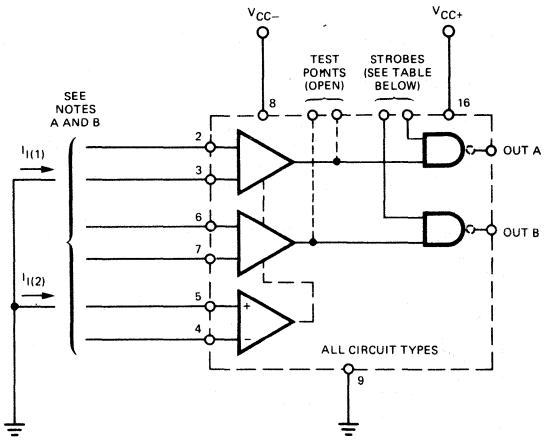
CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS					
				7538, 7539			75238, 75239		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
7538, 75238	A1-A2	15 mV	≤11 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA	≤0.4 V		16 mA
7539, 75239	A1-A2	15 mV	≤ 8 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤0.4 V		16 mA	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤0.4 V		16 mA	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

Fig. 1d – V_T

DC TEST CIRCUITS (Cont'd)

ALL CIRCUIT TYPES



PIN CONNECTIONS (Other than those shown above)

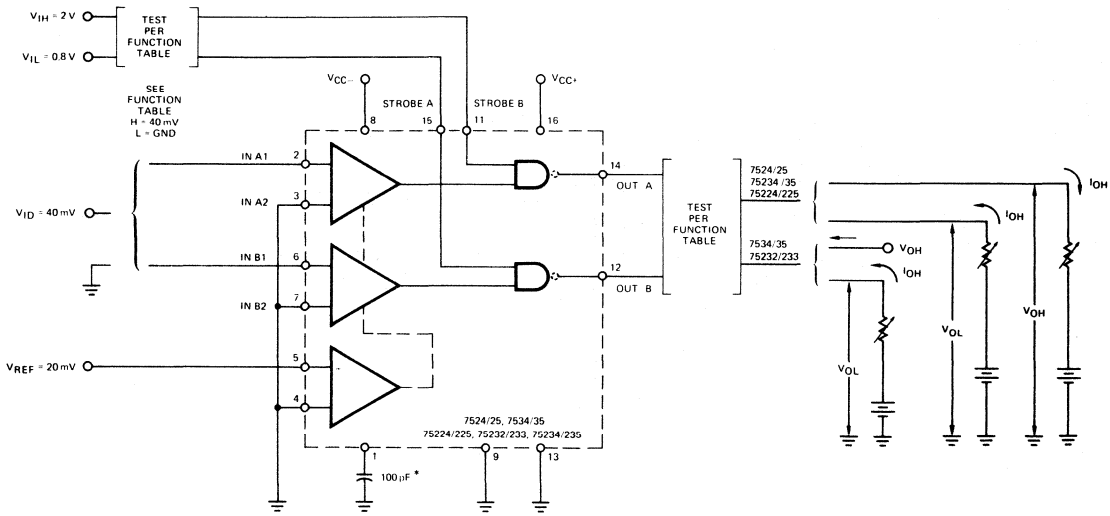
CIRCUIT TYPES	100 pF TO GROUND	APPLY GROUND	LEAVE OPEN
7524, 7525	External Capacitor (Pin 1)	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
7528, 7529, 7538, 7539	External Capacitor (Pin 1)	Strobes A and B (Pins 14, 11)	Test Points 1 and 2 Outputs A and B (Pins 15, 10, 13, 12)
7534, 7535	External Capacitor (Pin 1)	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
75224, 75225, 75232, 75233, 75234, 75235	Not Required	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
75238, 75239	Not Required	Strobes A and B (Pins 14, 11)	Test Points 1 and 2 Outputs A and B (Pins 15, 10, 13, 12)

NOTES:
A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

Fig. 2 – I_{IB}, I_{IO}

DC TEST CIRCUITS (Cont'd)

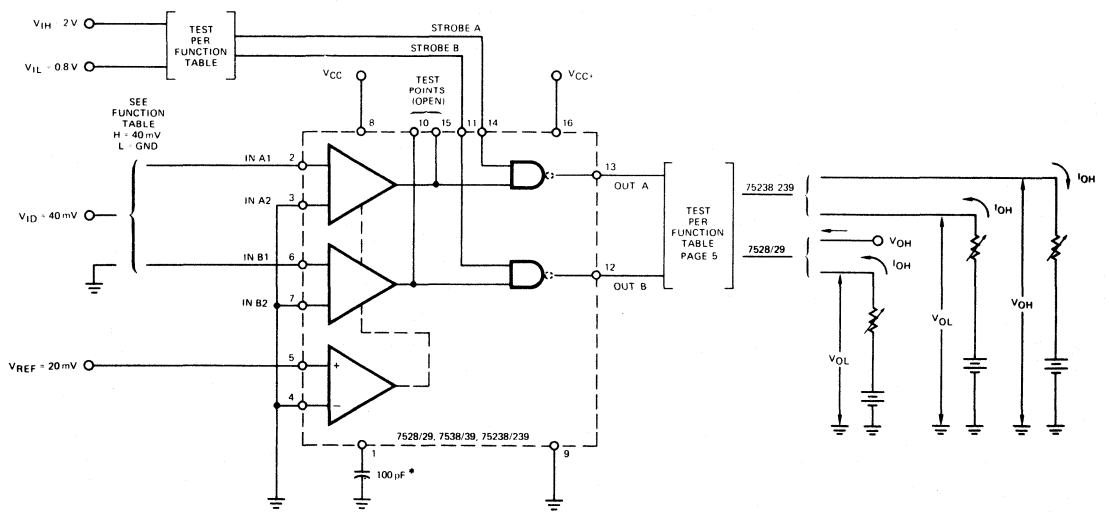
7524/25, 7534/35, 75224/225, 75232/233, 75234/235



*Required for 7524, 7525, 7534 and 7535.

Fig. 3a – V_{IH}, V_{IL}, V_{OH}, V_{OL}

7528/29, 7538/39, 75238/239

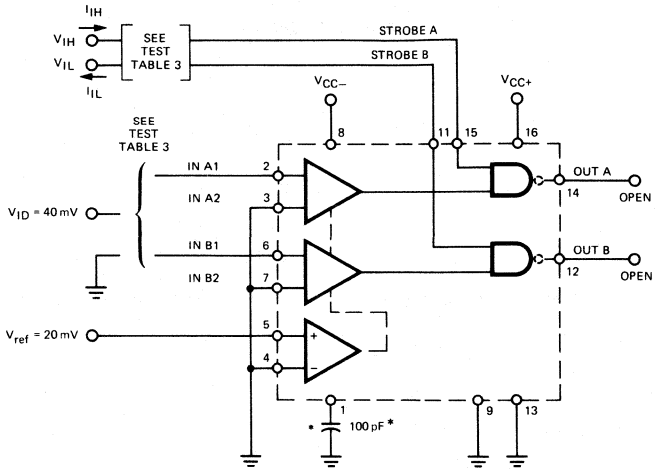


*Required for 7528/29; 7538/39

Fig. 3B – V_{IH}, V_{IL}, V_{OH}, V_{OL}

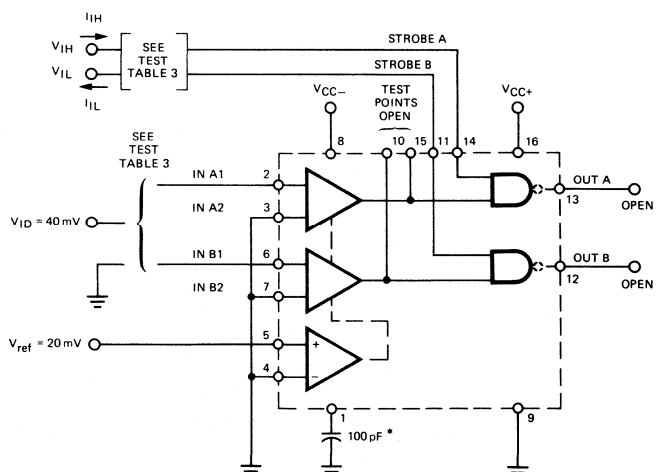
DC TEST CIRCUITS (Cont'd)

7524/25, 7534/35, 75224/225, 75232/233, 75234/235



*Required fro 7524/25, 7534/35

7528/29, 7538/39, 75238/239



*Required for 7528/29, 7538/39

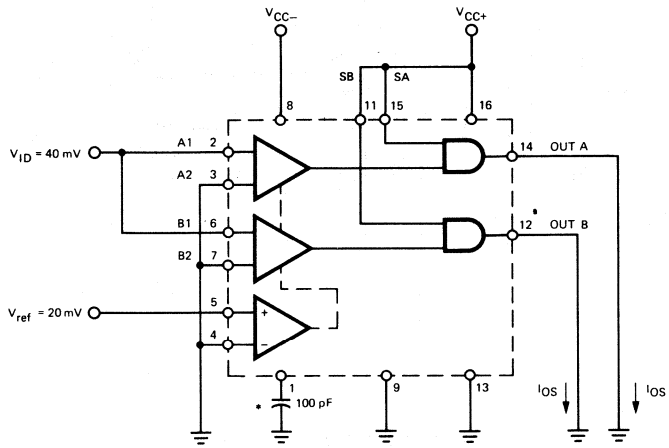
TEST TABLE 3

TEST	INPUT A1	INPUT B1	STROBE A	STROBE B
I_{IH} at Strobe A	GND	GND	V_{IH}	V_{IL}
I_{IH} at Strobe B	GND	GND	V_{IL}	V_{IH}
I_{IL} at Strobe A	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at Strobe B	GND	V_{ID}	V_{IL}	V_{IL}

Fig. 4 – I_{IH}, I_{IL}

DC TEST CIRCUITS (Cont'd)

7524/25, 75224/225



*Required for 7524/7525.

Fig. 5a – I_{OS}

7528/29

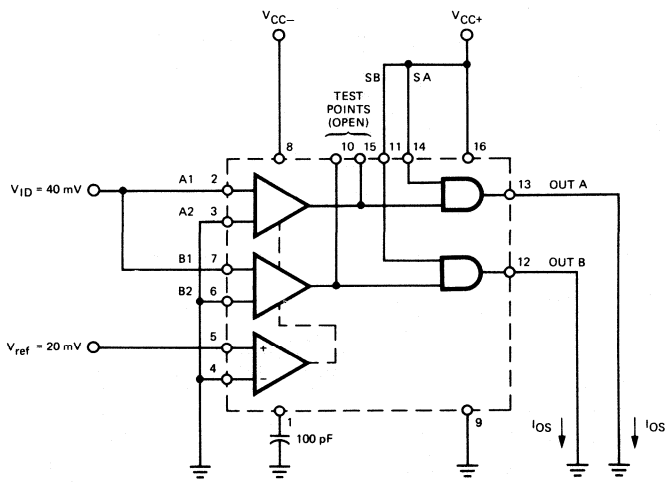


Fig. 5b – I_{OS}

DC TEST CIRCUITS (Cont'd)

75234/235

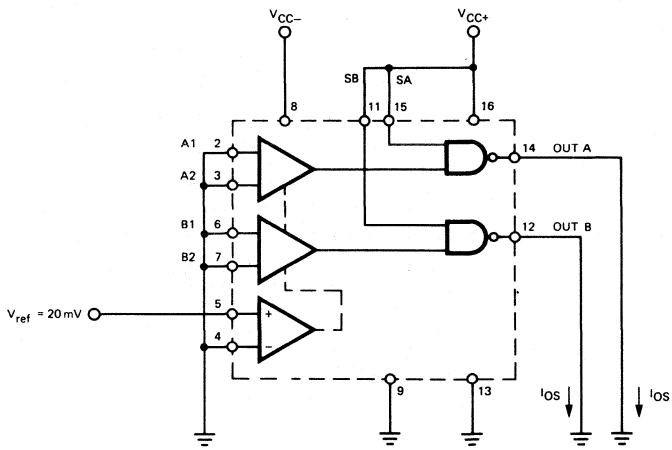


Fig. 5c – I_{OS}

75238/239

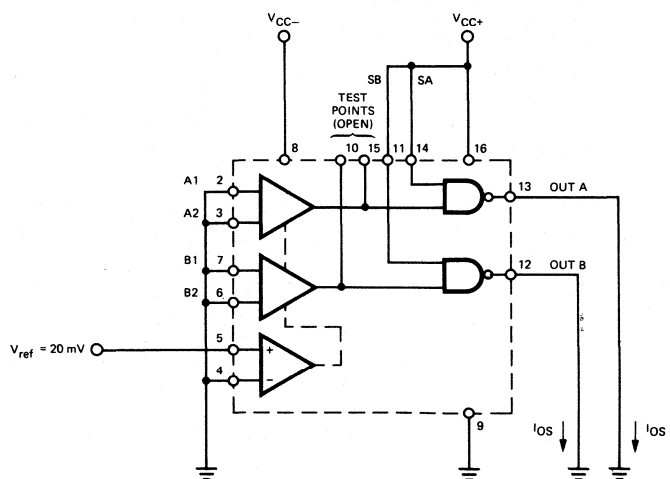
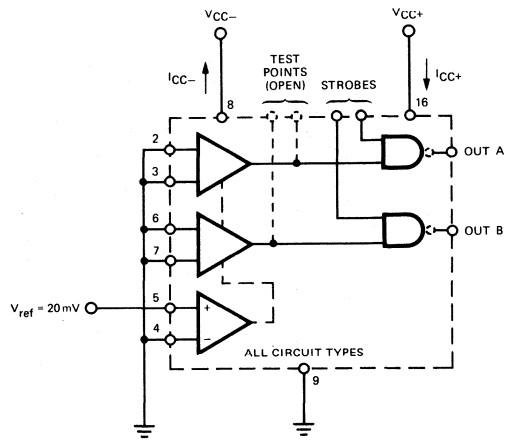


Fig. 5d – I_{OS}

11

DC TEST CIRCUITS (Cont'd)

ALL CIRCUIT TYPES



*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PIN CONNECTIONS (Other than those shown above)

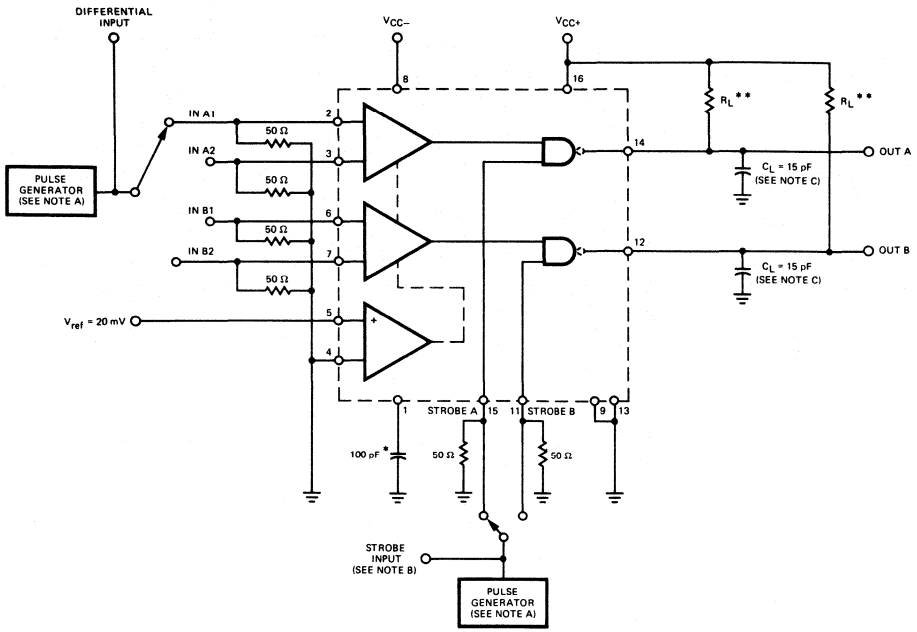
CIRCUIT TYPES	100 pF TO GROUND	APPLY GROUND	LEAVE OPEN
7524, 7525	External Capacitor (Pin 1)	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
7528, 7529, 7538, 7539	External Capacitor (Pin 1)	Strobes A and B (Pins 14, 11)	Test Points 1 and 2 Outputs A and B (Pins 15, 10, 13, 12)
7534, 7535	External Capacitor (Pin 1)	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
75224, 75225, 75232, 75233, 75234, 75235	Not Required	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
75238, 75239	Not Required	Strobes A and B (Pins 14, 11)	Test Points 1 and 2 Outputs A and B (Pins 15, 10, 13, 12)

Fig. 6 – I_{CC+}, I_{CC-}

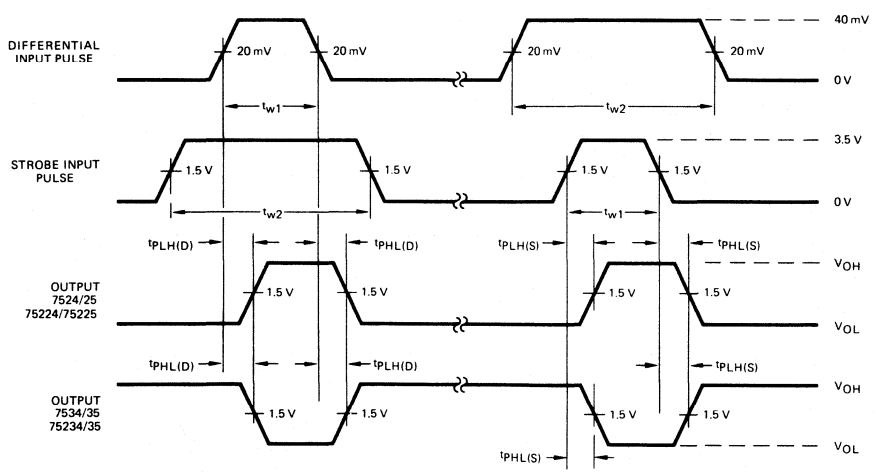
PROPAGATION DELAY TIME

7524/25, 7534/35, 75224, 225, 75234/235

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:

A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to strobe A when inputs A1-A2 are being tested and to strobe B when inputs B1-B2 are being tested.

C. C_L includes probe and jig capacitance.

*Required for 7524/25 and 7534/35.

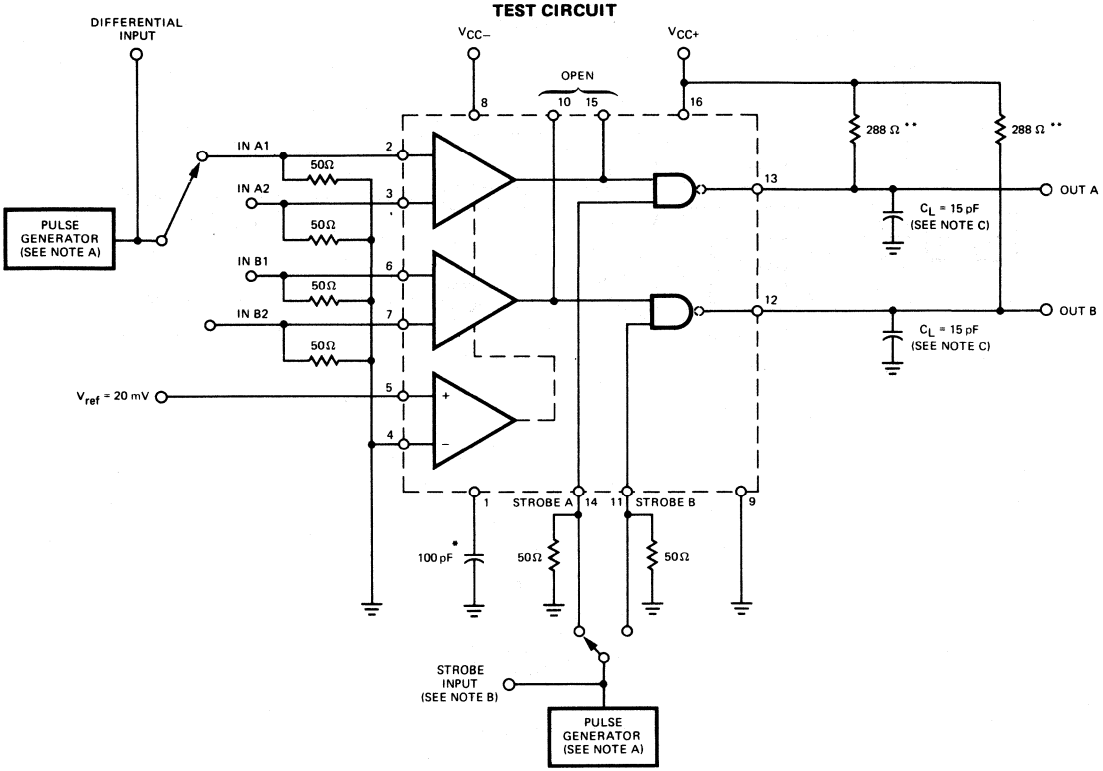
**R_L = 230 Ω for 7534/35 and R_L = 288 Ω for 7524/7525, 75224/225 and 75234/235.

Fig. 7

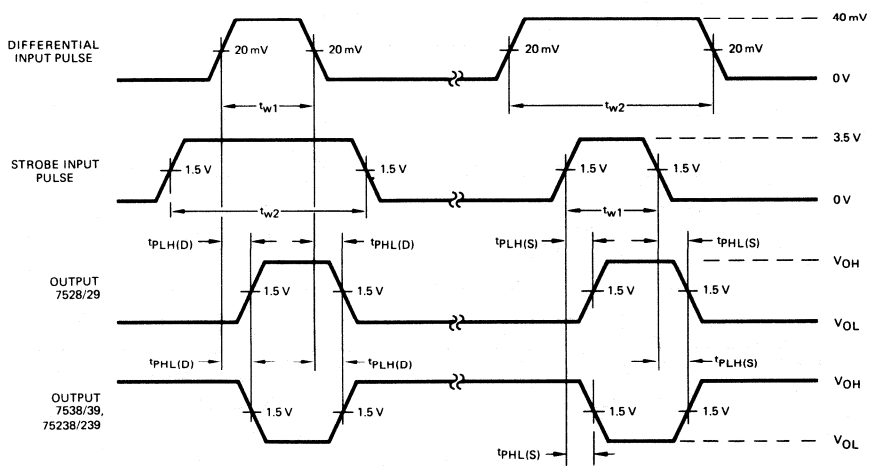
PROPAGATION DELAY TIME

7528/29, 7538/39, 75238/239

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:

A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to strobe A when inputs A1-A2 are being tested and to strobe B when inputs B1-B2 are being tested.

C. C_L includes probe and jig capacitance.

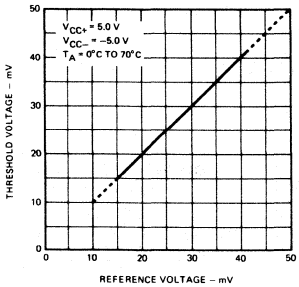
**R_L = 230 Ω for 7538 and 7539.

*Required for 7528/29, 7538/39.

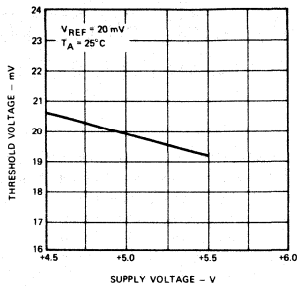
Fig. 8

TYPICAL PERFORMANCE CURVES

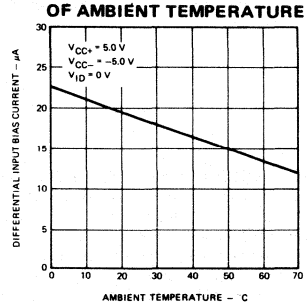
THRESHOLD VOLTAGE AS A FUNCTION OF REFERENCE VOLTAGE



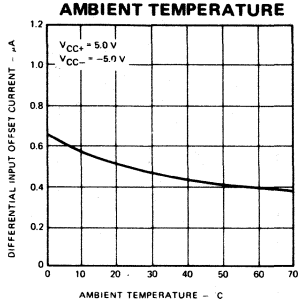
THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



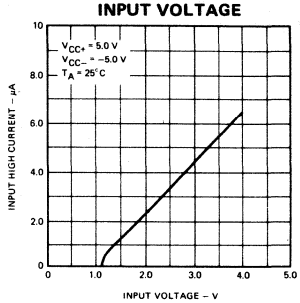
DIFFERENTIAL INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



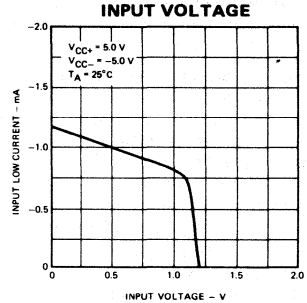
DIFFERENTIAL INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



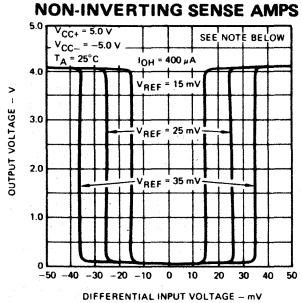
INPUT HIGH CURRENT AS A FUNCTION OF INPUT VOLTAGE



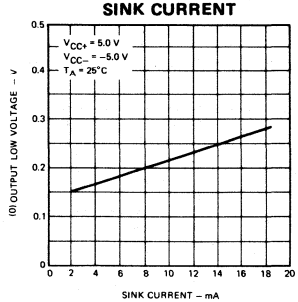
INPUT LOW CURRENT AS A FUNCTION OF INPUT VOLTAGE



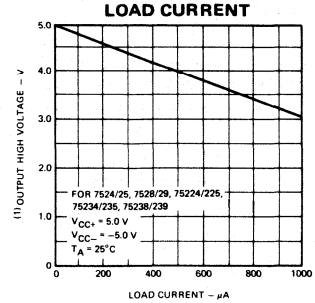
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE FOR ALL NON-INVERTING SENSE AMPS



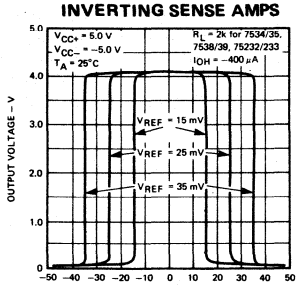
OUTPUT LOW VOLTAGE AS A FUNCTION OF SINK CURRENT



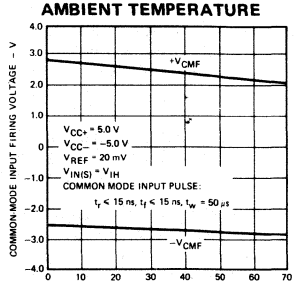
OUTPUT HIGH VOLTAGE AS A FUNCTION OF LOAD CURRENT



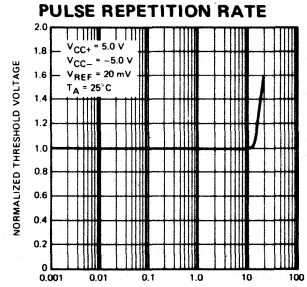
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE FOR ALL INVERTING SENSE AMPS



COMMON MODE FIRING VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



NORMALIZED THRESHOLD VOLTAGE AS A FUNCTION OF PULSE REPETITION RATE



11

55/75107A • 55/75108A
55/75107B • 55/75108B

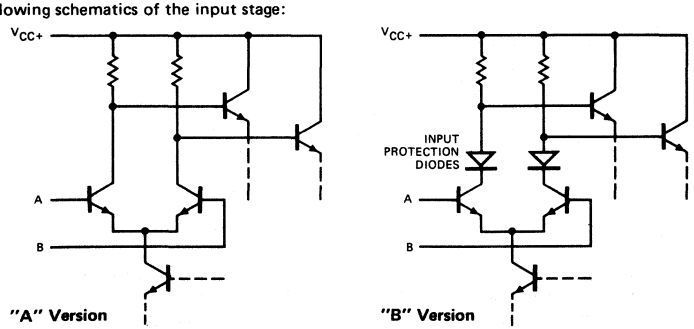
DUAL LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

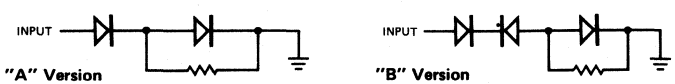
GENERAL DESCRIPTION – The 55/75107A/B and 55/75108A/B are high speed, two-channel Line Receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3V but can be increased to ±15V by the use of input attenuators. Separate or common strobes are available. The 55/75107A/B circuit features an active pull-up (totem pole output). The 55/75108A/B circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the 55109/75109 and 55110/75110 line drivers. The 55/75107A/B and 55/75108A/B line receivers are useful in high speed balanced, unbalanced and party line transmission systems and as data comparators. (See following description of A and B versions.)

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON-MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **HIGH INPUT SENSITIVITY**
- **INPUT COMMON-MODE VOLTAGE RANGE OF ±3 V**
- **SEPARATE OR COMMON STROBES**
- **TTL OR DTL DRIVE CAPABILITY**
- **WIRED-OR OUTPUT CAPABILITY**
- **HIGH DC NOISE MARGINS**
- **STROBE INPUT CLAMP DIODES**
- **55/75107B SERIES DEVICES ARE DIRECT REPLACEMENTS FOR 55/75107A SERIES DEVICES**
- **B VERSION AVAILABLE UPON REQUEST**
- **INPUT IS DIODE PROTECTED AGAINST POWER-OFF LOADING ON B VERSIONS DEVICES**

The essential difference between the 55/75107A and 55/75107B versions is shown in the following schematics of the input stage:

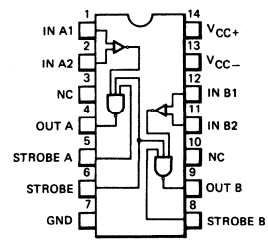


The input protection diodes are useful in certain party-line systems which may have multiple V_{CC+} power supplies and, in which case, may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4 V. Since this is not a widespread application problem, both the A and B versions will be available. The ratings and characteristic specifications of the B versions are the same as those of the A versions. The B versions will be supplied upon request.

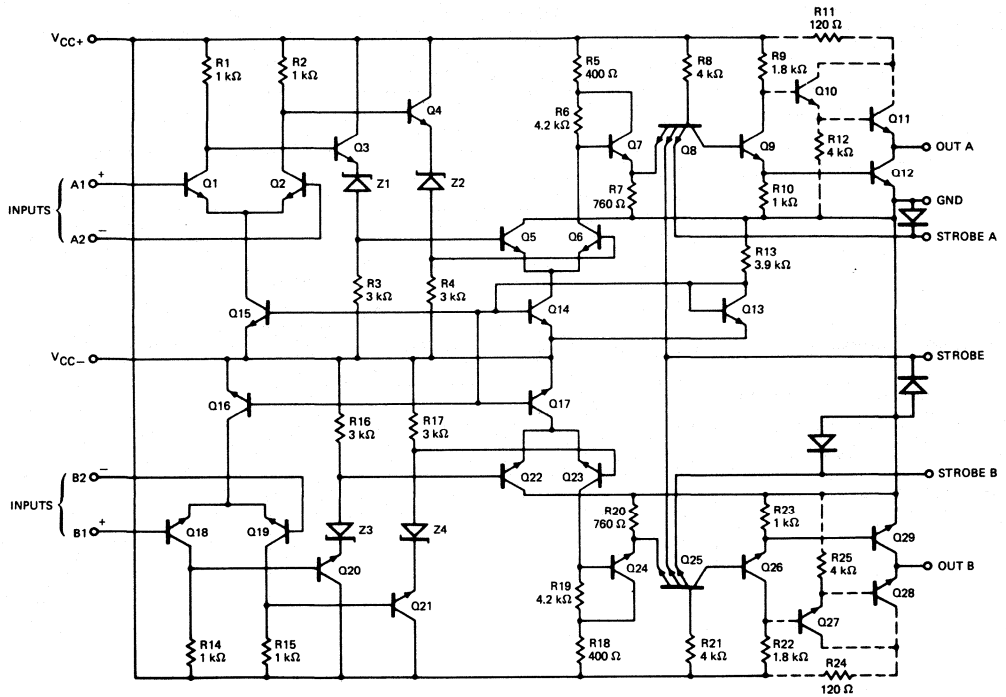
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
55107A	55107AFM
55107A	55107ADM
75107A	75107ADC
75107A	75107APC
55108A	55108AFM
55108A	55108ADM
75108A	75108ADC
75108A	75108APC
55107B	55107BFM
55107B	55107BDM
75107B	75107BDC
75107B	75107BPC
55108B	55108BFM
55108B	55108BDM
75108B	75108BDC
75108B	75108BPC

EQUIVALENT CIRCUIT



NOTE:
Components shown with dashed lines are applicable to the 55107A/B and 75107A/B only. See preceding description for differences between A and B versions.

11

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	±7 V
Internal Power Dissipation (Note 3)	670 mW
Differential Input Voltage (Note 2)	±6 V
Common Mode Input Voltage (Note 1)	±5 V
Strobe Input Voltage (Note 1)	5.5 V
Operating Temperature Range	
55107A/107B/108A/108B	−55°C to +125°C
75107A/107B/108A/108B	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Notes on following pages.

ELECTRICAL CHARACTERISTICS 55/75107A, 55/75107B

(Ratings Apply Over Full Ambient Temperature Range With V_{CC+} = Max and V_{CC-} = Max, unless otherwise noted) (Notes 4 & 6)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3 V to +3 V			30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2 V, V_{CM} = −3 V to +3 V				−10	μA
$I_{IH(G)}$	Gate Input HIGH Current	V_{GATE} = 2.4 V				40	μA
		V_{GATE} = V+				1.0	mA
$I_{IL(G)}$	Gate Input LOW Current	V_{GATE} = 0.4 V				−1.6	mA
$I_{IH(S)}$	Strobe Input HIGH Current	V_{STROBE} = 2.4 V				80	μA
		V_{STROBE} = V+				2.0	mA
$I_{IL(S)}$	Strobe Input LOW Current	V_{STROBE} = 0.4 V				−3.2	mA
V_{OH}	Output HIGH Voltage	I_L = −400 μA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN	2.4			V
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN			0.4	V
I_{SC}	Short-Circuit Output Current	V_{OUT} = 0 (Note 5)		−18		−70	mA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			−8.4	−15	mA

AC CHARACTERISTICS (V_{CC+} = +5 V, V_{CC-} = −5 V, R_L = 390 Ω, C_L = 50 pF, T_A = 25°C. See Test Circuit)

t_{PLH} (D)	Propagation Delay Time			17	25	ns
t_{PHL} (D)				17	25	ns
t_{PLH} (S)				10	15	ns
t_{PHL} (S)				10	15	ns

ELECTRICAL CHARACTERISTICS 55/75108A, 55/75108B

(Ratings Apply Over Full Ambient Temperature Range With V_{CC+} = Max and V_{CC-} = Max, unless otherwise noted) (Notes 4 & 6)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3 V to +3 V			30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2 V, V_{CM} = −3 V to +3 V				−10	μA
$I_{IH(G)}$	Gate Input HIGH Current	V_{GATE} = 2.4 V				40	μA
		V_{GATE} = V+				1.0	mA
$I_{IL(G)}$	Gate Input LOW Current	V_{GATE} = 0.4 V				−1.6	mA
$I_{IH(S)}$	Strobe Input HIGH Current	V_{STROBE} = 2.4 V				80	μA
		V_{STROBE} = V+				2.0	mA
$I_{IL(S)}$	Strobe Input LOW Current	V_{STROBE} = 0.4 V				−3.2	mA
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN			0.4	V
V_{IH}	Output HIGH Current	V_{OUT} = V+	V_{CC+} = MIN, V_{CC-} = MIN			250	μA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			−8.4	−15	mA

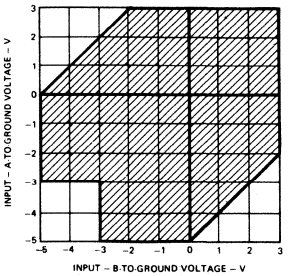
AC CHARACTERISTICS (V_{CC+} = +5 V, V_{CC-} = −5 V, R_L = 390 Ω, C_L = 15 pF, T_A = 25°C. See Test Circuit)

t_{PLH} (D)	Propagation Delay Time			19	25	ns
t_{PHL} (D)				19	25	ns
t_{PLH} (S)				13	20	ns
t_{PHL} (S)				13	20	ns

TRUTH TABLE

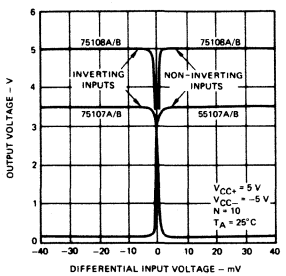
DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT
$V_{ID} \geq 25$ mV	L or H	L or H	H
−25 mV < V_{ID} <25 mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

RECOMMENDED COMBINATIONS OF INPUT VOLTAGE FOR LINE RECEIVERS

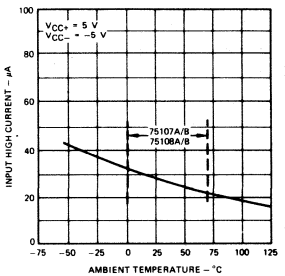


TYPICAL PERFORMANCE CURSES

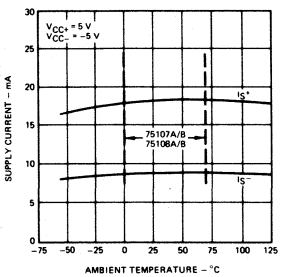
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



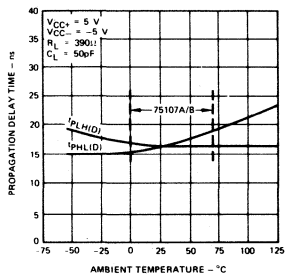
INPUT HIGH CURRENT INTO 1A OR 2A AS A FUNCTION OF AMBIENT TEMPERATURE



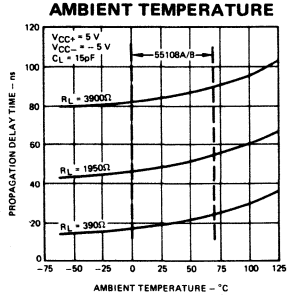
HIGH LOGIC LEVEL SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



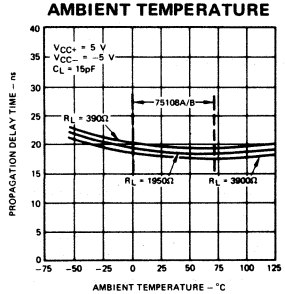
55/75107A, 55/75107B PROPAGATION DELAY TIME (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



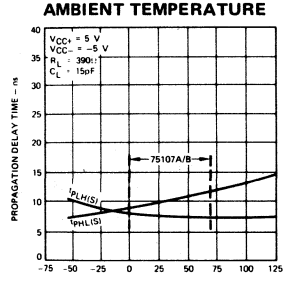
55/75108A, 55/75108B PROPAGATION DELAY TIME LOW-TO-HIGH LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



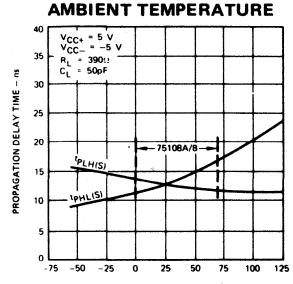
55/75108A, 55/75108B PROPAGATION DELAY TIME HIGH-TO-LOW LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



55/75107A, 55/75107B PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



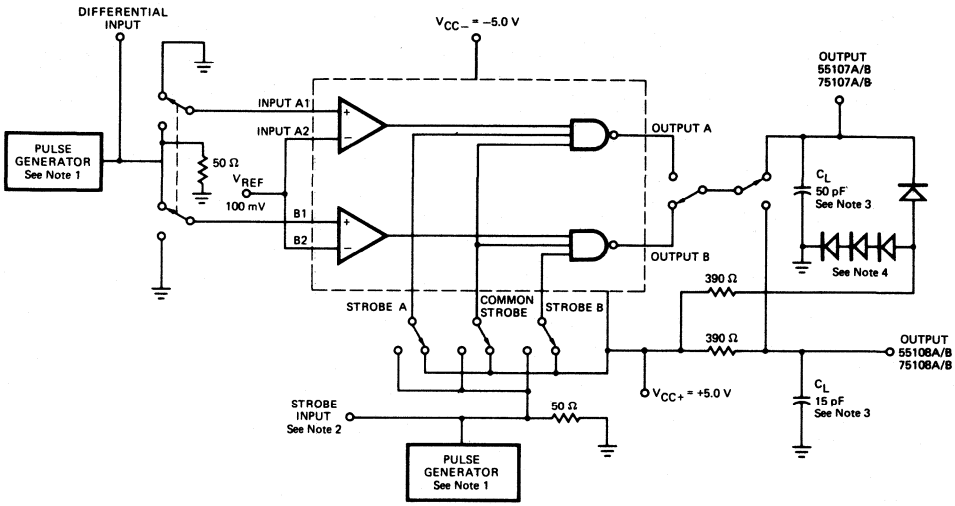
55/75108A, 55/75108B PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



NOTES:
1. These voltages are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For Flatpak derate linearly at 7.1 mW/°C above 60°C.
4. For 55107A/B and 55108A/B guaranteed supply voltage range is ±4.5 V to ±5.5 V. Operating temperature range is $-55°C \leq T_A \leq +125°C$. For 75107A/B and 75108A/B guaranteed supply voltage range is ±4.75 V to ±5.25 V. Operating temperature range is $0°C \leq T_A \leq 70°C$.
5. Note more than one (1) output should be shorted at a time.
6. V_{CC-} Max implies V_{CC-} = −5.5 V or −5.25 V, depending on device type.

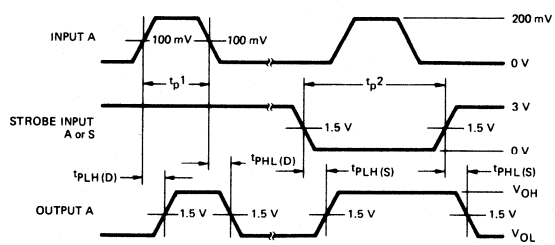
AC CHARACTERISTICS

AC TEST CIRCUIT



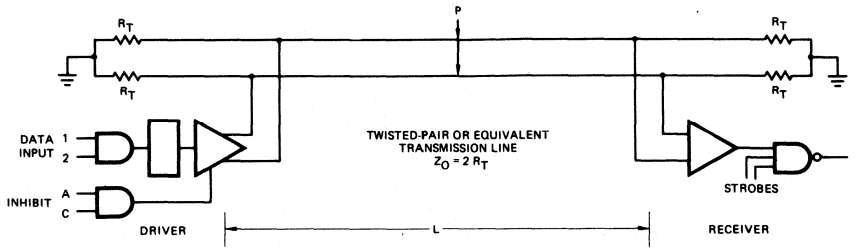
NOTES:
1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 μs, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested: to common Strobe when inputs A1-A2 or B1-B2 are being tested, and to Strobe B when inputs B1-B2 are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

VOLTAGE WAVEFORMS



APPLICATION

BASIC BALANCED-LINE TRANSMISSION SYSTEM



The 55/75107A/B dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30+1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \simeq 1/2\ I_{OUT(on)} \cdot R_T$$

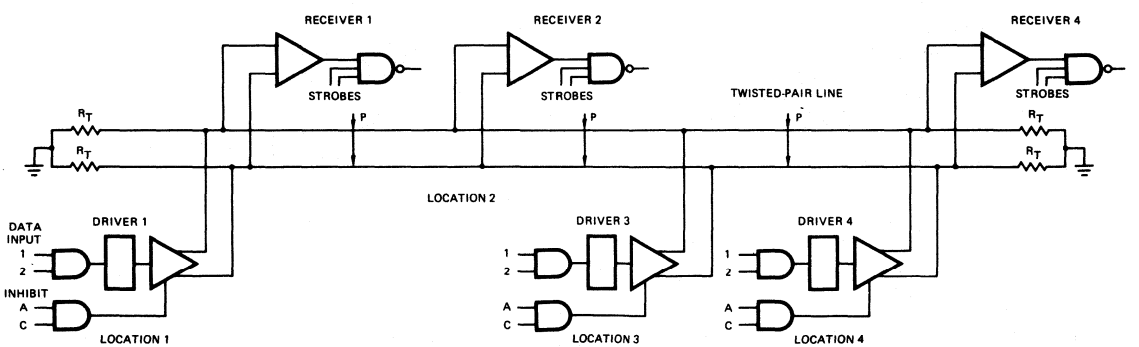
High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \simeq I_{OUT(on)} \cdot R_T$$

11

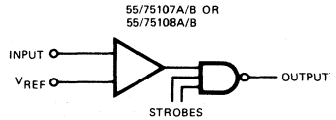
DATA-BUS OR PARTY-LINE SYSTEM



The strobe feature of the receivers and the inhibit feature of the drivers allow the 55/75107A/B dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The 55/75107A/B device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

APPLICATION (Cont'd)

UNBALANCED OR SINGLE-LINE SYSTEMS



The 55/75107A/B dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

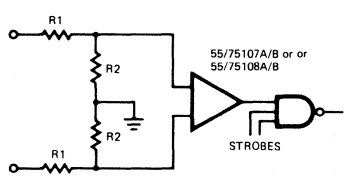
The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0 V to +3.0 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

PRECAUTIONS IN THE USE OF 55/75107A/B AND 55/75108A/B DUAL LINE RECEIVERS

The following precaution should be observed when using or testing 55/75107A/B line circuits:

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0 V and +3.0 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

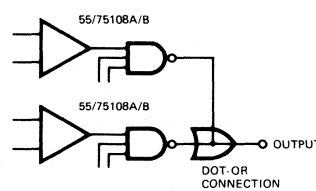
INCREASING COMMON-MODE INPUT VOLTAGE RANGE OF RECEIVER



FOR BALANCED, TERMINATED LINES,
$Z_{OUT} = 2R1 + 2R2$

The 55/75107A/B and 55/75108A/B line receivers feature a common-mode input voltage range of ±3.0 V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ±3.0 V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

55108A/75108A DOT-OR OUTPUT CONNECTIONS



The 55/75108A/B line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other 55/75108A/B outputs. This allows a level of logic to be implemented without additional logic delay.

55109 • 75109 • 55110 • 75110

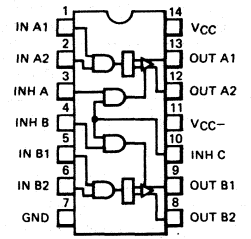
DUAL LINE DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55109/75109 and 55110/75110 are Dual Line Drivers featuring independent channels with common supply voltage and ground terminals. The major difference between the 55109/75109 and the 55110/75110 drivers is the output current specification. The output current is nominally 6 mA for the 55109/75109 and 12 mA for the 55110/75110. The driver circuits have a constant output that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off by appropriate logic levels at the inhibit inputs. The circuit also features an inhibit input that is common to both drivers, providing more circuit versatility. The common mode voltage range of the driver outputs is −3.0 V to +10 V, which allows a common mode voltage on the line without affecting the driver performance. (See Applications Circuit.)

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **TTL INPUT COMPATIBILITY**
- **CURRENT MODE OUTPUT (6mA or 12mA TYPICAL)**
- **HIGH OUTPUT IMPEDANCE**
- **HIGH COMMON MODE OUTPUT VOLTAGE RANGE (−3V to 10V)**
- **INHIBITOR AVAILABLE FOR DRIVER SELECTION**

CONNECTION DIAGRAM
14-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F

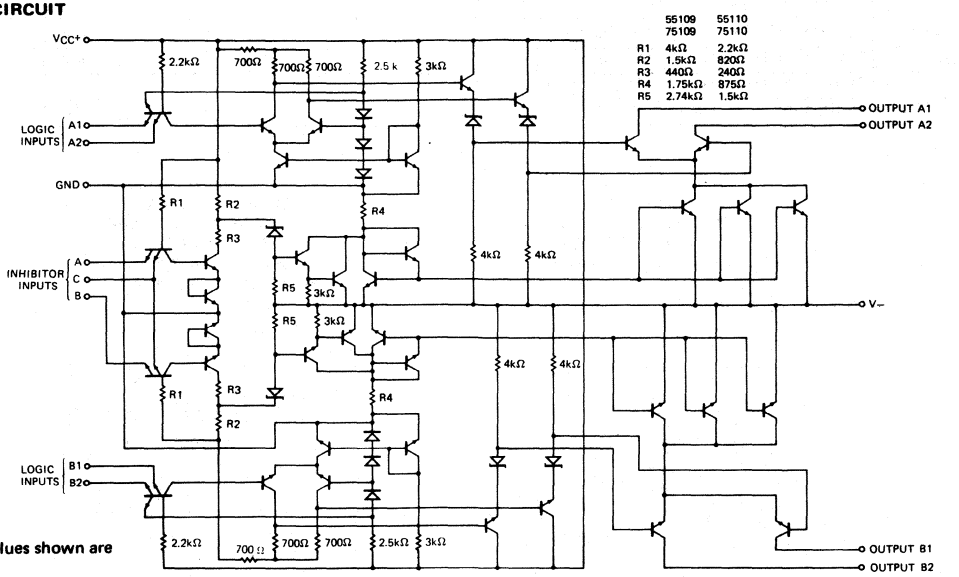


ORDER INFORMATION

TYPE	PART NO.
55109	55109DM
55109	75109DC
75109	75109PC
75109	55110DM
55110	75110DC
55110	75110PC
75110	55109FM
75110	55110FM

11

EQUIVALENT CIRCUIT



NOTES:
1. Component values shown are nominal.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC+} (See Note 1)	7 V
Supply Voltage V_{CC-} (See Note 1)	−7 V
Logic and Inhibitor Input Voltages (See Note 1)	5.5 V
Common-Mode Output Voltage (See Note 1)	−5 to 12 V
Operating Free-Air Temperature Range	
55109/55110	−55°C to +125°C
75109/75110	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation (See Note 5)	600 mW
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (soldering, 10 seconds)	260°C

Notes on the following pages.

55109 • 75109

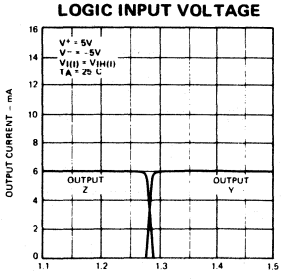
ELECTRICAL CHARACTERISTICS (Ratings apply over full ambient temperature range with V_{CC+} = Max and V_{CC-} = Max, unless otherwise specified. (Notes 2 & 4)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V			40	µA
		V_{IN} = MAX. V+			1.0	mA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V			−3.0	mA
$I_{IH(I)}$	Inhibit Input HIGH Current	$V_{INHIBIT}$ = 2.4 V			40	µA
		$V_{INHIBIT}$ = MAX. V+			1.0	mA
$I_{IL(I)}$	Inhibit Input LOW Current	$V_{INHIBIT}$ = 0.4 V			−3.0	mA
$I_{IH(CI)}$	Common-Inhibit HIGH Current	$V_{INHIBIT}$ = 2.4 V			80	µA
		$V_{INHIBIT}$ = MAX. V+			2.0	mA
$I_{IL(CI)}$	Common-Inhibit LOW Current	$V_{INHIBIT}$ = 0.4 V			−6.0	mA
$I_{O(ON)}$	ON-STATE Output Current	V_{CC+} = MAX., V_{CC-} = MAX.			7.0	mA
		V_{CC+} = MIN., V_{CC-} = MAX.	3.5			mA
$I_{O(OFF)}$	OFF-STATE Output Current	V_{CC+} = MIN., V_{CC-} = MIN.			100	µA
I_{CC+} (ON)	Supply Current with Driver Enabled	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 2.0 V		18	30	mA
I_{CC-} (ON)	Supply Current with Driver Enabled	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 2.0 V		−18	−30	mA
I_{CC+} (OFF)	Supply Current with Driver Inhibited	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 0.4 V		18		mA
I_{CC-} (OFF)	Supply Current with Driver Inhibited	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 0.4 V		−10		mA

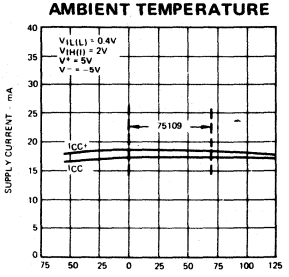
AC CHARACTERISTICS [V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C]

t_{PLH} (L)	Propagation Delay Time (Logic Inputs)	(See Test Circuit)		9.0	15	ns
t_{PHL} (L)	Propagation Delay Time (Logic Inputs)			9.0	15	ns
t_{PLH} (I)	Propagation Delay Time (Inhibitor Inputs)			16	25	ns
t_{PHL} (I)	Propagation Delay Time (Inhibitor Inputs)			13	25	ns

55109, 75109 OUTPUT CURRENT AS A FUNCTION OF LOGIC INPUT VOLTAGE



55109, 75109 SUPPLY CURRENT WITH DRIVER ENABLED AS A FUNCTION OF AMBIENT TEMPERATURE



RECOMMENDED OPERATING CONDITIONS (Note 3)

	55109 55110			75109 75110			
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}+ Positive Supply Voltage (Note 1)	4.5	5.0	5.5	4.75	5.0	5.25	V
V_{CC}− Negative Supply Voltage (Note 1)	−5.5	−5.0	−4.5	−5 .25	−5.0	−4.75	V
Positive Common Mode Output Voltage (Note 1)	0		10	0		10	V
Negative Common Mode Output Voltage (Note 1)	−3.0		0	−3.0		0	V

55110 • 75110

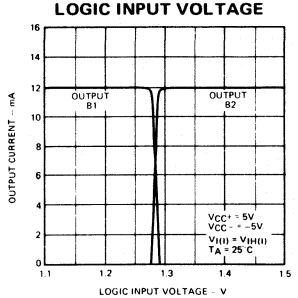
ELECTRICAL CHARACTERISTICS (Ratings apply over full ambient temperature range with V+ = Max and V− = Max, unless otherwise specified. (Notes 2 & 4)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V			40	μA
		V_{IN} = Max. V_{CC}+			1.0	mA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V			−3.0	mA
$I_{IH(I)}$	Inhibit Input HIGH Current	$V_{INHIBIT}$ = 2.4 V			40	μA
		$V_{INHIBIT}$ = Max. V_{CC}+			1.0	mA
$I_{IL(I)}$	Inhibit Input LOW Current	$V_{INHIBIT}$ = 0.4 V			−3.0	mA
$I_{IH(CI)}$	Common-Inhibit Input HIGH Current	$V_{INHIBIT}$ = 2.4 V			80	μA
		$V_{INHIBIT}$ = Max. V_{CC}+			2.0	mA
$I_{IL(CI)}$	Common-Inhibit Input LOW Current	$V_{INHIBIT}$ = 0.4 V			−6.0	mA
$I_{O(ON)}$	ON-STATE Output Current	V_{CC}+ = Max., V_{CC} − = Max.			15	mA
		V_{CC}+ = Min., V_{CC}− = Max.	6.5			mA
	OFF-STATE Output Current	V_{CC}+ = Min., V_{CC}− = Min.			100	μA
I_{CC} + (ON)	Supply Current with Driver Enabled	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 2.0 V		23	35	mA
I_{CC} − (ON)	Supply Current with Driver Enabled	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 2.0 V		−34	−50	mA
I_{CC} + (OFF)	Supply Current with Driver Inhibited	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 0.4 V		21		mA
I_{CC} − (OFF)	Supply Current with Driver Inhibited	V_{IN} = 0.4 V, $V_{INHIBIT}$ = 0.4 V		−17		mA

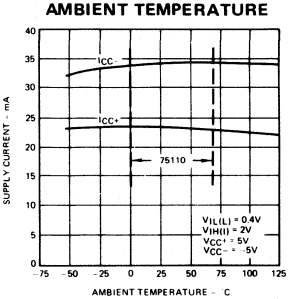
AC CHARACTERISTICS (V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C)

t_{PLH} (L)	Propagation Delay Time (Logic Inputs)	(See Test Circuit)		9.0	15	ns
t_{PHL} (L)	Propagation Delay Time (Logic Inputs)			9.0	15	ns
t_{PLH} (I)	Propagation Delay Time (Inhibitor Inputs)			16	25	ns
t_{PHL} (I)	Propagation Delay Time (Inhibitor Inputs)			13	25	ns

55110, 75110 OUTPUT CURRENT AS A FUNCTION OF LOGIC INPUT VOLTAGE



55110, 75110 SUPPLY CURRENT WITH DRIVER ENABLED AS A FUNCTION OF AMBIENT TEMPERATURE

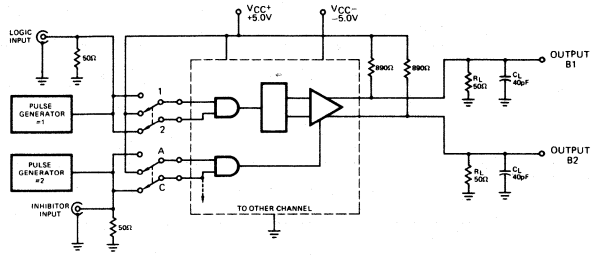


NOTES:

1. These voltage values are with respect to the network ground terminal.
2. For 55109 and 55110, guaranteed supply voltage range is ±4.5V to ±5.5V. Operating temperature range is $-55^{\circ}C \leq T_A \leq +125^{\circ}C$. For 75109 and 75110, guaranteed supply voltage range is ±4.75V to ±5.25V. Operating temperature range is $0^{\circ}C \leq T_A \leq +70^{\circ}C$.
3. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.
4. V_{CC}− Max implies V_{CC}− = −5.5V or −5.25V, depending on device type.
5. For Hermetic DIP, derate above 80°C at 8.3 mW/°C. For Flatpak, derate above 65°C at 7.1 mW/°C.

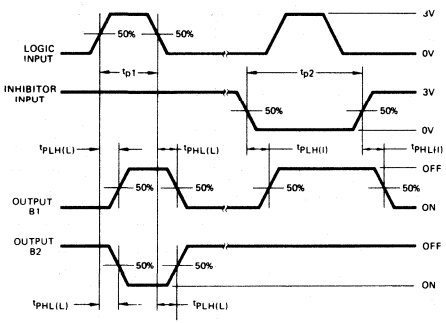
AC CHARACTERISTICS

TEST CIRCUIT



NOTES: 1. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 10 \pm 5$ns, $t_{p1} = 500$ns, PRR = 1MHz, $t_{p2} = 1\mu$s, PRR = 500kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

VOLTAGE WAVEFORMS

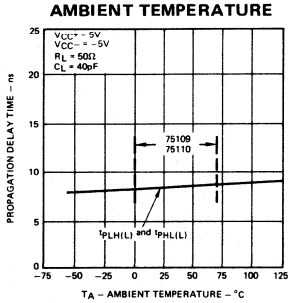


TRUTH TABLE

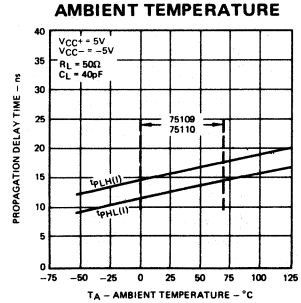
Logic Inputs		Inhibit Inputs		Outputs		
1	2	A/B	COM	1	2	
X	X	L	X	OFF	OFF	INHIBITED
X	X	X	L	OFF	OFF	INHIBITED
L	X	H	H	ON	OFF	
X	L	H	H	ON	OFF	
H	H	H	H	OFF	ON	

H = HIGH Input $\geq V_{IH} \geq 2.0$ Volts
L = LOW Input $\leq V_{IL} \leq 0.8$ Volts
X = Either HIGH or LOW
OFF = Output Transistor is OFF
ON = Output Transistor is ON

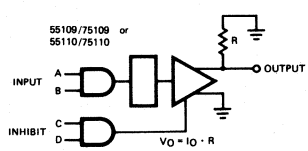
PROPAGATION DELAY TIME (LOGIC INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



PROPAGATION DELAY TIME (INHIBITOR INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



APPLICATIONS



A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and cross-talk problems. For large signal swings, the high output current (12 mA) of the 55110/75110 is recommended. Drivers may be parallelled for higher current. The unused driver output must be tied to ground. The following precaution should be observed when using or testing 55/75109 and 55/75110 dual line drivers.

When only one driver in a package is being used, the outputs of the other driver must either be grounded or inhibited in order to prevent excess power dissipation.

55121 • 75121

DUAL SINGLE-ENDED LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55121/75121 Dual Line Drivers are designed for driving 50 Ω to 500 Ω coaxial cable, strip line, or twisted pair transmission lines. All inputs are TTL or DTL compatible and the emitter-follower outputs enable two or more drivers to operate on the same line in parity line applications.

For a dual line driver to meet the IBM System/360 I/O Interface Specification, see 75123 or 8T23 data sheets.

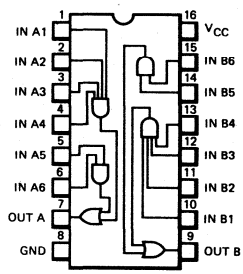
- **HIGH OUTPUT DRIVE CAPABILITY**
- **HIGH SPEED**
- **INPUT CLAMP DIODES**
- **SINGLE 5 V SUPPLY OPERATION**
- **SHORT CIRCUIT PROTECTED**
- **DIRECT REPLACEMENT FOR 8T13**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+6.0 V
Output Voltage (Note 1)	+6.0 V
Supply Voltage (Note 1)	+6.0 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	
Military (55121)	−55°C to +125°C
Commercial (75121)	0°C to +70°C
Lead Temperatures	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	800 mW

NOTES:
1. Voltages are with respect to the ground pin (pin 8)
2. For Hermetic DIP and Molded DIP rating applies to ambient temperatures up to 60°C, above 60°C derate linearly at 8.3 mW/°C. For Flatpak derate linearly at 7.1 mW/°C above 40°C.

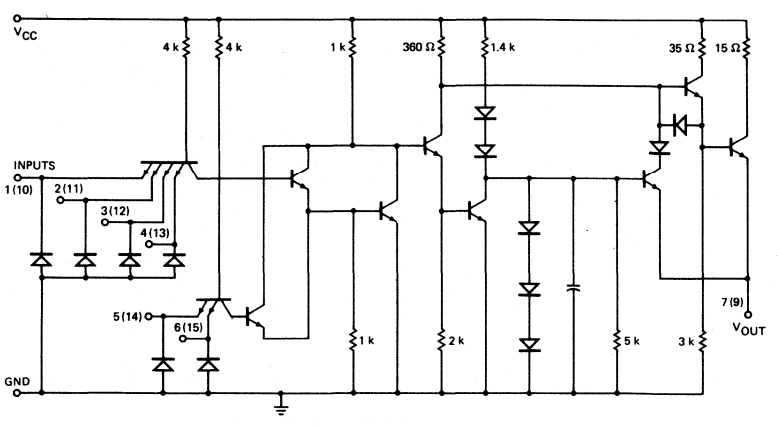
CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
55121	55121DM
55121	55121FM
75121	75121DC
75121	75121PC

EQUIVALENT CIRCUIT (For Each Driver)



55/75121 FUNCTION TABLE

INPUTS						OUTPUT
1	2	3	4	5	6	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Inputs Combinations						L

55121, 75121 RECOMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5	5.25	V
Output HIGH Current, I_{OH}				−75	mA
Operating Ambient Temperature, T_A	55121	−55		125	°C
	75121	0		70	°C

ELECTRICAL CHARACTERISTICS (V_{CC+} = 4.75 V to 5.25 V, Ratings apply over recommended temperature range unless noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_{IN}	Input Clamp Voltage	V_{CC} = 5.0 V, I_{IN} = −12 mA			−1.5	V
$V_{(BR)I}$	Input Breakdown Voltage	V_{CC} = 5.0 V, I_{IN} = 10 mA	5.5			V
V_{OH}	Output HIGH Voltage	V_{IH} = 2.0 V, I_{OH} = −75 mA (Note 3)	2.4			V
I_{OH}	Output HIGH Current	V_{CC} = 5.0 V, V_{IH} = 4.5 V V_{OH} = 2.0 V, T_A = 25°C (Note 3)	−100		−250	mA
I_{OL}	Output LOW Current	V_{IL} = 0.8 V, V_{OL} = 0.4 V (Note 3)			−800	μA
$I_{OUT(off)}$	Off-State Output Current	V_{CC} = 0, V_{OUT} = 3.0 V			500	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V			40	μA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current	V_{CC} = 5.0 V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs HIGH	V_{CC} = 5.25 V, All inputs at 2.0 V Outputs open			28	mA
I_{CCL}	Supply Current, Outputs LOW	V_{CC} = 5.25 V, All inputs at 0.8 V Outputs open			60	mA

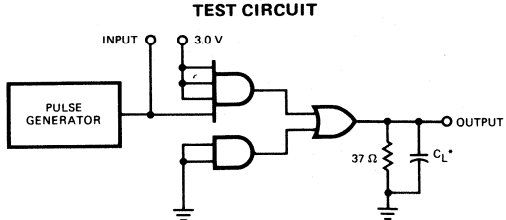
AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	R_L = 37 Ω, C_L = 15 pF See Test Circuit		11	20	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output			8.0	20	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	R_L = 37 Ω, C_L = 1000 pF See Test Circuit		22	50	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output			20	50	

NOTE:
4. The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.

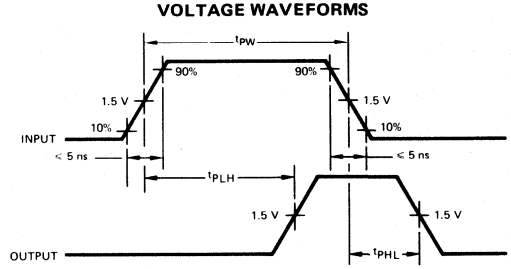
AC CHARACTERISTICS

TEST CIRCUIT



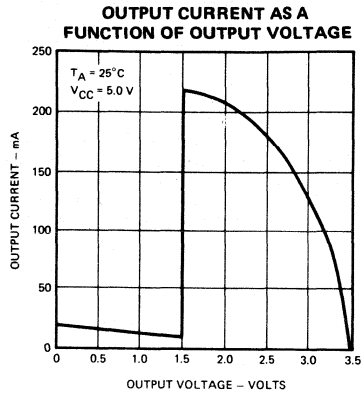
INPUT PULSE:
Amplitude = 2.6 V
t_{PW} = 40 ns (50% Duty Cycle)

VOLTAGE WAVEFORMS



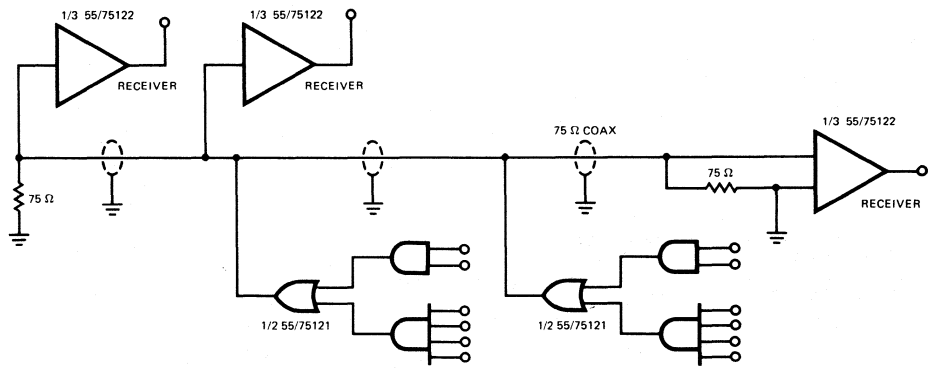
*Includes probe and jig capacitance.

TYPICAL PERFORMANCE CURVE FOR 55121 • 75121



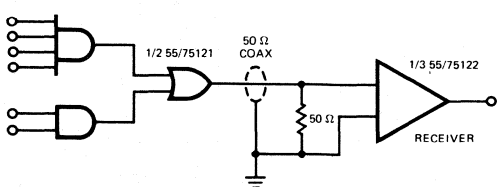
TYPICAL APPLICATIONS

75 Ω PARTY LINE (2 DRIVERS, 3 RECEIVERS)



NOTE: For party line operation, termination of each physical end of the line is recommended.

SIMPLEX OPERATION (1 DRIVER)



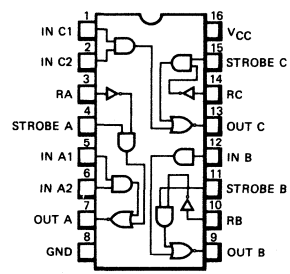
NOTE: For simplex operation, the line should be terminated only at the distant receiver site.

55/75122
TRIPLE LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55122/75122 Triple Line Receiver is designed to receive digital information from coaxial cable, strip line, or twisted pair single ended transmission lines. High input impedance (≈30 kΩ) presents minimal loading to the transmission lines in multiple reciever applications. The 55122/75122 has built-in hysteresis which makes it ideal for such applications as Schmitt triggers, one-shots, and oscillators. Use the 75124 or 8T24 triple line receiver where IBM System/360 I/O Interface Specification must be met.

- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5.0 V SUPPLY OPERATION**
- **DIRECT REPLACEMENT FOR 8T14**

CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1) R Input	+6.0 V
1, 2 or S Input	+5.5 V
Output Voltage (Note 1)	+6.0 V
Supply Voltage (Note 1)	+6.0 V
Output Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (55122)	−55°C to +125°C
Commercial (75122)	0°C to +70°C
Lead Temperatures	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	800 mW

FUNCTION TABLE

INPUTS				OUTPUT
1	2*	R	S	
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = HIGH
L = LOW
X = Don't Care

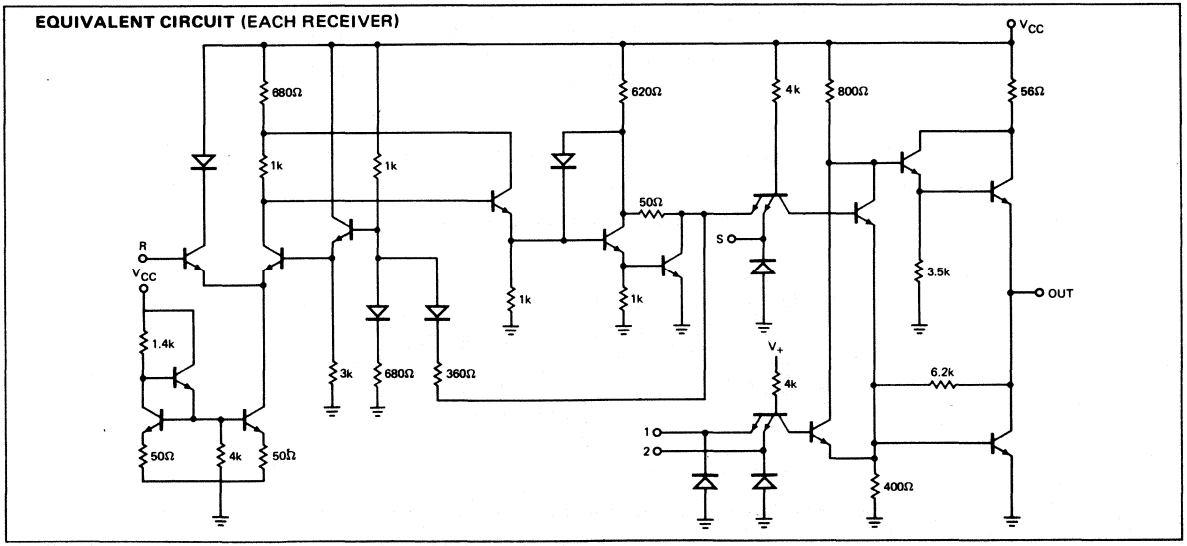
*Input 2 and last two lines of the Function Table are applicable to receivers A and C only.

ORDER INFORMATION

TYPE	PART NO.
55122	55122DM
55122	55122FM
75122	75122DC
75122	75122PC

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Flatpack derate at 7.1 mW/°C above 40°C.

EQUIVALENT CIRCUIT (EACH RECEIVER)



RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5.0	5.25	V
Output HIGH Current, I_{OH}				−500	μA
Output LOW Current, I_{OL}				16	mA
Operating Ambient Temperature, T_A	55122	−55		125	°C
	75122	0		70	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 4.75 V to 5.25 V, T_A = 25°C (unless otherwise noted)

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage	All Inputs		2.0			V
V_{IL}	Input LOW Voltage	All Inputs				0.8	V
$V_{T+} - V_{T-}$	Hysteresis†	R	V_{CC} = 5.0 V, T_A = 25°C	0.3	0.6		V
V_{IN}	Input Clamp Voltage	In 1, 2 or S	V_{CC} = 5.0 V, I_{IN} = −12 mA			−1.5	V
$V_{(BR)IN}$	Input Breakdown Voltage	In 1, 2 or S	V_{CC} = 5.0 V, I_{IN} = 10 mA	5.5			V
V_{OH}	Output HIGH Voltage		V_{IH} = 0 V, V_{IL} = 0.8 V, I_{OH} = −500 μA, See Note 3	2.6			V
			$V_{IN(A)}$ = 0 V, $V_{IN(B)}$ = 0 V, $V_{IN(S)}$ = 2.0 V, $V_{IN(R)}$ = 1.45 V (See Note 4, I_{OH} = −500 μA	2.6			
V_{OL}	Output LOW Voltage		V_{IH} = 2.0 V, V_{IL} = 0.8 V, I_{OL} = 16 mA, See Note 3			0.4	V
			$V_{IN(A)}$ = 0 V, $V_{IN(B)}$ = 0 V, $V_{IN(S)}$ = 2.0 V, $V_{IN(R)}$ = 1.45 V (See Note 5), I_{OL} = 16 mA			0.4	
I_{IH}	Input HIGH Current	In 1, 2 or S	V_{IN} = 4.5 V			40	μA
		R	V_{IN} = 3.8 V			170	
I_{IL}	Input LOW Current	In 1, 2 or S	V_{IN} = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current‡		V_{CC} = 5.0 V, T_A = 25°C	−50		−100	mA
I_{CC}	Supply Current		V_{CC} = 5.25 V			72	mA

†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Hysteresis Test Circuit.

‡Not more than one output should be shorted at a time.

NOTES:

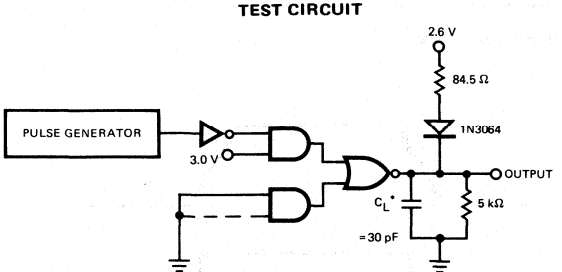
3. The output voltage limits are guaranteed for any appropriate combination of HIGH and LOW inputs specified by the function table for the desired output.
4. Receiver input was at a HIGH level immediately before being reduced to 1.45 V.
5. Receiver input was at a LOW level immediately before being raised to 1.45 V.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	See Test Circuit		20	30	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW			20	30	

AC CHARACTERISTICS

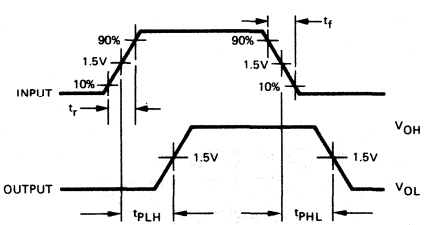
TEST CIRCUIT



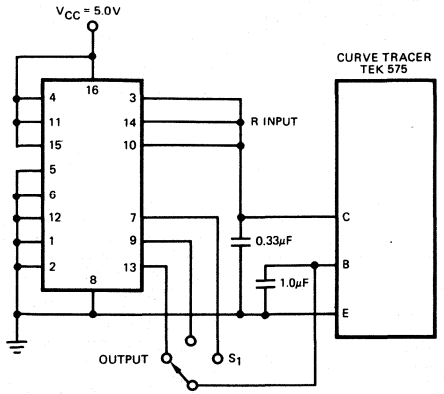
INPUT PULSE
Amplitude = 2.6 V
t_{PW} = 200 ns (50% Duty Cycle)
$t_r = t_f \leq 5$ ns (10% and 90% measurement points)

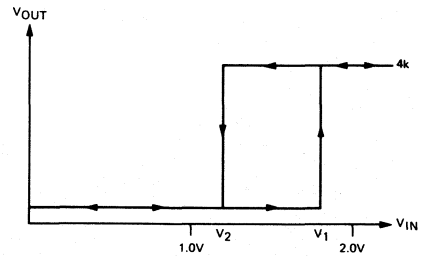
*Includes probe and jig capacitance.

VOLTAGE WAVEFORMS



HYSTERESIS TEST CIRCUIT

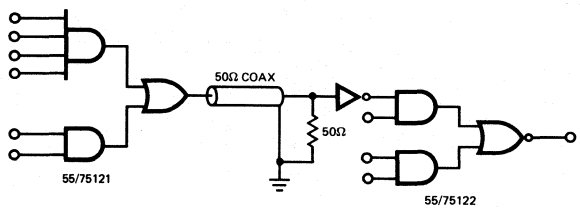


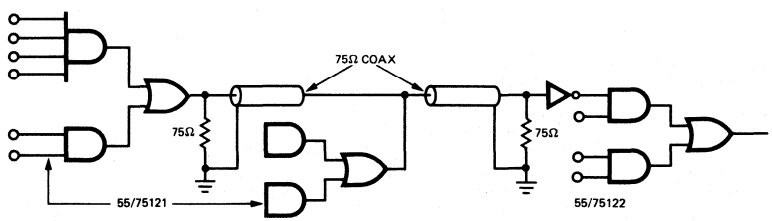


Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.8 V minimum and 2.0 V maximum.
2. Hysteresis = $V_1 - V_2 \geq 0.3$ V.

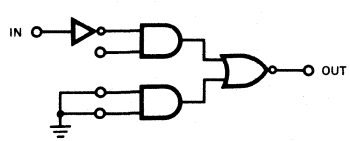
APPLICATIONS

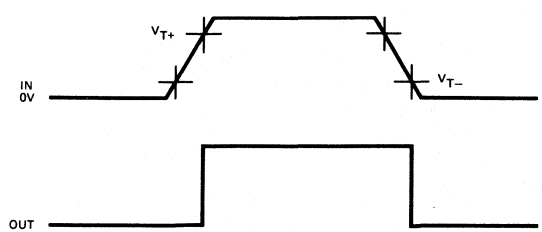




If more than one driver/receiver pair is to be used on each transmission line, the line should be terminated at both ends.

SCHMITT TRIGGER APPLICATION





55/75207•55/75208

DUAL MOS SENSE AMPLIFIERS

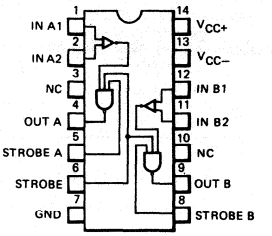
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55/75207 and 55/75208 are high speed, 2-channel sense amplifiers, electrically specified to replace the 55/75107 and 55/75108 in MOS memory systems. The tighter input threshold voltage (±10 mV vs ±25 mV for 55/75107 and 55/75108) can result in faster memory cycle times in the high performance MOS memory systems. Improved input threshold voltage makes them ideal in line reciever applications for recieving data over long transmission lines. The 55/75207 features a TTL compatible active pull up output. The 55/75208 features an open collector output configuration that permits wired-AND (collector dot) connections. The 55/75207 and 55/75208 are direct replacements for the 55/75107 and 55/75108 respectively.

- **±10 mV MAXIMUM INPUT SENSITIVITY**
- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **INPUT COMMON MODE VOLTAGE RANGE OF ±3.0 V**
- **SEPARATE OR COMMON STROBES**
- **TTL OR DTL DRIVE CAPABILITY**
- **WIRED-AND OUTPUT CAPABILITY (55/75208 ONLY)**
- **HIGH DC NOISE MARGINS**
- **STROBE INPUT CLAMP DIODES**

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)

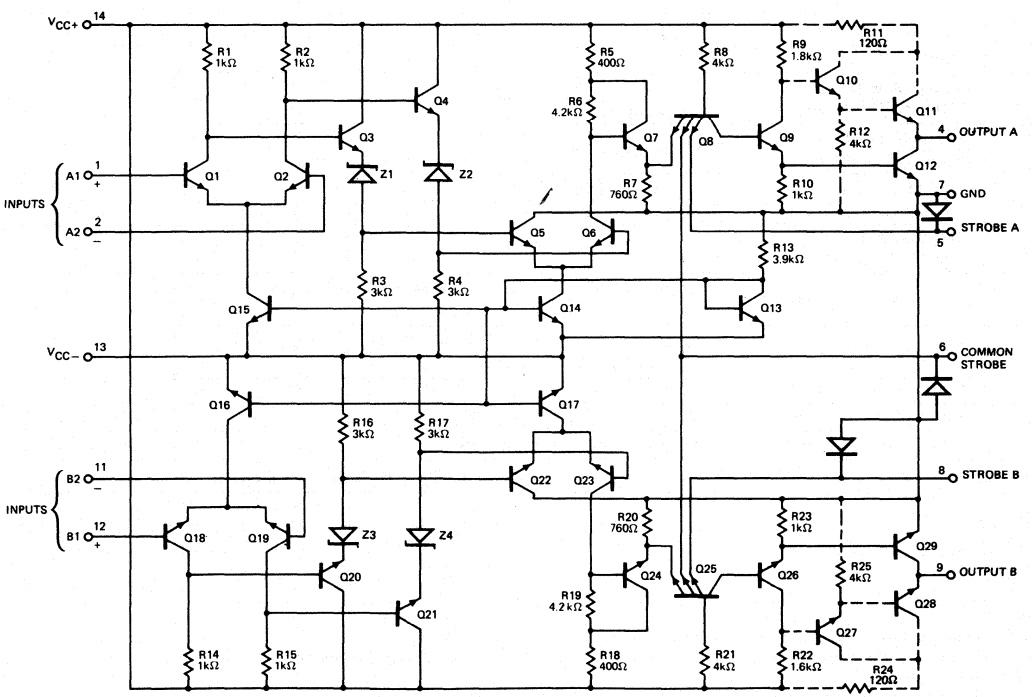
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.	TYPE	PART NO.
55207	55207FM	55208	55208FM
55207	55207DM	55208	55208DM
75207	75207DC	75208	75208DC
75207	75207PC	75208	75208PC

EQUIVALENT CIRCUIT



NOTE: Components shown with dashed lines are applicable to the 55/75207 only.

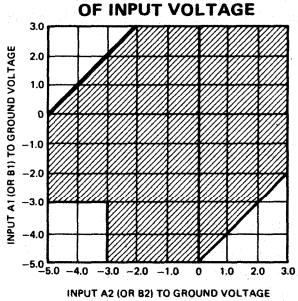
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	±7.0 V
Internal Power Dissipation (Note 2)	670 mW
Differential Input Voltage (Note 3)	±6.0 V
Common Mode Input Voltage (Note 1)	±5.0 V
Strobe Input Voltage (Note 1)	5.5 V
Operating Temperature Range	0°C to +70°C
55207/208	−55°C to +125°C
75207/208	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

TRUTH TABLE

DIFFERENTIAL INPUTS A1-A2 (or B1-B2)	STROBES A (or B)	STROBES (Common)	OUTPUT A (or B)
$V_{ID} \geq 10$ mV	L or H	L or H	H
-10 mV $< V_{ID} < 10$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -10$ mV	L or H	L	H
	L	L or H	H
	H	H	L

RECOMMENDED COMBINATIONS OF INPUT VOLTAGE



55/75207

ELECTRICAL CHARACTERISTICS (V_{CC+} = +5.25 V; V_{CC-} = −5.25 V, Rating apply over full ambient temperature range, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	TEST FIGURE	MIN	TYP	MAX	UNITS
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3.0 V to +3.0 V	2		30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2.0 V, V_{CM} = −3.0 V, to +3.0 V	2			−10	μA
$I_{IH(S)}$	Strobe (A or B) Input HIGH Current	V_{STROBE} = 2.4 V	4			40	μA
		V_{STROBE} = V+	4			1.0	mA
$I_{IL(S)}$	Strobe (A or B) Input LOW Current	V_{STROBE} = 0.4 V	4			−1.6	mA
$I_{IH(CS)}$	Common Strobe Input HIGH Current	$V_{COM.\ STROBE}$ = 2.4 V	4			80	μA
		$V_{COM.\ STROBE}$ = V+	4			2.0	mA
$I_{IL(CS)}$	Common Strobe Input LOW Current	$V_{COM.\ STROBE}$ = 0.4 V	4			−3.2	mA
V_{OH}	Output HIGH Voltage	I_{IL} = −400 μA, V_{CM} = −3.0 V to +3.0 V, V+ = +4.75 V; V− = −4.75 V	3	2.4			V
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3.0 V to +3.0 V, V+ = +4.75 V; V− = −4.75 V	3			0.4	V
I_{OS}	Short-Circuit Output Current	V_{OUT} = 0 (Note 4)	5	−18		−70	mA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C	6		18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C	6		−8.4	−15	mA

AC CHARACTERISTICS (V+ = +5.0 V, V− = −5.0 V, R_L = 470 Ω, C_L = 15 pF, T_A = 25°C, See Test Circuit)

$t_{PLH(D)}$	Propagation Delay Time	7		17	35	ns
$t_{PHL(D)}$		7		17	20	ns
$t_{PLH(S)}$		7		10	17	ns
$t_{PHL(S)}$		7		10	17	ns

NOTES:
1. These voltages are with respect to network ground terminal.
2. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For Flatpak derate linearly at 7.1 mW/°C above 60°C.
3. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
4. Not more than one (1) output should be shorted at a time.

55/75208

ELECTRICAL CHARACTERISTICS (V_{CC+} = +5.25 V; V_{CC-} = −5.25 V, Rating apply over full ambient temperature range, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	TEST FIGURE	MIN	TYP	MAX	UNITS
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3.0 V to +3.0 V	2		30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2.0 V, V_{CM} = −3.0 V to +3.0 V	2			−10	μA
$I_{IH(S)}$	Strobe (A or B) Input HIGH Current	V_{STROBE} = 2.4 V,	4			40	μA
		V_{STROBE} = V_{CC+}	4			1.0	mA
$I_{IL(S)}$	Strobe (A or B) Input LOW Current	V_{STROBE} = 0.4 V	4			−1.6	mA
$I_{IH(CS)}$	Common Strobe Input HIGH Current	$V_{COM. STROBE}$ = 2.4 V	4			80	μA
		$V_{COM. STROBE}$ = V+	4			2.0	mA
$I_{IL(CS)}$	Common Strobe Input LOW Current	$V_{COM. STROBE}$ = 0.4 V	4			−3.2	mA
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3.0 V to +3.0 V, V_{CC+} = +4.75 V; V_{CC-} = −4.75 V	3			0.4	V
I_{OH}	Output HIGH Current	V_{OUT} = V+, V_{CM} = −3.0 V to +3.0 V, V_{CC+} = 4.75 V; V_{CC-} = −4.75 V	3			250	μA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C	6		18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C	6		−8.4	−15	mA

AC CHARACTERISTICS (V_{CC+} = +5.0 V, V_{CC-} = −5.0 V, R_L = 470 Ω, C_L = 15 pF, T_A = 25°C, See Test Circuit)

$t_{PLH(D)}$	Propagation Delay Time	7		19	35	ns
$t_{PHL(D)}$		7		19	20	ns
$t_{PLH(S)}$		7		13	17	ns
$t_{PHL(S)}$		7		13	17	ns

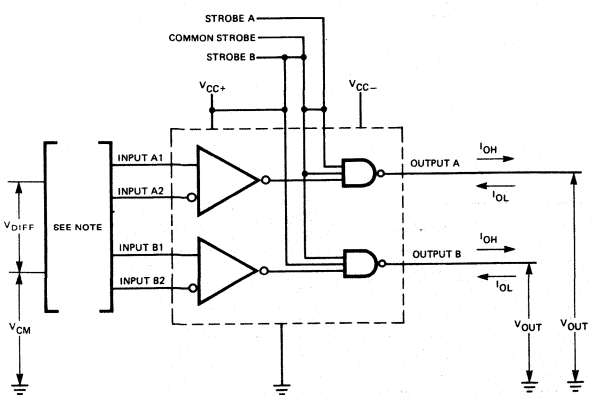
INPUT LOGIC LEVEL DEFINITION

SYMBOL	PARAMETER	TEST FIGURE	MIN	MAX	UNITS
V_{IDH}	High Level Input Voltage Between Differential Inputs	1	0.01	5.0	V
V_{IDL}	Low Level Input Voltage Between Differential Inputs	1	−5.0	−0.01	V
$V_{IH(S)}$	High Level Input Voltage at Strobe Inputs	3	2.0	5.5	V
$V_{IL(S)}$	Low Level Input Voltage at Strobe Inputs	3	0	0.8	V

11

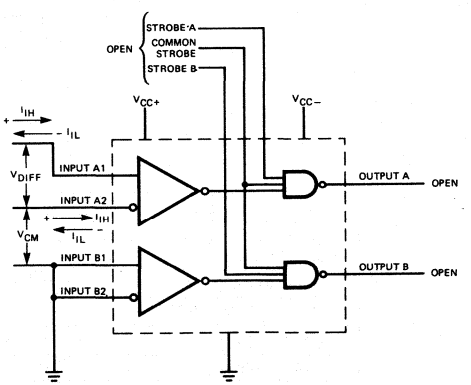
DC TEST CIRCUIT†

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.



NOTE:
When testing one channel, the inputs of the other channel are grounded.

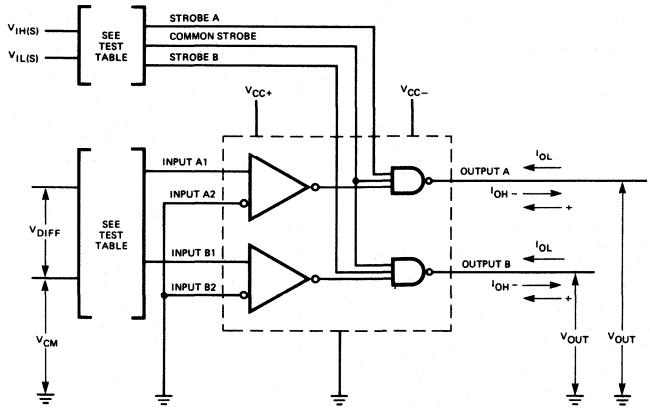
Fig. 1 – V_{IDH} and V_{IDL}



NOTE:
Each pair of differential inputs is tested separately. The other pair of inputs are grounded.

Fig. 2 – I_{IH} and I_{IL}

DC TEST CIRCUITS (Cont'd)†



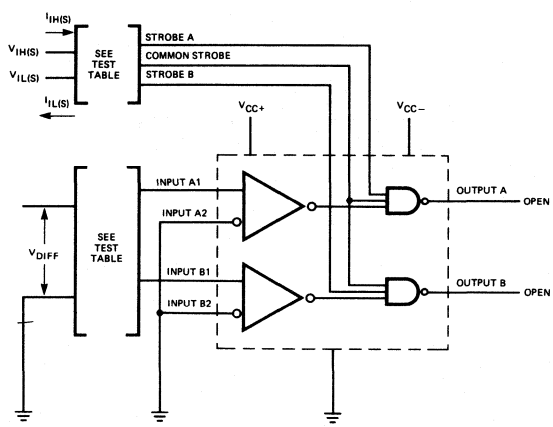
TEST TABLE

55/75207	55/75208	V_{DIFF}	STROBE A OR B	COMMON STROBE
TEST		APPLY		
V_{OH}	I_{OH}	+10 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	−10 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{OH}	−10 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	−10 mV	$V_{IH(S)}$	$V_{IH(S)}$

NOTES:
1. V_{CM} = −3.0 V to +3.0 V
2. When testing one channel, the inputs of the other channel should be grounded.

Fig. 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, I_{OH}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

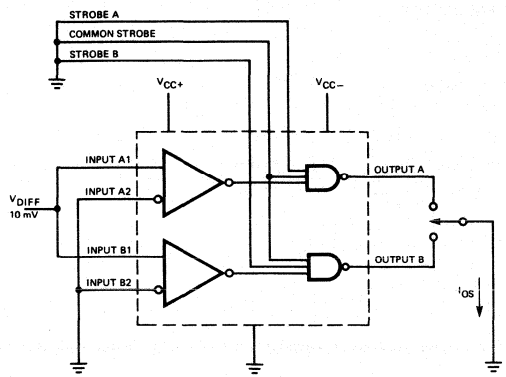


TEST	INPUT A1	INPUT B1	STROBE A	COMMON STROBE	STROBE B
I_{IH} at Strobe A	+10 mV	GND	$V_{IH(S)}$	GND	GND
I_{IH} at Strobe B	GND	+10 mV	GND	GND	$V_{IH(S)}$
I_{IH} at Common Strobe	+10 mV	+10 mV	GND	$V_{IH(S)}$	GND
I_{IL} at Strobe A	−10 mV	GND	$V_{IL(S)}$	4.5 V	GND
I_{IL} at Strobe B	GND	−10 mV	GND	4.5 V	$V_{IL(S)}$
I_{IL} at Common Strobe	−10 mV	−10 mV	4.5 V	$V_{IL(S)}$	4.5 V

Fig. 4 – $I_{IH(S)}$, $I_{IL(S)}$, $I_{IH(CS)}$, $I_{IL(CS)}$

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

DC TEST CIRCUITS (Cont'd)†



NOTES:
1. Each channel is tested separately.
2. Not more than one output should be grounded at a time.

Fig. 5 – I_{OS}

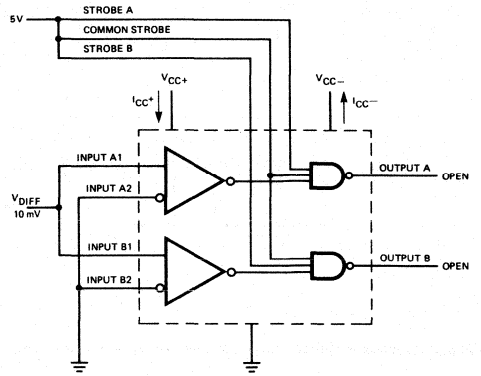
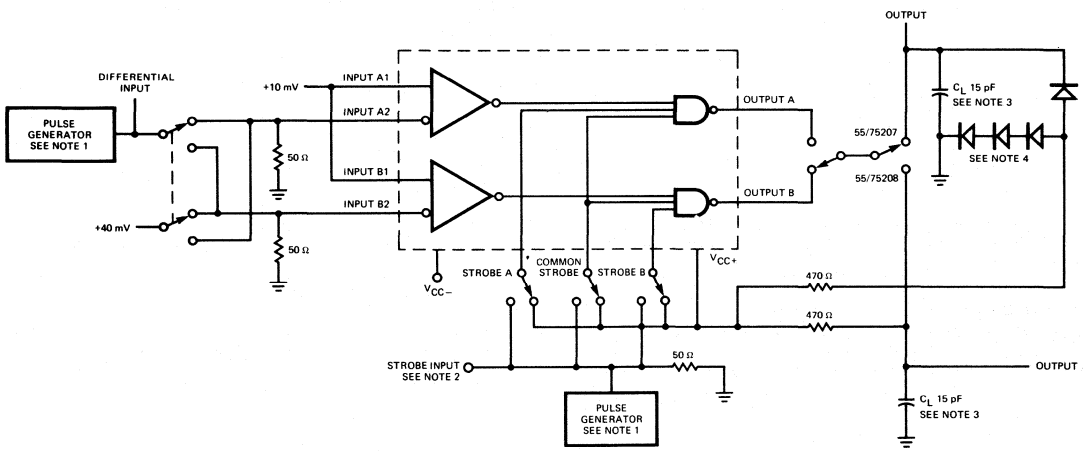


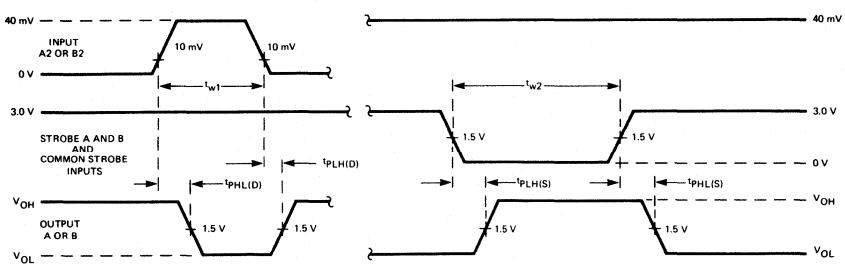
Fig. 6 – I_{CC+} and I_{CC-}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



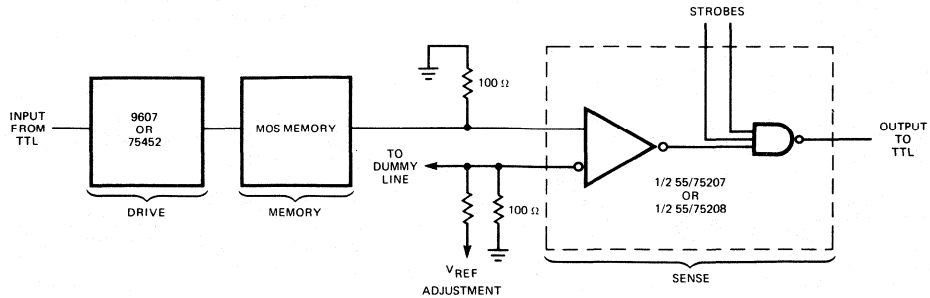
NOTES:
1. The pulse generators have the following characteristics: Z_{OUT} = 50 Ω, $t_r \leq 5$ ns, $t_f \leq 5$ ns, t_{w1} = 500 ns with PRR = 1 MHz, t_{w2} = 1 μs with PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe A when inputs A1 – A2 are being tested, to the Common Strobe when inputs A1 – A2 or B1 – B2 are being tested, and to Strobe B when inputs B1 – B2 are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

Fig. 7 – PROPAGATION DELAY TIMES

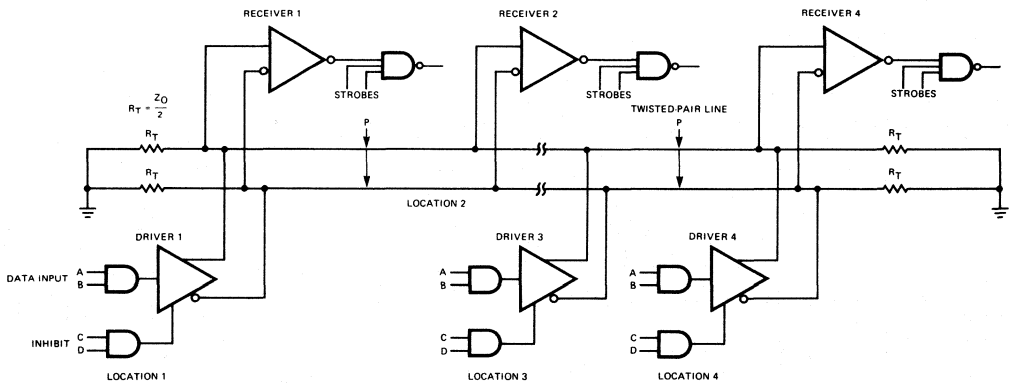
11

TYPICAL APPLICATIONS

MOS MEMORY SENSE AMPLIFIER



DATA-BUS PARTY-LINE SYSTEM



Receivers are 55207, 75207 or 55208, 75208; drivers are 55109, 75109, 55110 or 75110. For proper system operation, each receiver and driver on the bus should have its ground pin connected to a common lead (either shield or extra wire) to allow a common mode reference to be established.

PRECAUTIONS:
When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0 V and +3.0 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

55325•75325
MEMORY DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The 55325 and 75325 are Memory Drivers for use in magnetic memories constructed on a silicon chip using the Fairchild Planar* process. The device contains four 600 mA switches, two source switches and two sink switches that can be selected by the appropriate logic input and appropriate strobe. The device has adequate base drive to source currents up to 375 mA with V_{CC2} of 15 V or 600 mA with V_{CC2} voltage of 24 V. In applications requiring drive to source currents greater than 375 mA, an external resistor may be used to regulate the source base current to within ±5% and reduce the power dissipation to allow higher source currents at higher ambient temperatures.

Internal voltage surge protection of each of the output sink transistors is provided for switching inductive loads.

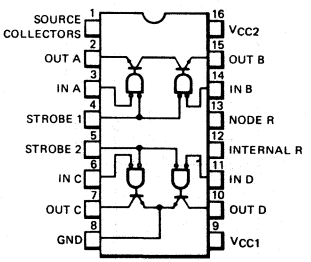
- **600 mA OUTPUT CAPABILITY**
- **FAST SWITCH TIMES**
- **OUTPUT SHORT- CIRCUIT CURRENT**
- **DUAL SINK AND DUAL SOURCE OUTPUTS**
- **MINIMUM TIME SKEW BETWEEN ADDRESS AND OUTPUT CURRENT RISE**
- **24 V CAPABILITY**
- **TTL OR DTL COMPATIBLE**
- **SOURCE BASE DRIVE EXTERNALLY ADJUSTABLE**
- **INPUT CLAMP DIODES**

POSITIVE LOGIC TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS (Note 3)			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
IN A	IN B	IN C	IN D	S1	S2	A	B	C	D
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = HIGH Level, L = LOW Level, X = Don't Care

CONNECTION DIAGRAMS
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 7B 9B 4L
PACKAGE CODES D P F



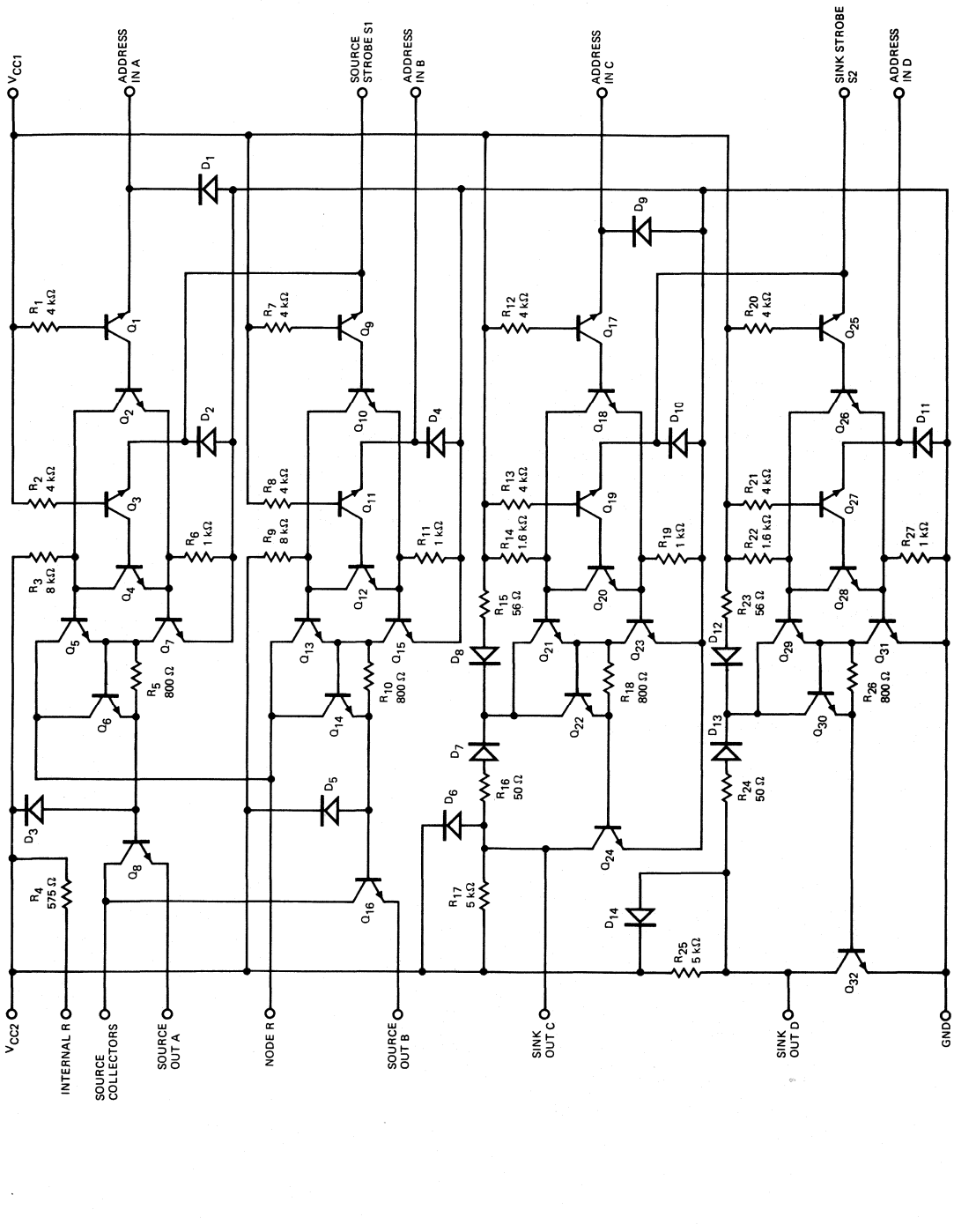
ORDER INFORMATION

TYPE	PART NO.
55325	55325DM
75325	75325DC
55325	55325FM
75325	75325PC

*Planar is a patented Fairchild process.

11

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC1} (Note 1)	+7.0 V
Supply Voltage V_{CC2} (Note 1)	+25 V
Input Voltage (Any Address or Strobe Input)	+5.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
55325	−55°C to +125°C
75325	0°C to +70°C
Internal Power Dissipation (Note 2)	1 W
Lead Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

55325

ELECTRICAL CHARACTERISTICS: Ratings apply for $-55°C \leq T_A \leq 125°C$, unless otherwise specified.

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		Fig. 1 & 2		2.0			V
V_{IL}	Input LOW Voltage		Fig. 3 & 4				0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{IN} = −10 mA, T_A = 25°C Fig. 5			−1.3	−1.7	V
I_{OFF}	Source-collectors Terminal Off-State Current		V_{CC1} = 4.5 V, V_{CC2} = 24 V Fig. 1	Full Range			500	µA
				T_A = 25°C		3.0	150	
V_{OH}	Sink Output HIGH Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{OUT} = 0, Fig. 2		19	23		V
V_{SAT}	Saturation Voltage	Source Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{source} \approx$ −600 mA See Notes 3 & 4, and Fig. 3	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
		Sink Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{sink} \approx$ 600 mA See Notes 3 & 4 and Fig. 4	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 5.5 V, Fig. 5				1.0	mA
		Strobe Inputs					2.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 2.4 V, Fig. 5			3.0	40	µA
		Strobe Inputs				6.0	80	
I_{IL}	Input LOW Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 0.4 V, Fig. 5			−1.0	−1.6	mA
		Strobe Inputs				−2.0	−3.2	
$I_{CC(off)}$	Supply Current, All Sources and Sinks Off	From V_{CC1}	V_{CC1} = 5.5 V, V_{CC2} = 24 V T_A = 25°C, Fig. 6			14	22	mA
		From V_{CC2}				7.5	20	
I_{CC1}	Supply Current from V_{CC1}, Either Sink On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{sink} = 50 mA, T_A = 25°C Fig. 7			55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{source} = −50 mA, T_A = 25°C Fig. 8			32	50	mA

NOTES:

1. Voltage values are with respect to network ground terminal.
2. Refer to Dissipation Derating Curve, Figure 13.
3. Not more than one output is to be on at any one time.
4. Parameters measured using the following pulse techniques; t_W = 200 µs, duty cycle ≤ 2%.

75325

ELECTRICAL CHARACTERISTICS: Rating apply for $0°C \leq T_A \leq 70°C$ unless otherwise specified.

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		Fig. 1 & 2		2.0			V
V_{IL}	Input LOW Voltage		Fig. 3 & 4				0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{IN} = −10 mA, T_A = 25°C Fig. 5			−1.3	−1.7	V
I_{OFF}	Source-collectors Terminal Off-State Current		V_{CC1} = 4.5 V, V_{CC2} = 24 V	Full Range			200	μA
			Fig. 1	T_A = 25°C		3.0	200	
V_{OH}	Sink Output HIGH Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{OUT} = 0, Fig. 2		19	23		V
V_{SAT}	Saturation Voltage	Source Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V	Full Range			0.9	V
			R_L = 24 Ω, $I_{source} \approx$ −600 mA See Notes 3 & 4, and Fig. 3	T_A = 25°C		0.43	0.75	
		Sink Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V	Full Range			0.9	V
			R_L = 24 Ω, $I_{sink} \approx$ 600 mA See Notes 3 & 4, and Fig. 4	T_A = 25°C			0.75	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V				1.0	mA
		Strobe Inputs	V_{IN} = 5.5 V, Fig. 5				2.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V			3.0	40	μA
		Strobe Inputs	V_{IN} = 2.4 V, Fig. 5			6.0	80	
I_{IL}	Input LOW Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V			−1.0	−1.6	mA
		Strobe Inputs	V_{IN} = 0.4 V, Fig. 5			−2.0	−3.2	
$I_{CC(off)}$	Supply Current, All Sources and Sinks Off	From V_{CC1}	V_{CC1} = 5.5 V, V_{CC2} = 24 V			14	22	mA
		From V_{CC2}	T_A = 25°C, Fig. 6			7.5	20	
I_{CC1}	Supply Current from V_{CC1}, Either Sink On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{sink} = 50 mA, T_A = 25°C Fig. 7			55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{source} = −50 mA, T_A = 25°C Fig. 8			32	50	mA

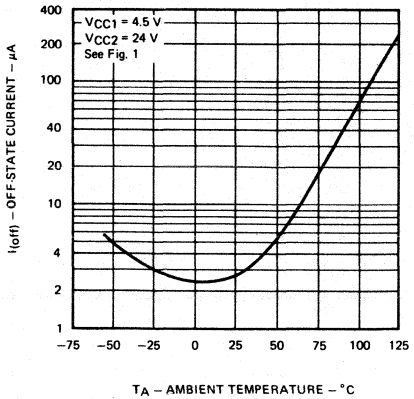
55325 • 75325

SWITCHING CHARACTERISTICS: V_{CC1} = 5.0 V, T_A = 25°C (See Test Circuit Figures 9 and 10)

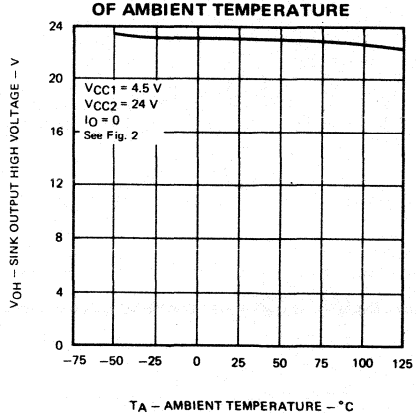
SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time to Source Collectors	9	V_{CC2} = 15 V, R_L = 24 Ω		25	50	ns
t_{PHL}			C_L = 25 pF		25	50	
t_{TLH}	Transition Time to Source Outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ		55		ns
t_{THL}			C_L = 25 pF		7.0		
t_{PLH}	Propagation Delay Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω		20	45	ns
t_{PHL}			C_L = 25 pF		20	45	
t_{TLH}	Transition Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω		7.0	15	ns
t_{THL}			C_L = 25 pF		9.0	20	
t_s	Storage Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		15	30	ns

TYPICAL PERFORMANCE CURVES

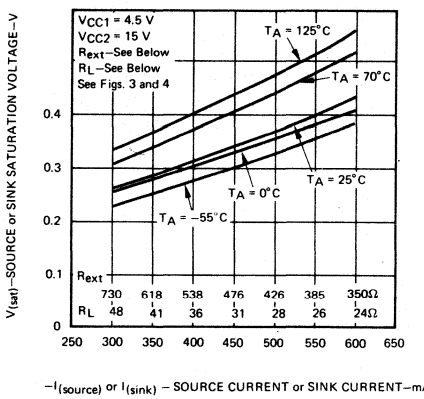
OFF-STATE CURRENT INTO SOURCE COLLECTORS AS A FUNCTION OF AMBIENT TEMPERATURE



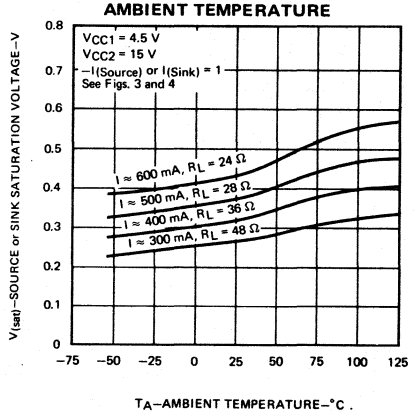
SINK OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



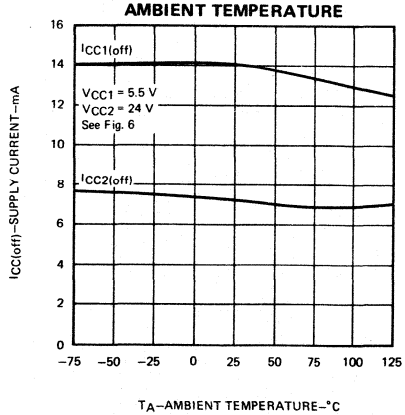
SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF SOURCE CURRENT OR SINK CURRENT



SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



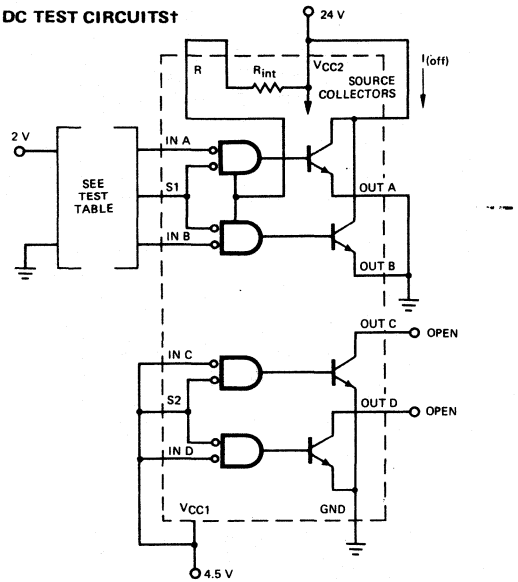
SUPPLY CURRENT, ALL SOURCES AND SINKS OFF AS A FUNCTION OF AMBIENT TEMPERATURE



11

PARAMETER MEASUREMENT INFORMATION

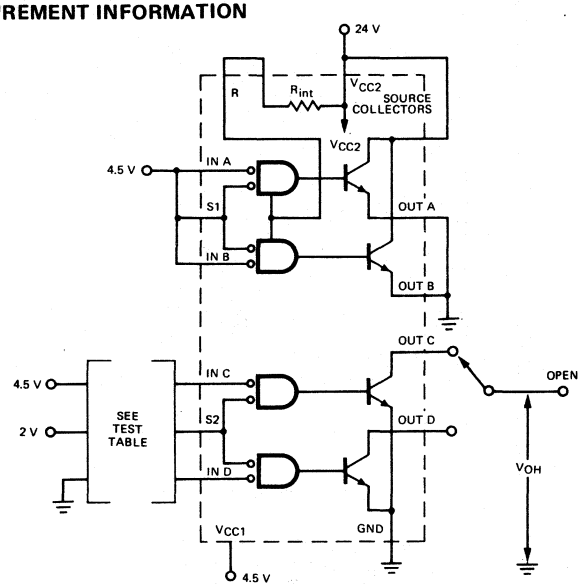
DC TEST CIRCUITS†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

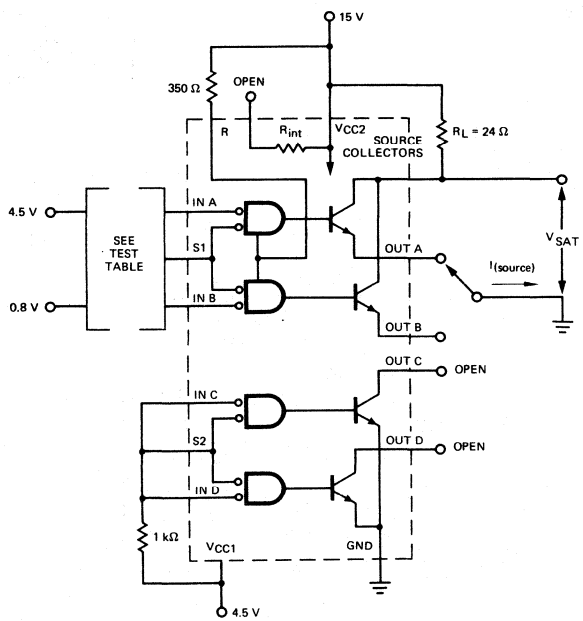
Fig. 1 $I_{(OFF)}$ AND V_{IH}



TEST TABLE

C	D	S2	OUT C	OUT D
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

Fig. 2 V_{IH} AND V_{OH}



TEST TABLE

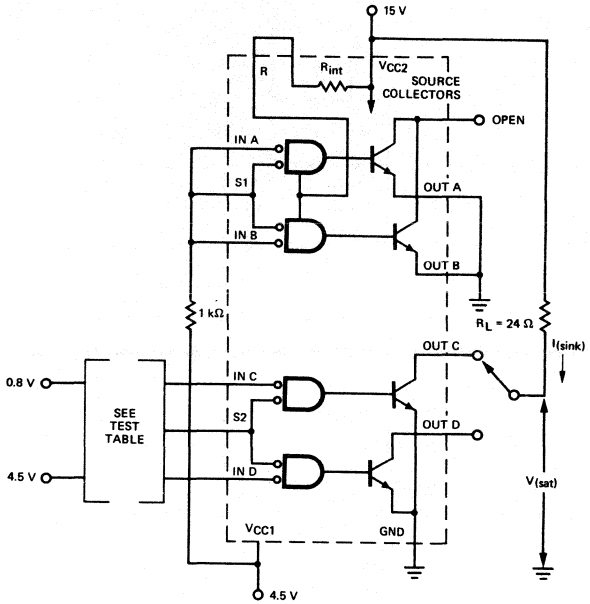
A	B	S1	OUT A	OUT B
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

Fig. 3 V_{IL} AND SOURCE $V_{(sat)}$ (Note 4)

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

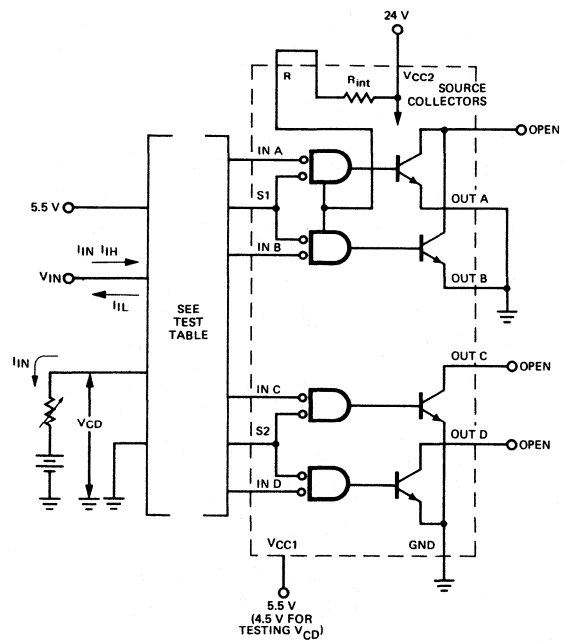
DC TEST CIRCUITS (Cont'd)



TEST TABLE

C	D	S2	OUT C	OUT D
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

Fig. 4 V_{IL} AND SINK $V_{(sat)}$ (Note 4)



TEST TABLES

I_I, I_{IH}

APPLY V_{IN} = 5.5 V, MEASURE I_{IN} / APPLY V_{IN} = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1; B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_{IN} = 0.4 V, MEASURE I_{IL} / APPLY I_{IN} = −10 mA MEASURE V_{CD}	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

Fig. 5 V_{CD}, I_{IN}, I_{IH}, AND I_{IL}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS (Cont'd)

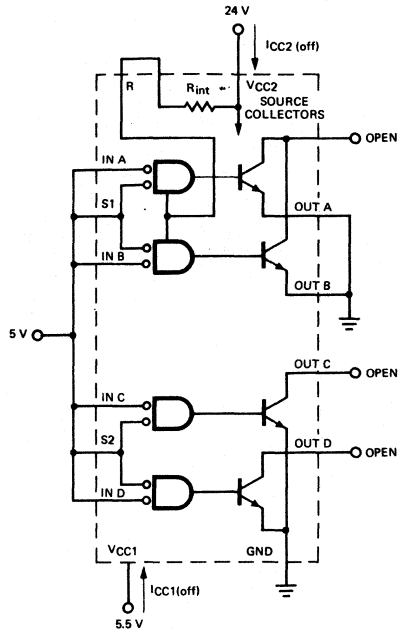
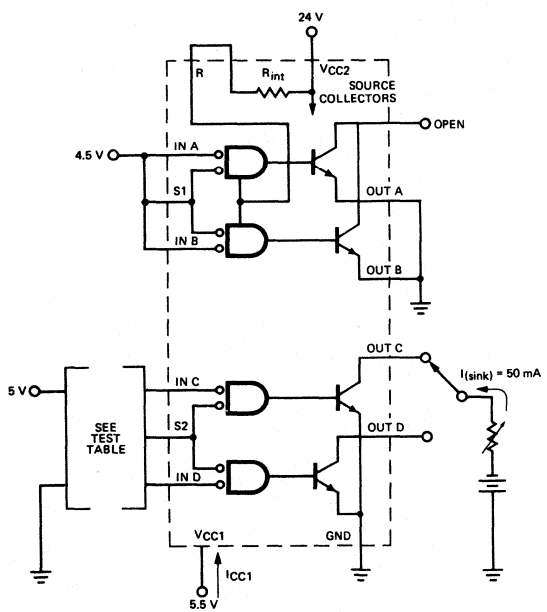


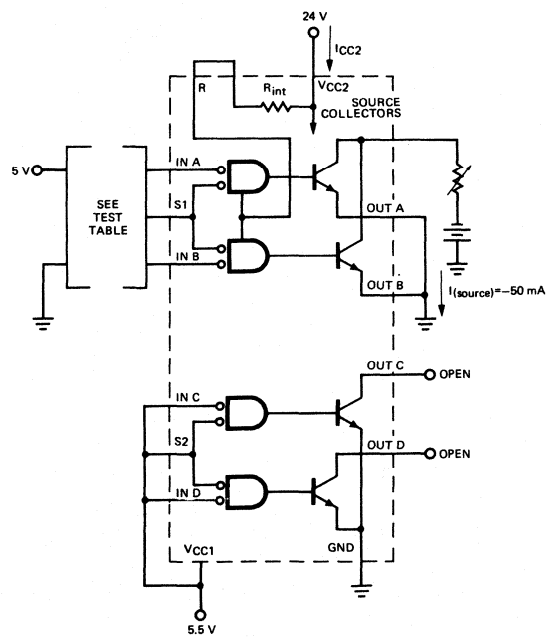
Fig. 6 $I_{CC1(OFF)}$ AND $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	OUT C	OUT D
GND	5 V	GND	$I_{(sink)}$	OPEN
5 V	GND	GND	OPEN	$I_{(sink)}$

Fig. 7 I_{CC1}, EITHER SINK ON



TEST TABLE

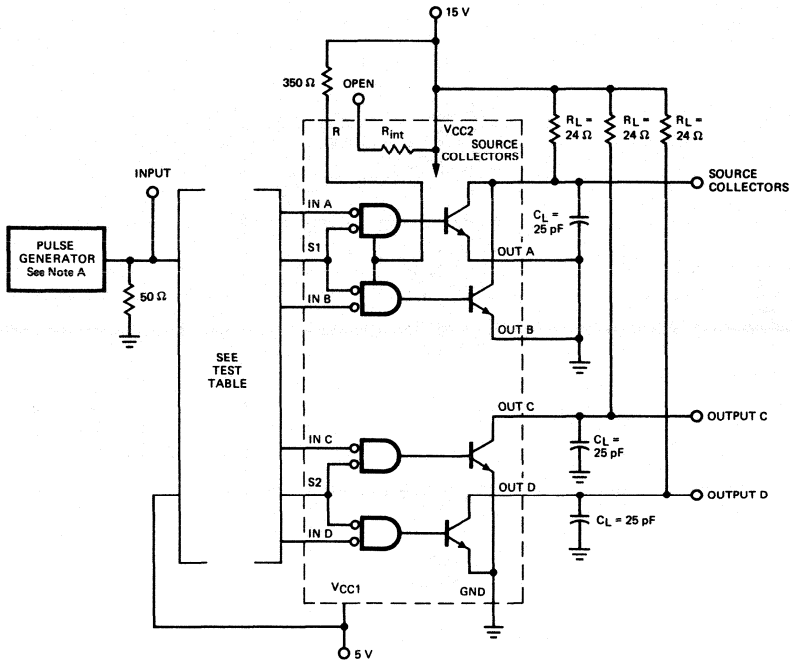
A	B	S1
GND	5 V	GND
5 V	GND	GND

Fig. 8 I_{CC2}, EITHER SOURCE ON

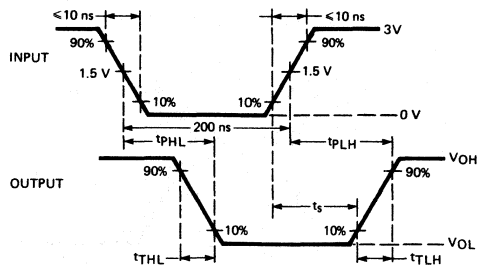
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



VOLTAGE WAVEFORMS



TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink Output C	C and S2	A, B, D and S1
	Sink Output D	D and S2	A, B, C and S1

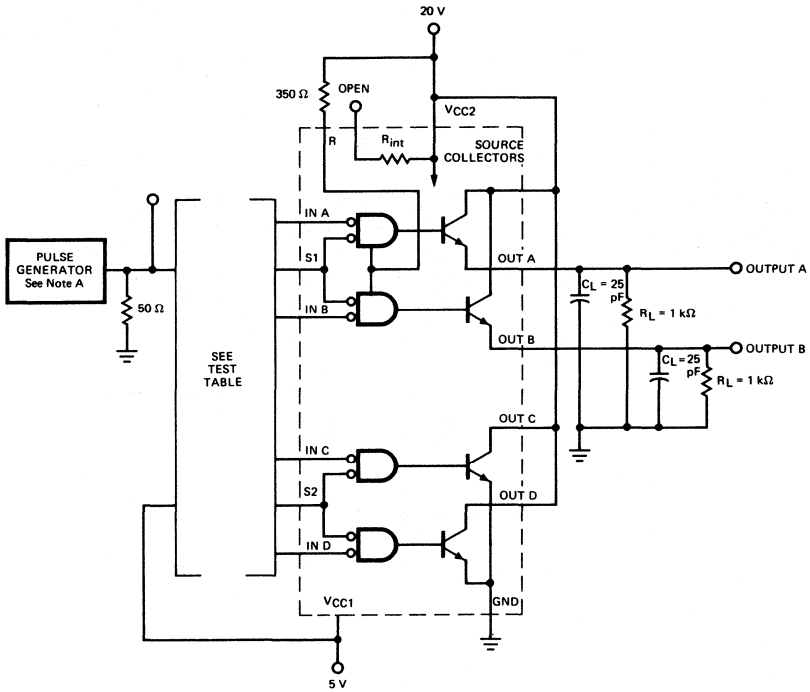
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%. (f ≤ 50 kHz).
B. C_L includes probe and jig capacitance.

Fig. 9 SWITCHING TIMES

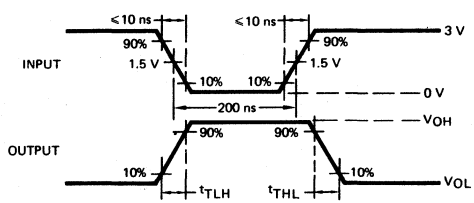
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Cont'd)



VOLTAGE WAVEFORMS



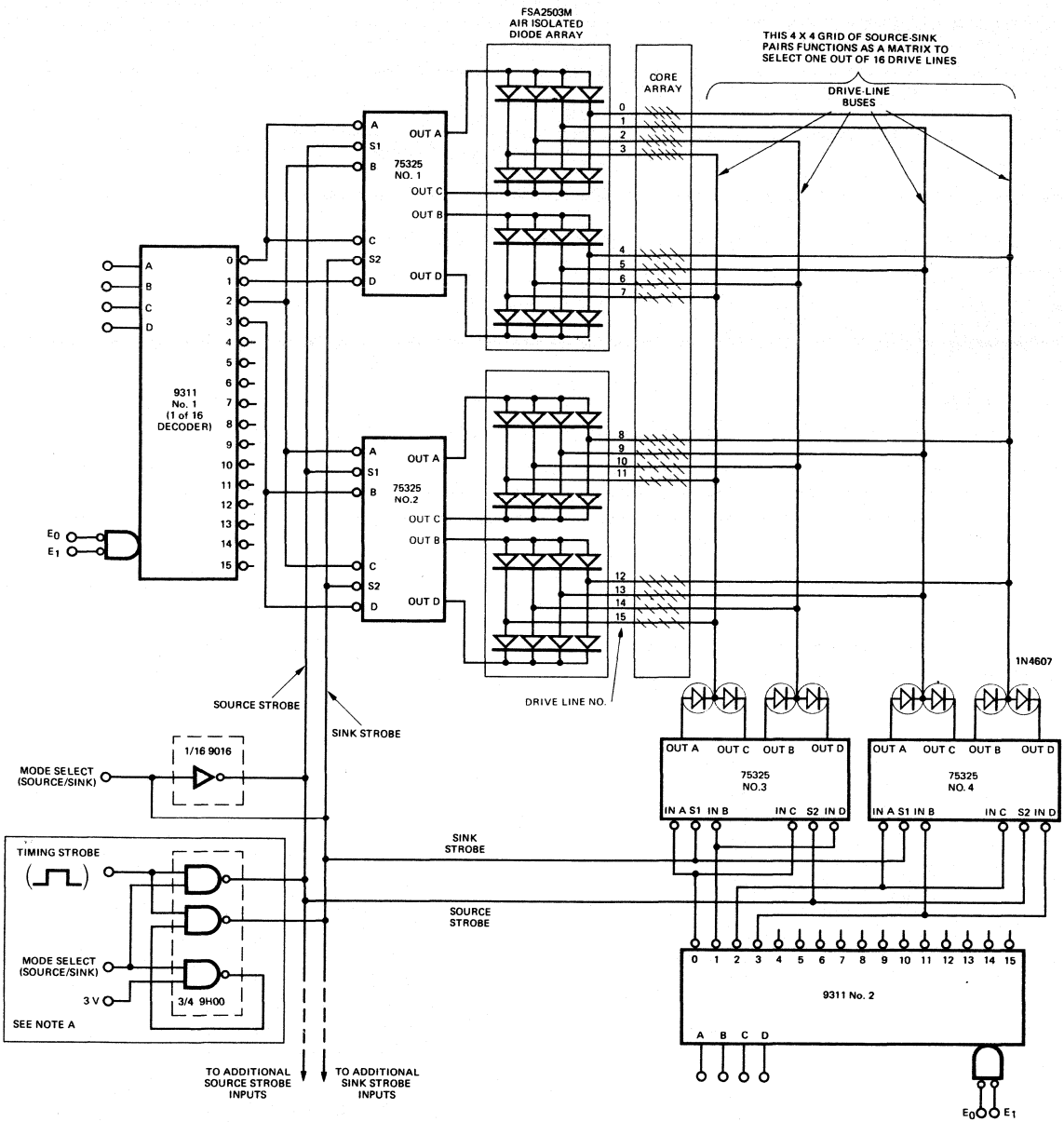
TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source Output A	A and S1	B, C, D, and S2
	Source Output B	B and S1	A, C, D, and S2

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%. (f ≤ 50 kHz)
B. C_L includes probe and jig capacitance.

Fig. 10 TRANSITION TIMES OF SOURCE OUTPUTS

APPLICATIONS



In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 11. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, 9311 No. 1 must be set to 3 (with mode select HIGH), enabling source B of 75325 No. 2 to drive lines 12 through 15, and 9311 No. 2 must be set to 2, providing a sink at C of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from HIGH to LOW. The size of such a matrix is limited only by the number of drive-lines that a source sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver.

NOTE A: This optional mode-select and timing-strobe technique can be used in place of the 9N40 mode-select and 9311 timing-strobe when minimum time skew is desired.

Fig. 11 75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

APPLICATIONS (Cont'd)

EXTERNAL RESISTOR CALCULATION – A typical magnetic-memory word drive requirement is shown in Figure 12. A source-output transistor of one 75325 delivers load current (I_L). The sink-output transistor of another 75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad \text{where: } P_{Rext} \text{ is in mW.} \quad \text{(Equation 2)}$$

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\, I_L \quad \text{where: } I_{CS} \text{ is in mA.} \quad \text{(Equation 3)}$$

As an example, let $V_{CC2(min)} = 20$ V and $V_L = 3$ V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

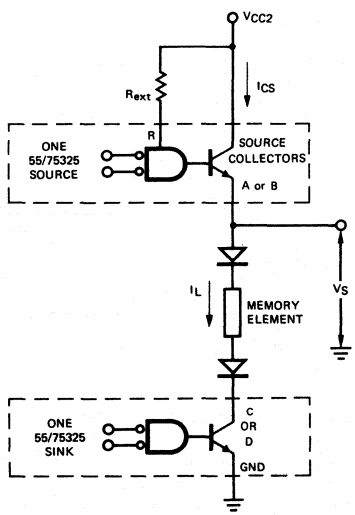
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

EXTERNAL RESISTOR CALCULATION (Cont'd)



NOTES: A. For clarity, partial logic diagrams of two 75325's are shown.
B. Source and sink shown are in different packages.

Fig. 12

THERMAL INFORMATION

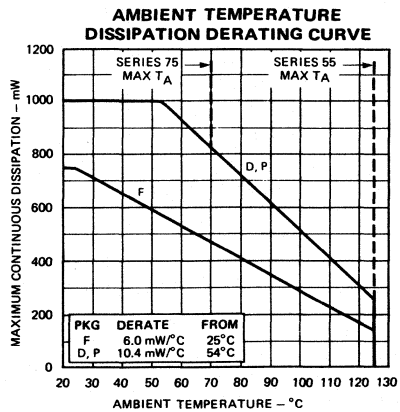


Fig. 13

55/75450A • 55/75451A • 55/75452A
55/75453A • 55/75454A
DUAL PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55/75450A, 55/75451A, 55/75452A, 55/75453A and 55/75454A are Dual High Speed General Purpose Interface Drivers that convert TTL and DTL logic levels to high current drive capability. The 55450A and 75450A feature two TTL NAND gates and two uncommitted transistors. The 55/75451A, 55/75452A, 55/75453A and 55/75454A feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The 55/75450A series offers flexibility in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **NO LATCH-UP AT 20 V**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

TEST TABLE 1 – Operating Temperature Range and Supply Voltage Range

	55450A Series	75450A Series
Temperature, T_A	–55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

11

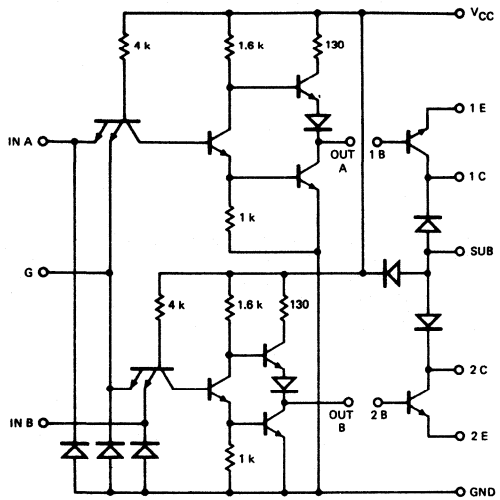
ABSOLUTE MAXIMUM RATINGS

	55450A	75450A	55451A 55452A 55453A 55454A	75451A 75452A 75453A 75454A
Supply Voltage, V_{CC} (See Note 1)	7 V	7 V	7 V	7 V
Input Voltage (See Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage(See Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Base Voltage	35 V	35 V		
Collector to Emitter Voltage (See Note 3)	30 V	30 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (See Notes 1 and 4)			30 V	30 V
Continuous Collector Current (See Note 5)	300 mA	300 mA		
Continuous Output Current (See Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (See Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Free-Air Temperature Range	–55°C to +125°C	0°C to 70°C	–55°C to +125°C	0°C to 70°C
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C
Lead Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP, Flatpak and Metal Can (Soldering, 60 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 55450A and 75450A only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Flatpak, derate at 7.1 mW/°C above 40°C. For the Molded Mini DIP and Ceramic Mini DIP, derate at 6.7 mW/°C above 30°C. For the Metal Can, derate at 6.3 mW/°C above 20°C. The rating for Metal Can requires a heat sink that provides a thermal resistance from case to free air ($R_{\theta CA}$) of not more than 95°C/W.

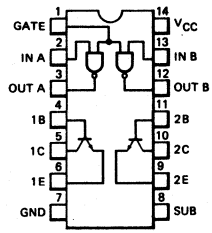
55450A/75450A
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-LEAD
(TOP VIEW)
PACKAGE OUTLINE 6A 9A 3I
PACKAGE CODE D P F



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = XY$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55450A	55450ADM
55450A	55450AFM
75450A	75450ADC
75450A	75450APC

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

TTL Gates

SYMBOL	PARAMETER		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNIT
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = −400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V I_{OL} = 16 mA	55450A		0.22	0.5	V
					75450A		0.22	0.4	
I_I	Input Current at Maximum Input Voltage	Input A	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Input G						2	
I_{IH}	Input HIGH Current	Input A	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Input G						80	
I_{IL}	Input LOW Current	Input A	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Input G						−3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			6	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55450A/75450A

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

Output Transistors

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP (Note 10)	MAX	UNIT
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55450A	10			
			75450A	20			
		V_{CE} = 3 V, I_C = 300 mA	55450A	15			
			75450A	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450A		0.85	1.2	V
			75450A		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55450A		1.05	1.4	V
			75450A		1.05	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450A		0.25	0.5	V
			75450A		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55450A		0.5	0.8	V
			75450A		0.5	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		12		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNIT
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		10		ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		14		ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		10		ns
t_f	Fall Time				11		ns

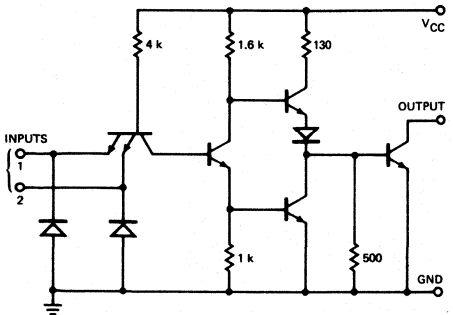
Gates and Transistors Combined

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		22	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				22	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				10	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				14	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, I_C ≈ 300 mA R_{BE} = 500 Ω	V_S −6.5			mV

NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

55451A/75451A
DUAL POSITIVE AND PERIPHERAL DRIVER

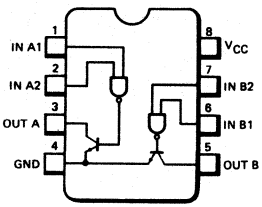
EQUIVALENT CIRCUIT (Each Driver)



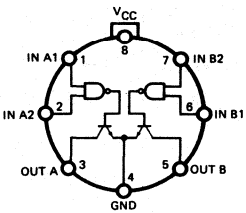
Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55451A	55451ARM
75451A	75451ARC
75451A	75451ATC

ORDER INFORMATION

TYPE	PART NO.
55451A	55451AHM
75451A	75451AHC

Positive Logic: $Z = XY$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55451A			300	μA
				75451A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55451A		0.25	0.5	V
				75451A		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55451A		0.5	0.8	
				75451A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			7.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			52	65	mA

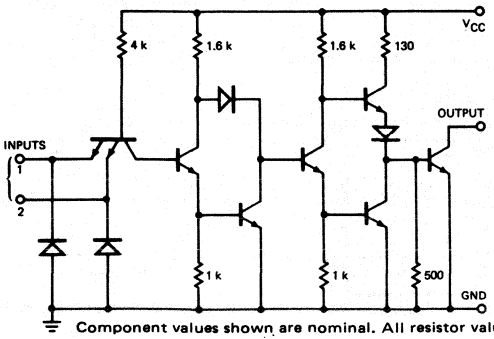
NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55452A/75452A
DUAL POSITIVE NAND PERIPHERAL DRIVER

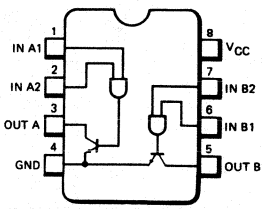
EQUIVALENT CIRCUIT (Each Driver)



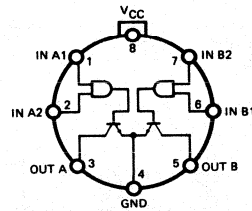
Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55452A	55452ARM
75452A	75452ARC
75452A	75452ATC

ORDER INFORMATION

TYPE	PART NO.
55452A	55452AHM
75452A	75452AHC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55452A			300	μA
				75452A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55452A		0.25	0.5	V
				75452A		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55452A		0.5	0.8	
				75452A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			11	14	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			56	71	mA

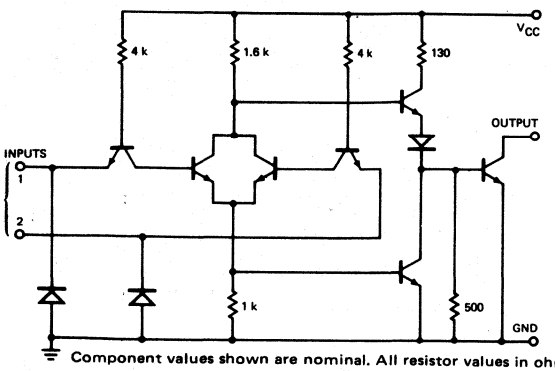
NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55453A/75453A
DUAL POSITIVE OR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

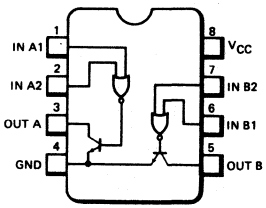
TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

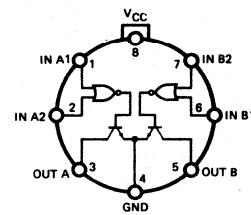
H = HIGH Level, L = LOW Level

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
55453A	55453ARM
75453A	75453ARC
75453A	75453ATC

ORDER INFORMATION

TYPE	PART NO.
55453A	55453AHM
75453A	75453AHC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55453A			300	µA
				75453A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55453A		0.25	0.5	V
				75453A		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55453A		0.5	0.8	
				75453A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			54	68	mA

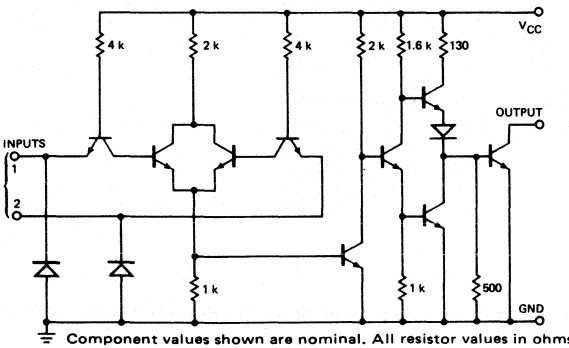
NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25 °C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55454A/75454A
DUAL POSITIVE NOR PERIPHERAL DRIVER

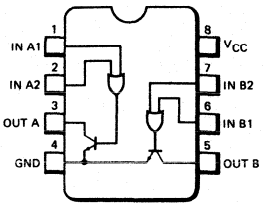
EQUIVALENT CIRCUIT (Each Driver)



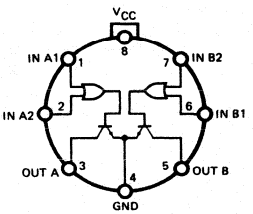
Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55454A	55454ARM
75454A	75454ARC
75454A	75454ATC

ORDER INFORMATION

TYPE	PART NO.
55454A	55454AHM
75454A	75454AHC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55454A			300	μA
				75454A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55454A		0.25	0.5	V
				75454A		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55454A		0.5	0.8	
				75454A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			61	79	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

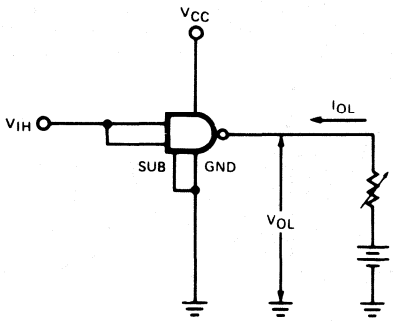
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT†

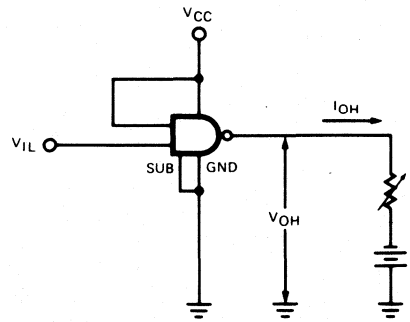
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

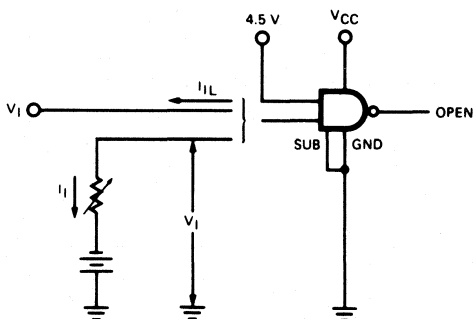
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

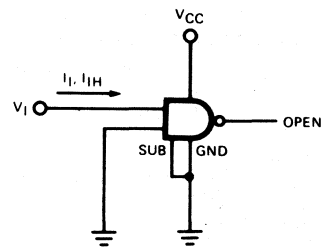
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

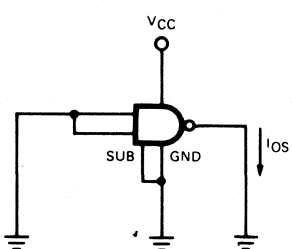
I_I, I_{IH}



Each input is tested separately

Fig. 4

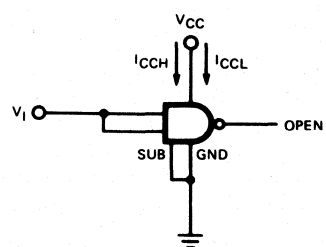
I_{OS}



Each gate is tested separately.
(55450A/75450A only)

Fig. 5

I_{CCH}, I_{CCL}

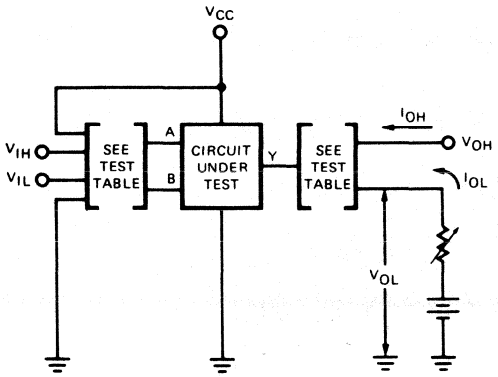


Both gates are tested simultaneously.

Fig. 6

PARAMETER MEASUREMENT INFORMATION

V_{IH}, V_{IL}, I_{OH}, V_{OL}



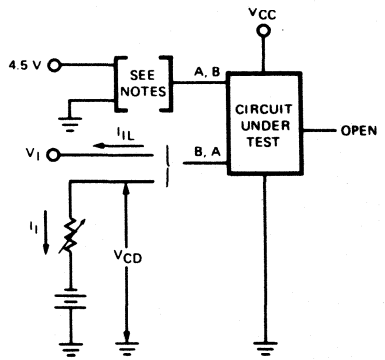
TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75451A	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
55/75452A	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
55/75453A	V_{IH}	GND	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
55/75454A	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

NOTE: Each input is tested separately.

Fig. 7

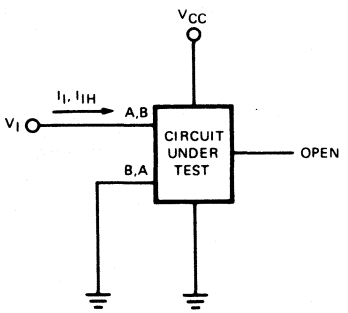
V_{CD}, I_{IL}



NOTES: A. Each input is tested separately.
B. When testing I_{IL} 55/75453A and 55/75454A, the input not under test is grounded. For all other circuits it is at 4.5 V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

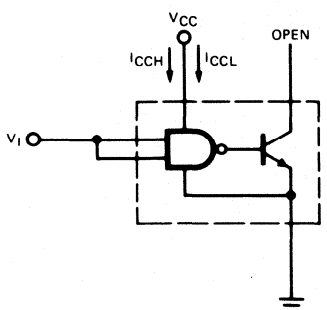
I_I, I_{IH}



Each input is tested separately.

Fig. 9

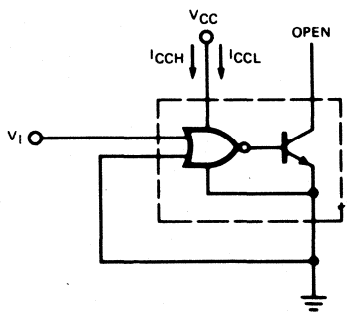
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

Fig. 11

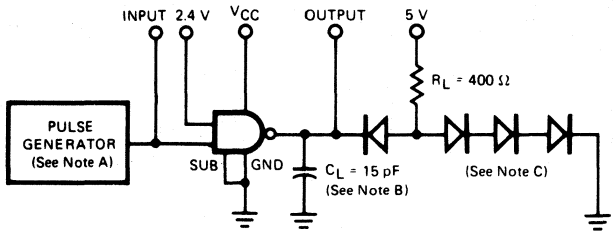
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

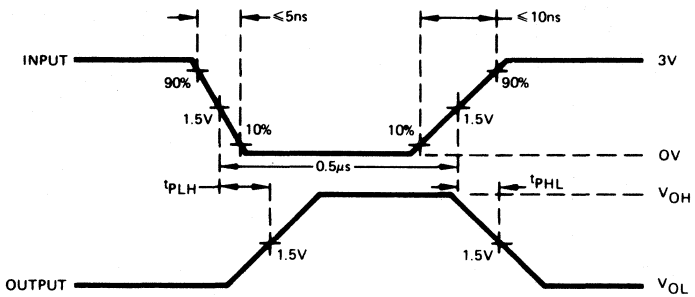
SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE
(55450A, 75450A ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are FD777.

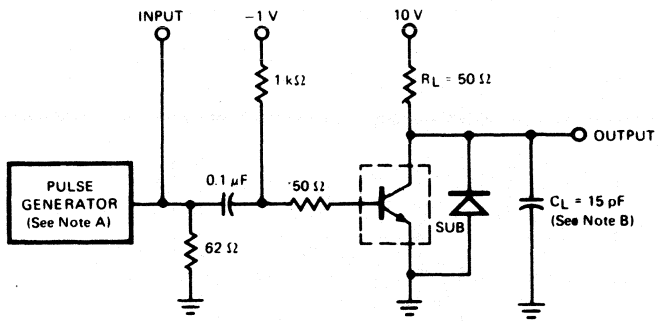
Fig. 12

PARAMETER MEASUREMENT INFORMATION

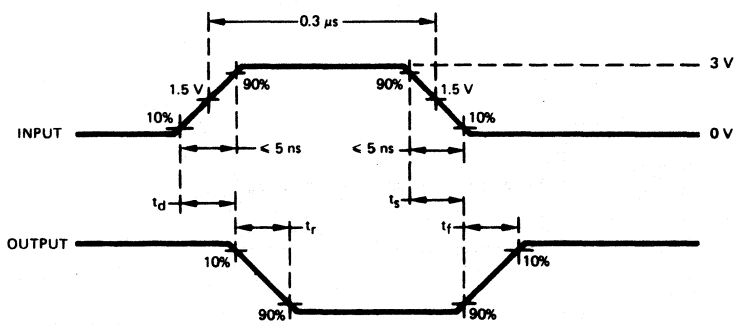
SWITCHING CHARACTERISTICS

SWITCHING TIMES, EACH TRANSISTOR
(55450A, 75450A ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

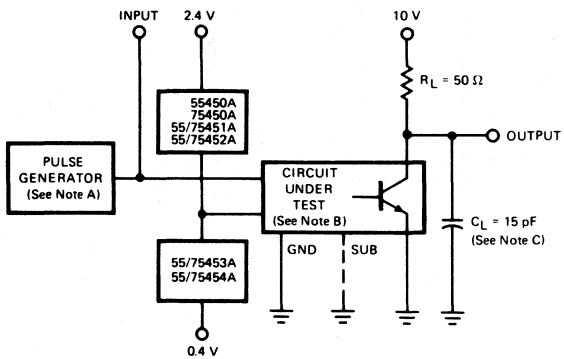
Fig. 13

PARAMETER MEASUREMENT INFORMATION

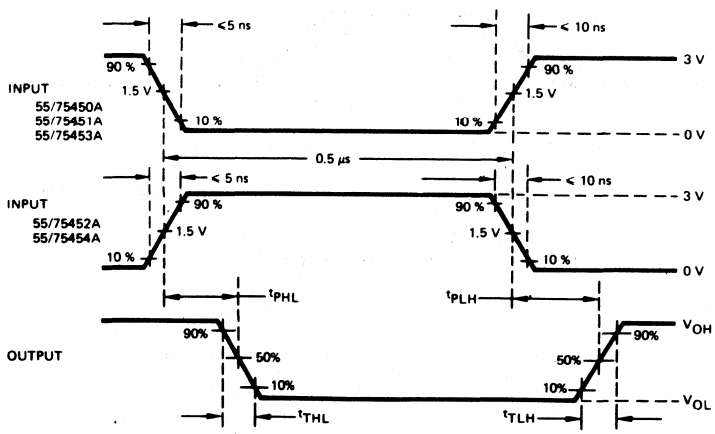
SWITCHING CHARACTERISTICS

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When Testing 55450A/75450A, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

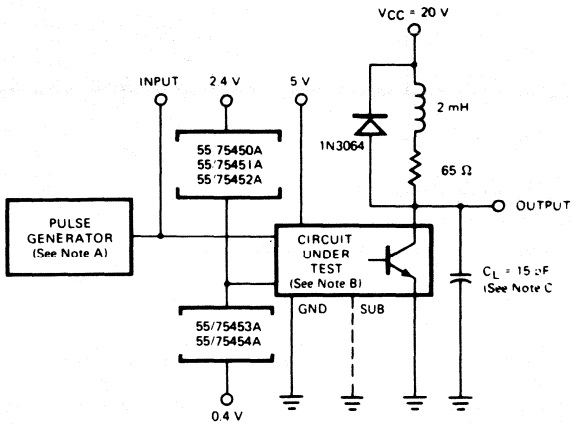
Fig. 14

PARAMETER MEASUREMENT INFORMATION

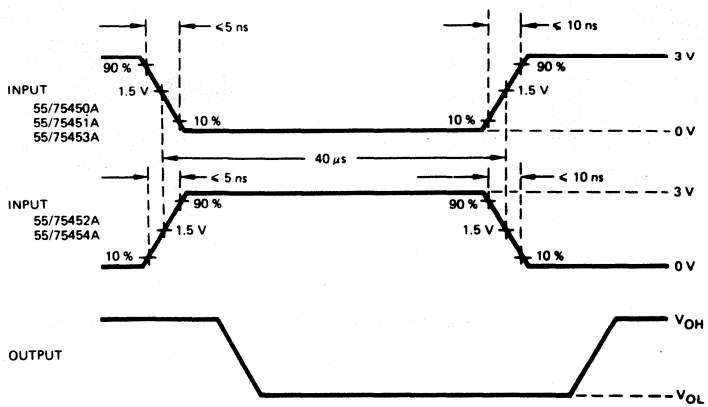
SWITCHING CHARACTERISTICS

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

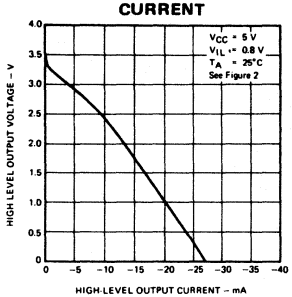


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55450A or 75450A, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

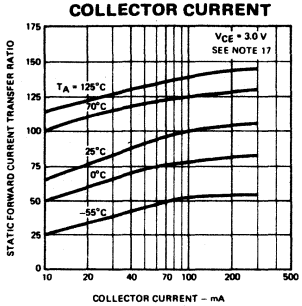
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 75450A SERIES

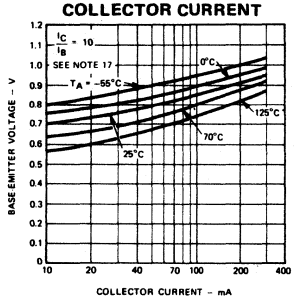
55450A/75450A TTL GATE HIGH-LEVEL OUTPUT VOLTAGE AS A FUNCTION OF HIGH-LEVEL OUTPUT CURRENT



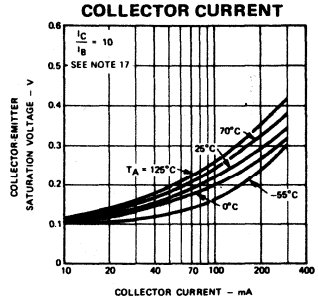
55450A/75450A TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55450A/75450A TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17: These parameters must be measured using pulse techniques. t_W = 300 μs, duty cycle ≤ 2%.

55/75450B • 55/75451B • 55/75452B
55/75453B • 55/75454B
DUAL HIGH SPEED PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55/75450B, 55/75451B, 55/75452B, 55/75453B and 55/75454B are Dual High Speed General Purpose Interface Drivers that convert TTL and DTL logic levels to high current drive capability. The 55450B and 75450B feature two TTL NAND gates and two uncommitted transistors. The 55/75451B, 55/75452B, 55/75453B and 55/75454B feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The 55/75450B series offers flexibility in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **NO LATCH-UP AT 20 V**
- **HIGH SPEED SWITCHING**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

TEST TABLE 1 – Operating Temperature Range and Supply Voltage Range

	55450B Series	75450B Series
Temperature, T_A	–55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

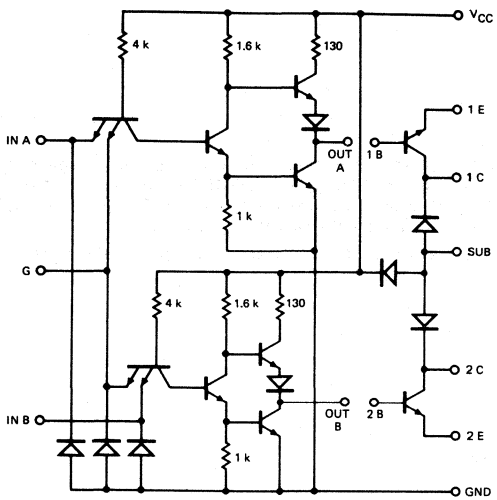
ABSOLUTE MAXIMUM RATINGS

	55450B	75450B	55451B 55452B 55453B 55454B	75451B 75452B 75453B 75454B
Supply Voltage, V_{CC} (See Note 1)	7 V	7 V	7 V	7 V
Input Voltage (See Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage (See Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Base Voltage	35 V	35 V		
Collector to Emitter Voltage (See Note 3)	30 V	30 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (See Notes 1 and 4)			30 V	30 V
Continuous Collector Current (See Note 5)	300 mA	300 mA		
Continuous Output Current (See Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (See Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Free-Air Temperature Range	–55°C to +125°C	0°C to 70°C	–55°C to +125°C	0°C to 70°C
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C
Lead Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP, Flatpak and Metal Can (Soldering, 60 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 55450B and 75450B only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Flatpak, derate at 7.1 mW/°C above 40°C. For the Molded Mini DIP and Hermetic Mini DIP, derate at 6.7 mW/°C above 30°C. For the Metal Can, derate at 6.3 mW/°C above 20°C. The rating for Metal Can requires a heat sink that provides a thermal resistance from case to free air ($R_{\theta CA}$) of not more than 95°C/W.

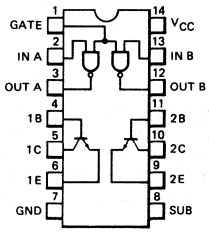
55450B/75450B
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-LEAD
(TOP VIEW)
PACKAGE OUTLINE 6A 9A 3I
PACKAGE CODE D P F



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = XY$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55450B	55450BDM
55450B	55450BFM
75450B	75450BDC
75450B	75450BPC

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

TTL Gates

SYMBOL	PARAMETER		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNIT
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = -12 mA				-1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = -400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V	55450B		0.22	0.5	V
				I_{OL} = 16 mA	75450B		0.22	0.4	
I_I	Input Current at Maximum Input Voltage	Input A	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Input G						2	
I_{IH}	Input HIGH Current	Input A	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Input G						80	
I_{IL}	Input LOW Current	Input A	3	V_{CC} = MAX, V_I = 0.4 V				-1.6	mA
		Input G						-3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		-18		-55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			6	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55450B/75450B

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

Output Transistors

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP (Note 10)	MAX	UNIT
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55450B	10			
			75450B	20			
		V_{CE} = 3 V, I_C = 300 mA	55450B	15			
			75450B	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450B		0.85	1.2	V
			75450B		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55450B		1.05	1.4	V
			75450B		1.05	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450B		0.25	0.5	V
			75450B		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55450B		0.5	0.8	V
			75450B		0.5	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		12	22	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8	15	ns

Output Transistors

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNIT
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		8	15	ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		12	20	ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		7	15	ns
t_f	Fall Time				6	15	ns

Gates and Transistors Combined

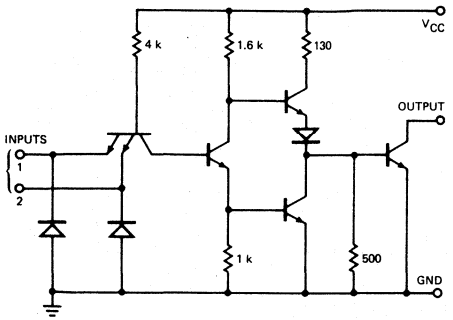
SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		20	30	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	30	ns
t_{TLH}	Transition Time, Output LOW to HIGH				7	12	ns
t_{THL}	Transition Time, Output HIGH to LOW				9	15	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, I_C ≈ 300 mA R_{BE} = 500 Ω	V_S −6.5			mV

NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

11

55451B/75451B
DUAL POSITIVE AND PERIPHERAL DRIVER

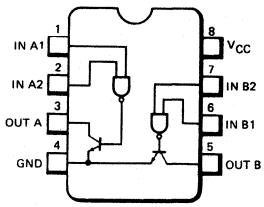
EQUIVALENT CIRCUIT (Each Driver)



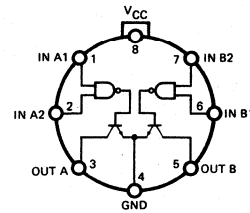
Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55451B	55451BRM
75451B	75451BRC
75451B	75451BTC

ORDER INFORMATION

TYPE	PART NO.
55451B	55451BHM
75451B	75451BHC

Positive Logic: $Z = XY$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55451B			300	μA
				75451B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55451B		0.25	0.5	V
				75451B		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55451B		0.5	0.8	
				75451B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			7.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			52	65	mA

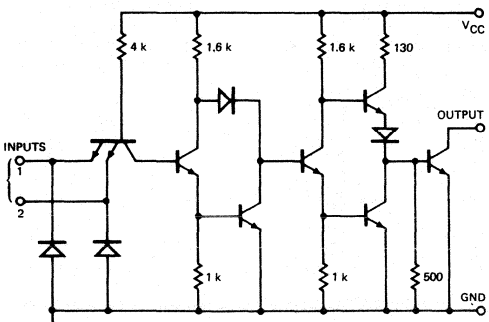
NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		18	25	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				18	25	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55452B/75452B
DUAL POSITIVE NAND PERIPHERAL DRIVER

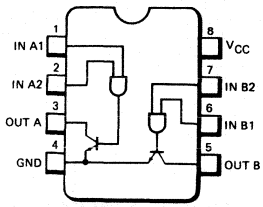
EQUIVALENT CIRCUIT (Each Driver)



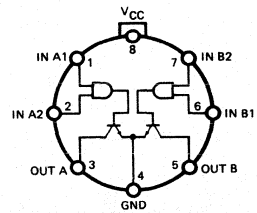
Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55452B	55452BRM
75452B	75452BRC
75452B	75452BTC

ORDER INFORMATION

TYPE	PART NO.
55452B	55452BHM
75452B	75452BHC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55452B			300	μA
				75452B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55452B		0.25	0.5	V
				75452B		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55452B		0.5	0.8	
				75452B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			11	14	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			56	71	mA

NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

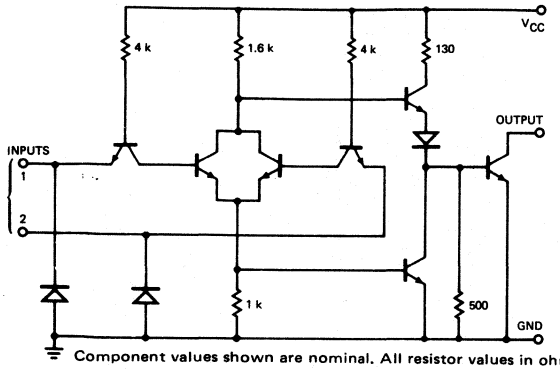
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				22	35	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

11

55453B/75453B
DUAL POSITIVE OR PERIPHERAL DRIVER

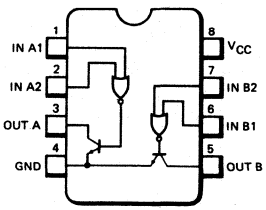
EQUIVALENT CIRCUIT (Each Driver)



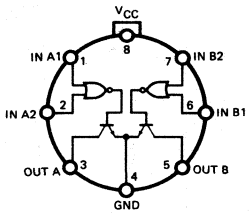
Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55453B	55453BRM
75453B	75453BRC
75453B	75453BTC

ORDER INFORMATION

TYPE	PART NO.
55453B	55453BHM
75453B	75453BHC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55453B			300	µA
				75453B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55453B		0.25	0.5	V
				75453B		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55453B		0.5	0.8	
				75453B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			54	68	mA

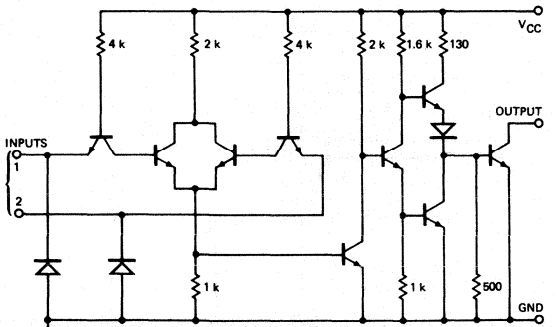
NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		18	25	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				16	25	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55454B/75454B
DUAL POSITIVE NOR PERIPHERAL DRIVER

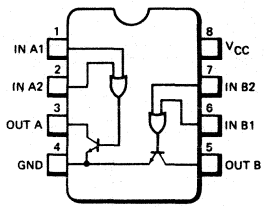
EQUIVALENT CIRCUIT (Each Driver)



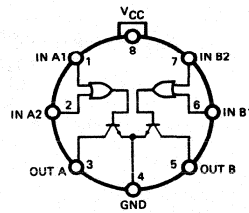
Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55454B	55454BRM
75454B	75454BRC
75454B	75454BTC

ORDER INFORMATION

TYPE	PART NO.
55454B	55454BHM
75454B	75454BHC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55454B			300	µA
				75454B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55454B		0.25	0.5	V
				75454B		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55454B		0.5	0.8	
				75454B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			61	79	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

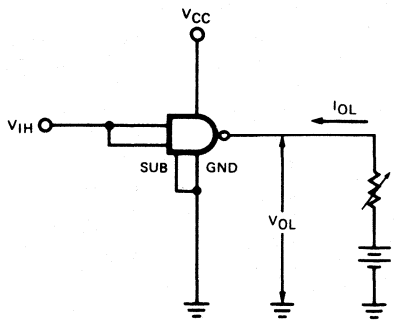
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		27	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				24	35	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT†

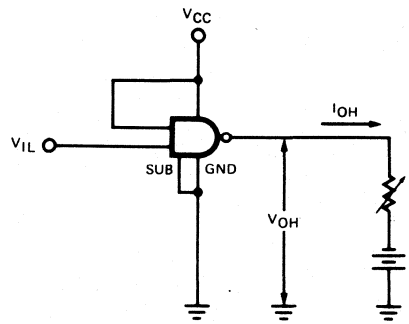
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

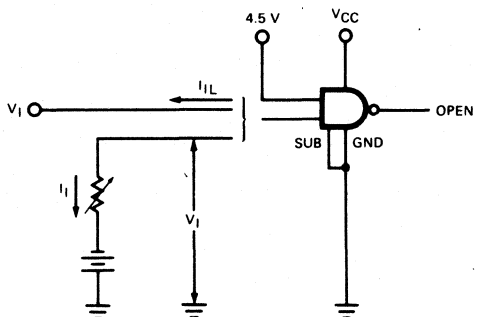
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

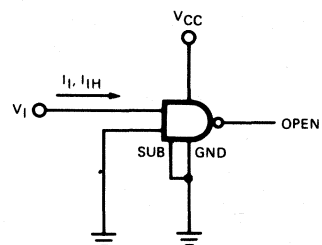
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

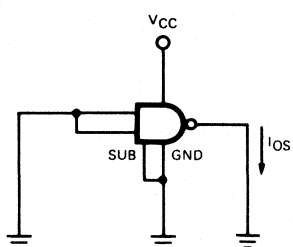
I_I, I_{IH}



Each input is tested separately

Fig. 4

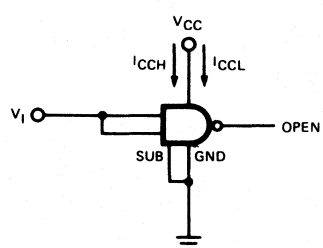
I_{OS}



Each gate is tested separately.
(55450B/75450B only)

Fig. 5

I_{CCH}, I_{CCL}

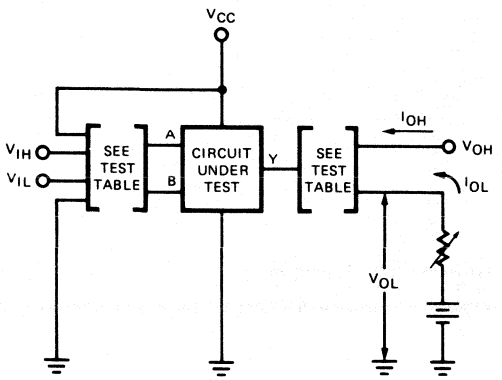


Both gates are tested simultaneously.

Fig. 6

PARAMETER MEASUREMENT INFORMATION

V_{IH}, V_{IL}, I_{OH}, V_{OL}



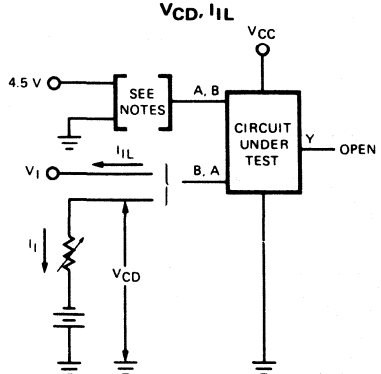
TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75451B	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75452B	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
55/75453B	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75454B	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

NOTE: Each input is tested separately.

Fig. 7

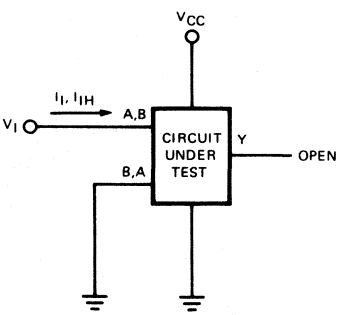
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing I_{IL} 55/75453B and 55/75454B, the input not under test is grounded. For all other circuits it is at 4.5V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

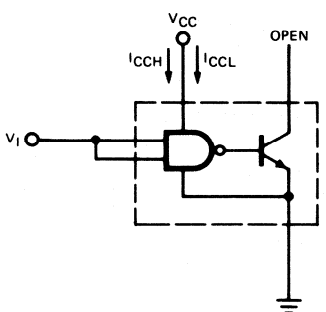
I_I, I_{IH}



Each input is tested separately.

Fig. 9

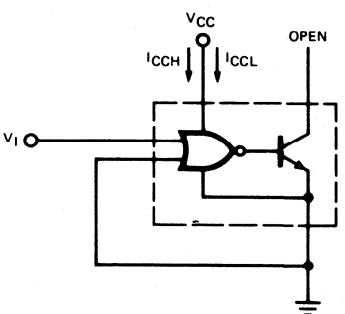
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

Fig. 11

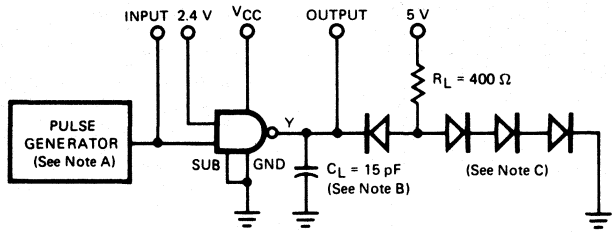
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

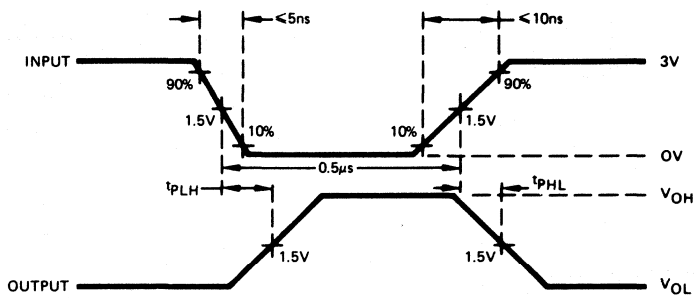
AC CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE (55450B, 75450B ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B C_L include probe and jig capacitance.
C All diodes are FD777.

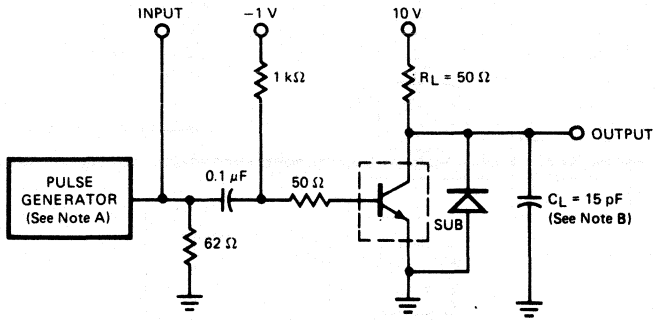
Fig. 12

PARAMETER MEASUREMENT INFORMATION

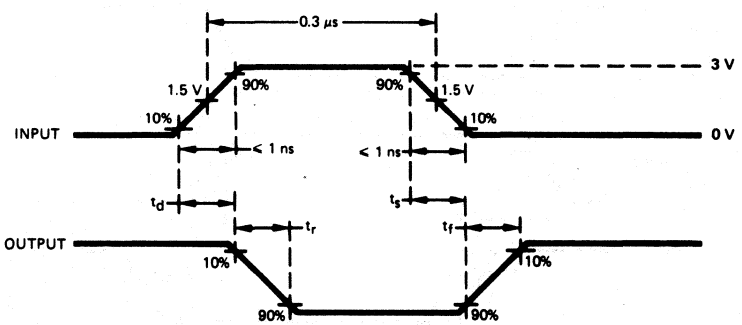
AC CHARACTERISTICS

SWITCHING TIMES, EACH TRANSISTOR (55450B, 75450B ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

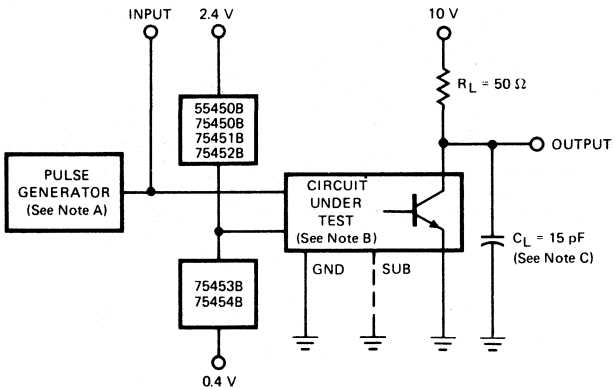
Fig. 13

PARAMETER MEASUREMENT INFORMATION

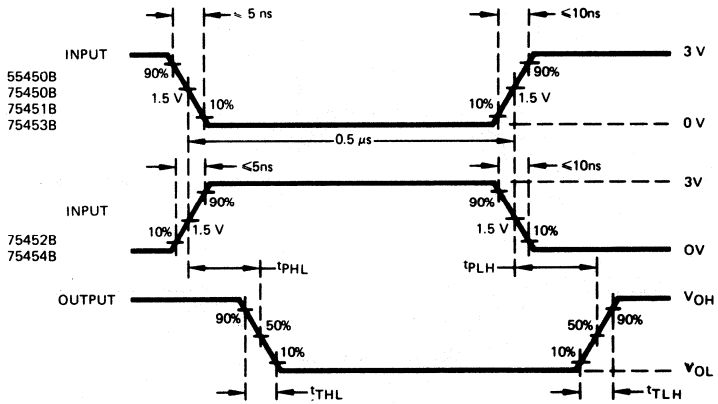
AC CHARACTERISTICS

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 500\ \Omega$.
B. When testing 55450B/75450B, connect output Y to transistor baseand ground the substrate terminal.
C. C_L includes probe and jig capacitance.

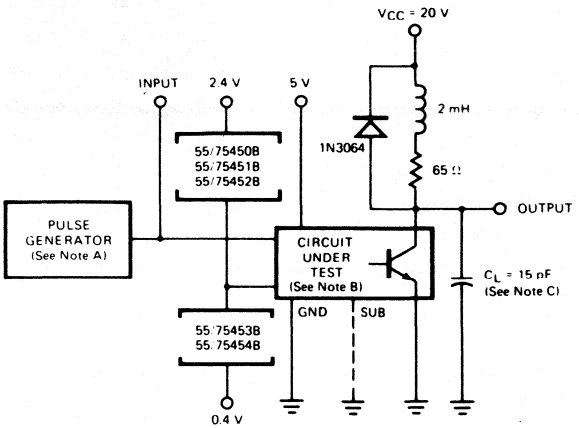
Fig. 14

PARAMETER MEASUREMENT INFORMATION

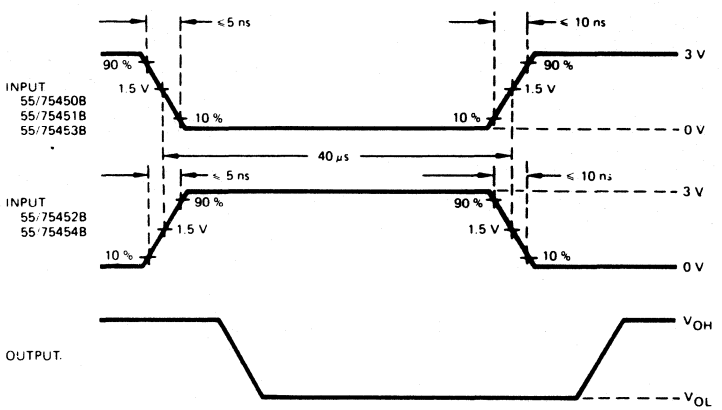
AC CHARACTERISTICS

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

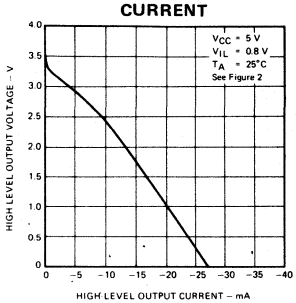


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55450 or 75450, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

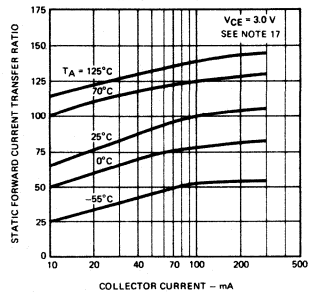
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 75450B SERIES

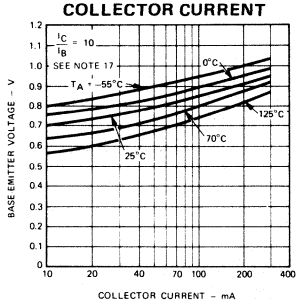
55450B/75450B TTL GATE HIGH-LEVEL OUTPUT VOLTAGE AS A FUNCTION OF HIGH-LEVEL OUTPUT CURRENT



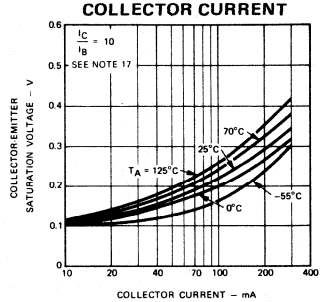
55450B/75450B TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55450B/75450B TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

55/75460 • 55/75461 • 55/75462
55/75463 • 55/75464
DUAL HIGH VOLTAGE HIGH CURRENT PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55/75460 Peripheral Driver Series converts TTL and DTL logic levels to HIGH voltage, HIGH current levels. The 55/75460 Series is directly interchangeable with the 55/75450 Series and affords higher breakdown at the expense of speed. The 55/75460 Series features two 54/74 TTL input gates and two HIGH voltage HIGH current npn uncommitted transistors.

The 55/75461, 55/75462, 55/75463 and 55/75464 feature two standard 54/74 TTL input gates in AND, NAND, OR and NOR configurations, respectively. The logic gates are internally connected to the bases of the npn transistors.

- **NO OUTPUT LATCH-UP AT 30 V**
- **MEDIUM SWITCHING SPEED**
- **300 mA OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

TEST TABLE 1 – Operating Temperature Range and Supply Voltage Range

	55460 Series	75460 Series
Temperature, T_A	−55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

11

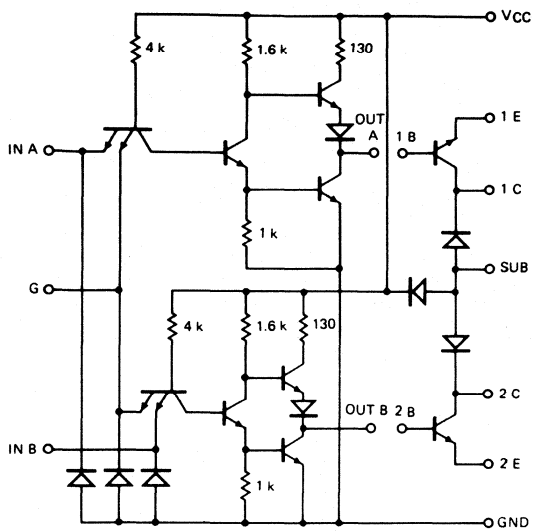
ABSOLUTE MAXIMUM RATINGS

	55460	75460	55461 55462 55463 55464	75461 75462 75463 75464
Supply Voltage, V_{CC} (Note 1)	7 V	7 V	7 V	7 V
Input Voltage (Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage (Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (Note 6)	40 V	40 V		
Collector to Substrate Voltage (Note 6)	40 V	40 V		
Collector to Base Voltage	40 V	40 V		
Collector to Emitter Voltage (Note 3)	40 V	40 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (Notes 1 and 4)			35 V	35 V
Continuous Collector Current (Note 5)	300 mA	300 mA		
Continuous Output Current (Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Free-Air Temperature Range	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP and Metal Can (Soldering, 30 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 55460 and 75460 only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 70°C ambient temperature, derate linearly at 8.3 mW/°C for hermetic DIP, and 6.3 mW/°C for metal can. For the flatpak derate at 7.1 mW/°C. For plastic Mini DIP and hermetic Mini DIP derate above 30°C at 6.7 mW/°C. The rating for metal can requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 95°C/W.

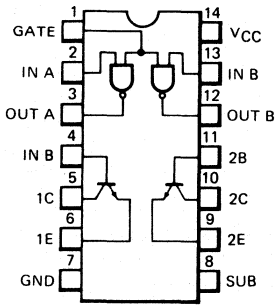
55460/75460
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = \overline{X}\overline{Y}$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55460	55460DM
55460	55460FM
75460	75460DC
75460	75460PC

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

TTL Gates

SYMBOL	PARAMETER		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNIT
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = -400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA	55460		0.25	0.5	V
					75460		0.25	0.4	
I_I	Input Current at Maximum Input Voltage	Input A, B	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Gate						2	
I_{IH}	Input HIGH Current	Input A, B	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Gate						80	
I_{IL}	Input LOW Current	Input A, B	3	V_{CC} = MAX, V_I = 0.4 V				-1.6	mA
		Gate						-3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		-18	-35	-55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2.8	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			7	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55460/75460

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

Output Transistors

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP (Note 10)	MAX	UNIT
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		40			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		40			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55460 T_A=−55°C	10			
			75460 T_A=0°C	20			
		V_{CE} = 3 V, I_C = 300 mA	55460 T_A=−55°C	15			
			75460 T_A=0°C	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55460		0.85	1.2	V
			75460		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55460		1.0	1.4	V
			75460		1.0	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55460		0.25	0.5	V
			75460		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55460		0.45	0.8	V
			75460		0.45	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		22		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS (Note 12)	MIN*	TYP	MAX	UNIT
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		10		ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		16		ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		23		ns
t_f	Fall Time				14		ns

Gates and Transistors Combined

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		45	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				10	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, I_C ≈ 300 mA R_{BE} = 500 Ω	V_S −10			mV

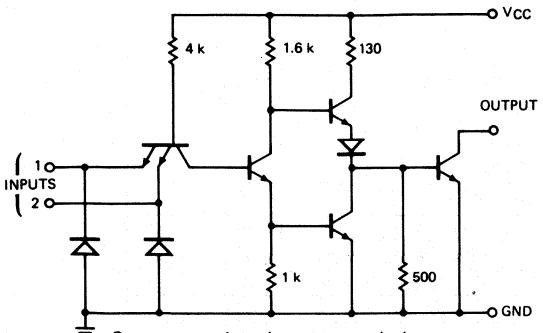
NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

11

55461/75461

DUAL POSITIVE AND PERIPHERAL DRIVER

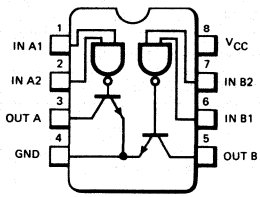
EQUIVALENT CIRCUIT (Each Driver)



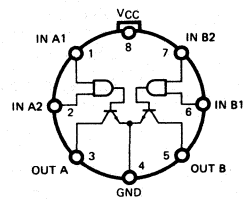
Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT
1	2	
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55461	55461RM
75461	75461RC
75461	75461TC

ORDER INFORMATION

TYPE	PART NO.
55461	55461HM
75461	75461HC

Positive Logic: $Z = XY$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IH} = 2 V	55461			300	µA
				75461			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55461		.16	0.5	V
				75461		.16	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55461		.35	0.8	
				75461		.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			61	76	mA

NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

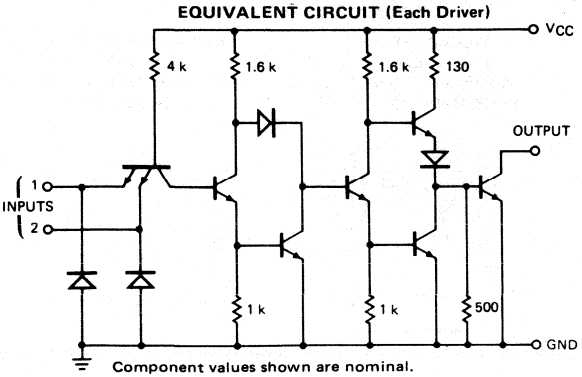
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

55462/75462

DUAL POSITIVE NAND PERIPHERAL DRIVER

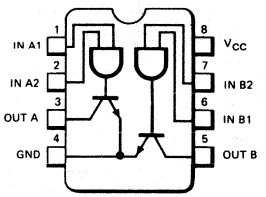
EQUIVALENT CIRCUIT (Each Driver)



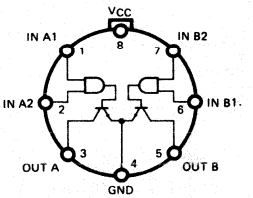
Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55462	7562RM
75462	75462RC
75462	75462TC

ORDER INFORMATION

TYPE	PART NO.
55462	55462HM
75462	75462HC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V V_{IL} = 0.8 V	55462			300	µA
				75462			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V I_{OL} = 100 mA	55462		.16	0.5	V
				75462		.16	0.4	
			V_{CC} = MIN, V_{IH} = 2 V I_{OL} = 300 mA	55462		.35	0.8	
				75462		.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			65	76	mA

NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

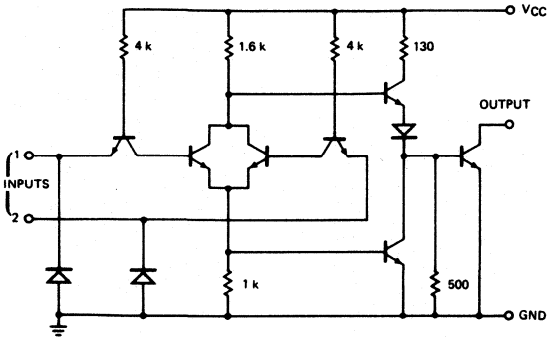
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

11

55463/75463
DUAL POSITIVE OR PERIPHERAL DRIVER

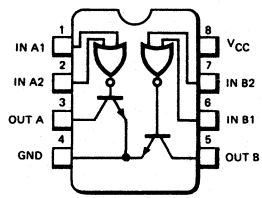
EQUIVALENT CIRCUIT (Each Driver)



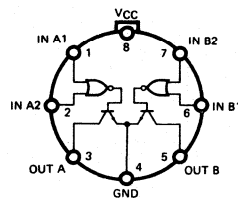
Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55463	55463RM
75463	75463RC
75463	75463TC

ORDER INFORMATION

TYPE	PART NO.
55463	55463HM
75463	75463HC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IH} = 2 V	55463			300	µA
				75463			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55463		0.18	0.5	V
				75463		0.18	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55463		0.39	0.8	
				75463		0.39	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			63	76	mA

NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

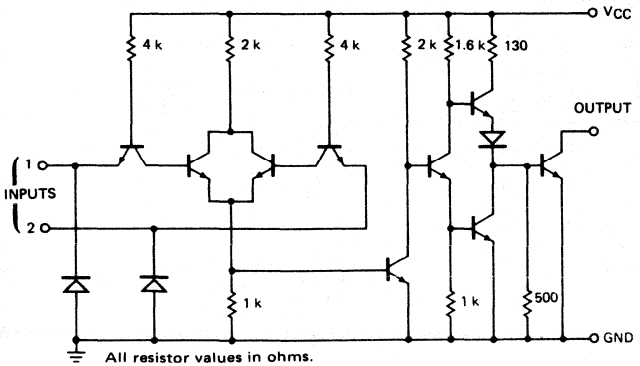
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN-	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

55464/75464

DUAL POSITIVE NOR PERIPHERAL DRIVER

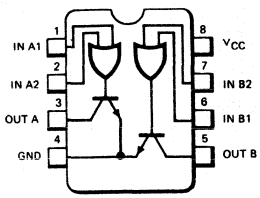
EQUIVALENT CIRCUIT (Each Driver)



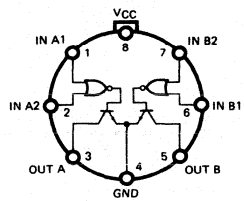
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55464	55464RM
75464	75464RC
75464	75464TC

ORDER INFORMATION

TYPE	PART NO.
55464	55464HM
75464	75464HC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IL} = 0.8 V	55464			300	µA
				75464			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55464		0.17	0.5	V
				75464		0.17	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55464		0.38	0.8	
				75464		0.38	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			14	19	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			72	85	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

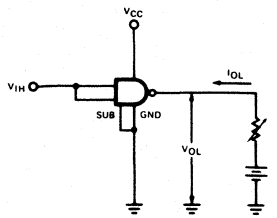
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT†

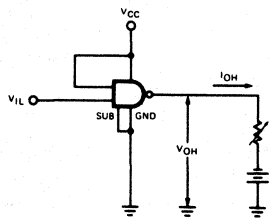
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

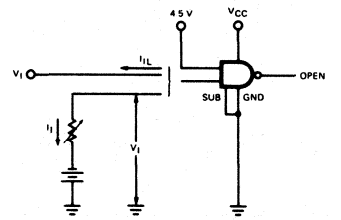
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

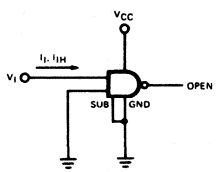
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

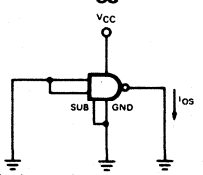
I_I, I_{IH}



Each input is tested separately

Fig. 4

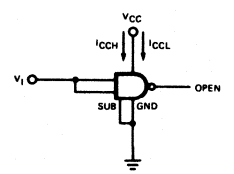
I_{OS}



Each gate is tested separately.
(55460/75460 only)

Fig. 5

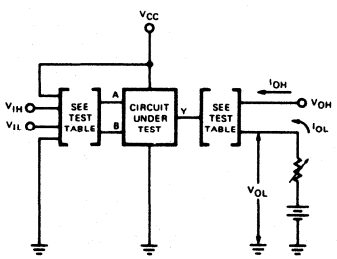
I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

Fig. 6

V_{IH}, V_{IL}, I_{OH}, V_{OL}



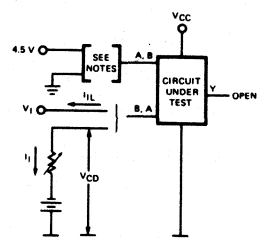
NOTE: Each input is tested separately.

Fig. 7

TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75461	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75462	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
55/75463	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75464	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

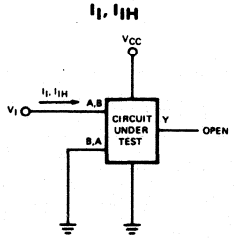
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing I_{IL} 55/75463 and 55/75464, the input not under test is grounded. For all other circuits it is at 4.5V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

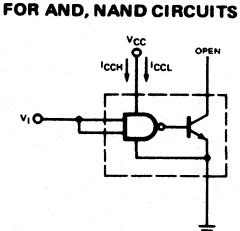
I_I, I_{IH}



Each input is tested separately.

Fig. 9

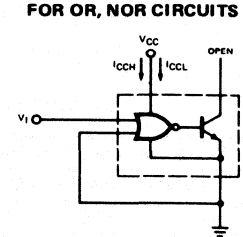
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

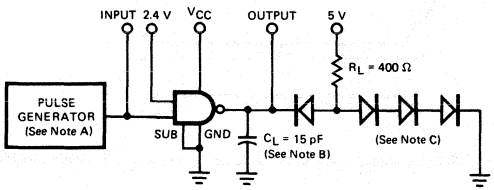
Fig. 11

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

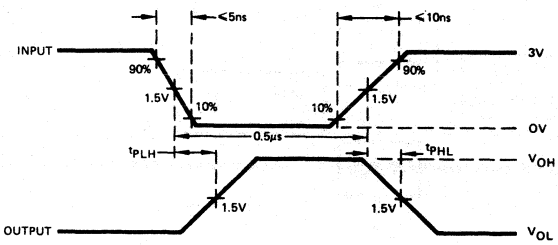
PARAMETER MEASUREMENT INFORMATION
SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE
(55460, 75460 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS

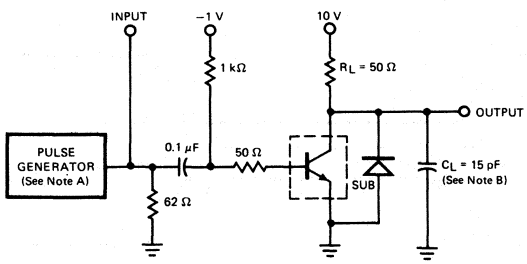


NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are FD777.

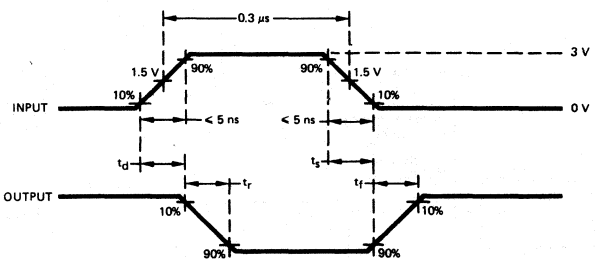
Fig. 12

SWITCHING TIMES, EACH TRANSISTOR
(55460, 75460 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS

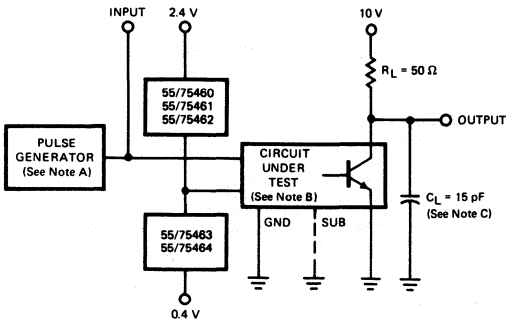


NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

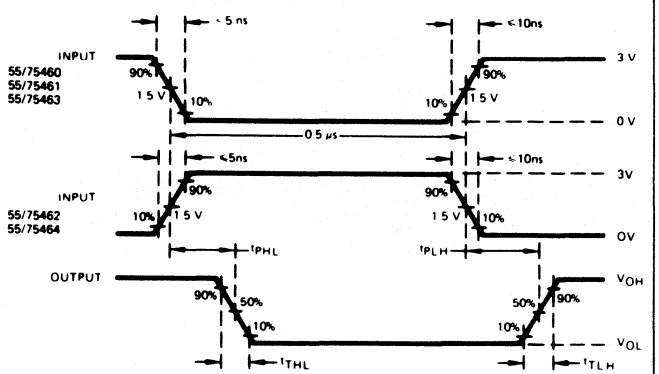
Fig. 13

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

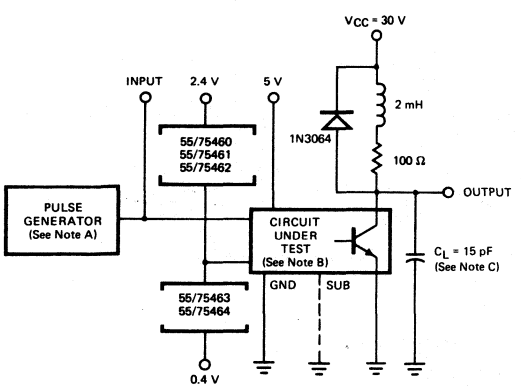


NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing 55460/75460, connect output Y to transistor base and ground the substrate terminal
C. C_L includes probe and jig capacitance.

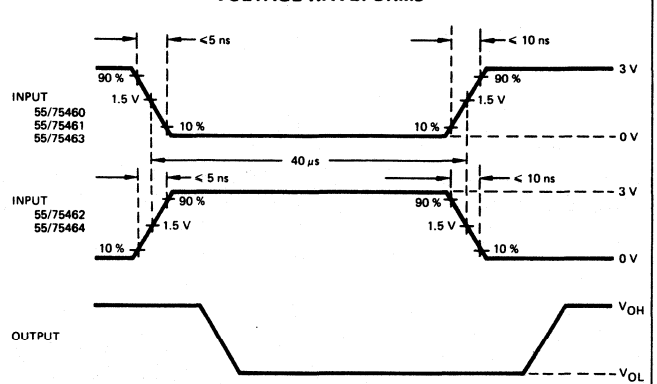
Fig. 14

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

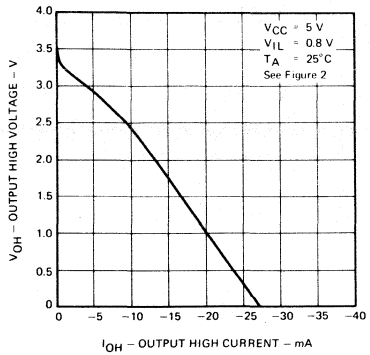


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55460 or 75460, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

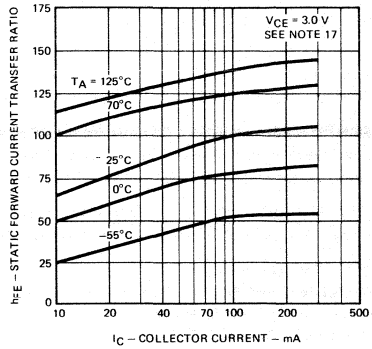
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 55460/75460 SERIES

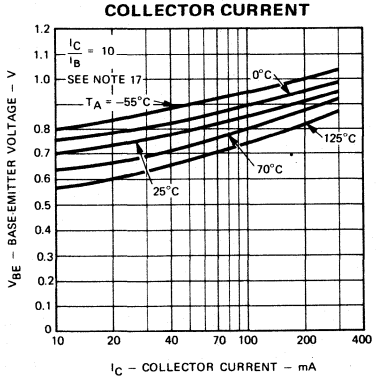
55460/75460 TTL GATE OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



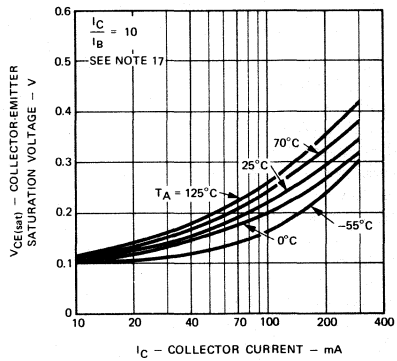
55460/75460 TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55460/75460 TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

11

55/75470 • 55/75471 • 55/75472
55/75473 • 55/75474

DUAL HIGH VOLTAGE HIGH CURRENT PERIPHERAL DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55/75470 Peripheral Driver Series converts TTL and DTL logic levels to HIGH voltage, HIGH current levels. The 55/75470 Series is directly interchangeable with the 55/75460 Series and affords higher breakdown at the expense of speed. The 55/75470 Series features two 54/74 TTL input gates and two HIGH voltage HIGH current npn uncommitted transistors.

The 55/75471, 55/75472, 55/75473 and 55/75474 feature two standard 54/74 TTL input gates in AND, NAND, OR and NOR configurations, respectively. The logic gates are internally connected to the bases of the npn transistors.

- **NO OUTPUT LATCH-UP AT 40 V**
- **MEDIUM SWITCHING SPEED**
- **300 mA OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

TEST TABLE 1 – Operating Temperature Range and Supply Voltage Range

	55470 Series	75470 Series
Temperature, T_A	−55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

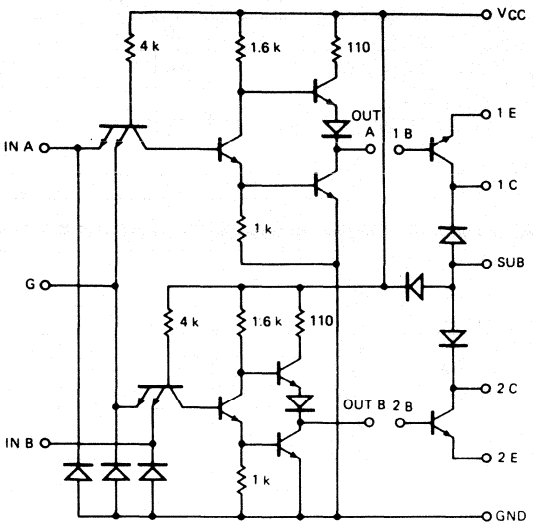
ABSOLUTE MAXIMUM RATINGS

	55470	55470	55471 55472 55473 55474	75471 75472 75473 75474
Supply Voltage, V_{CC} (Note 1)	7 V	7 V	7 V	7 V
Input Voltage (Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage (Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (Note 6)	50 V	50 V		
Collector to Substrate Voltage (Note 6)	50 V	50 V		
Collector to Base Voltage	50 V	50 V		
Collector to Emitter Voltage (Note 3)	50 V	50 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (Notes 1 and 4)			40 V	40 V
Continuous Collector Current (Note 5)	300 mA	300 mA		
Continuous Output Current (Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Free-Air Temperature Range	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP, Flatpak and Metal Can (Soldering, 60 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 55470 and 75470 only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Flatpak, derate at 7.1 mW/°C above 40°C. For the Molded Mini DIP and Ceramic Mini DIP, derate at 6.7 mW/°C above 30°C. For the Metal Can, derate at 6.3 mW/°C above 20°C. The rating for Metal Can requires a heat sink that provides a thermal resistance from case to free air ($R_{\theta CA}$) of not more than 95°C.

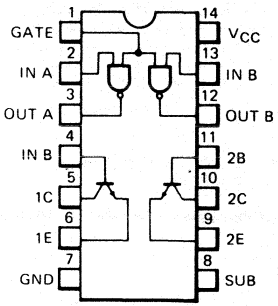
55470/75470
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = \overline{XY}$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55470	55470DM
55470	55470FM
75470	75470DC
75470	75470PC

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

TTL Gates

SYMBOL	PARAMETER		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNIT
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = -400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V I_{OL} = 16 mA	55470		0.25	0.5	V
					75470		0.25	0.4	
I_I	Input Current at Maximum Input Voltage	Input A, B	4	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
		Gate						2.0	
I_{IH}	Input HIGH Current	Input A, B	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Gate						80	
I_{IL}	Input LOW Current	Input A, B	3	V_{CC} = MAX, V_I = 0.4 V				-1.6	mA
		Gate						-3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		-18	-35	-55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2.8	4.0	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			7.0	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

11

55470/75470

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

Output Transistors

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP (Note 10)	MAX	UNIT
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		50			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		50			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55470 T_A=−55°C	10			
			75470 T_A=0°C	20			
		V_{CE} = 3 V, I_C = 300 mA	55470 T_A=−55°C	15			
			75470 T_A=0°C	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55470		0.85	1.2	V
			75470		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55470		1.0	1.4	V
			75470		1.0	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55470		0.25	0.5	V
			75470		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55470		0.45	0.8	V
			75470		0.45	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		26		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				10		ns

Output Transistors

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNIT
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		10		ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		16		ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		23		ns
t_f	Fall Time				14		ns

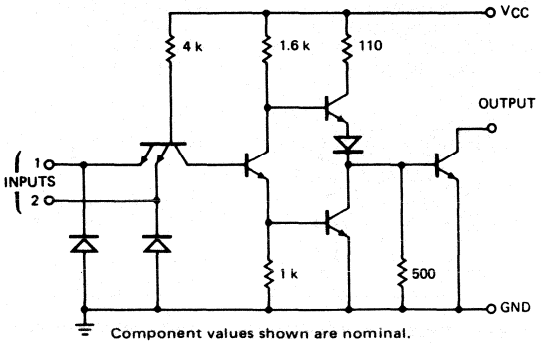
Gates and Transistors Combined

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		55	75	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				45	60	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 40 V, I_C ≈ 300 mA, R_{BE} = 500 Ω	V_S − 15			mV

NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

55471/75471
DUAL POSITIVE AND PERIPHERAL DRIVER

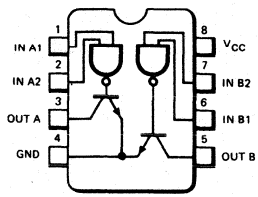
EQUIVALENT CIRCUIT (Each Driver)



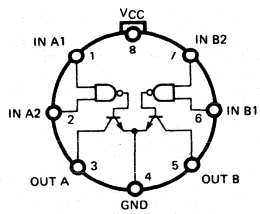
Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT
1	2	
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55471	55471RM
75471	75471RC
75471	75471TC

ORDER INFORMATION

TYPE	PART NO.
55471	55471HM
75471	75471HC

Positive Logic: Z = XY

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2.0			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 40 V, V_{IH} = 2 V	55471			300	μA
				75471			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55471		0.16	0.5	V
				75471		0.16	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55471		0.35	0.8	
				75471		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			61	76	mA

NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

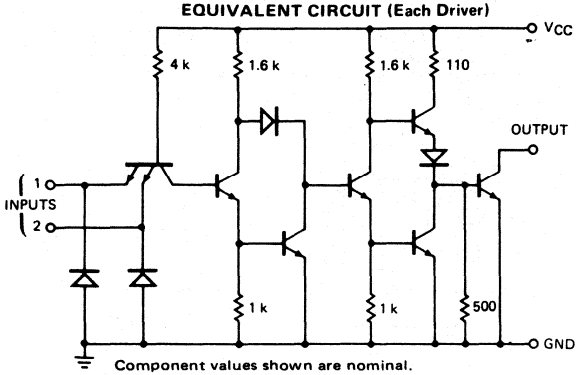
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8.0	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 40 V, $I_O \approx$ 300 mA	V_S -15			mV

11

55472/75472
DUAL POSITIVE NAND PERIPHERAL DRIVER

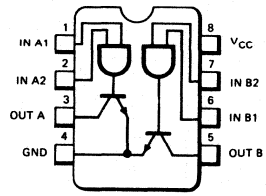
EQUIVALENT CIRCUIT (Each Driver)



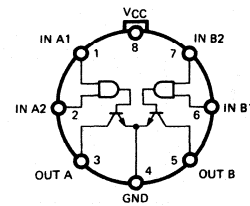
Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55472	55472RM
75472	75472RC
75472	75472TC

ORDER INFORMATION

TYPE	PART NO.
55472	55472HM
75472	75472HC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2.0			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 40 V, V_{IL} = 0.8 V	55472			300	μA
				75472			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55472		0.16	0.5	V
				75472		0.16	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55472		0.35	0.8	
				75472		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			65	76	mA

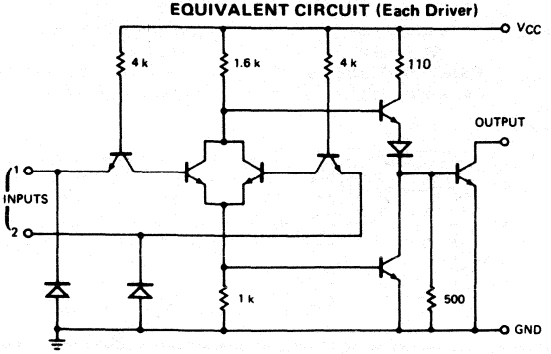
NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		60	75	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				45	60	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 40 V, $I_O \approx$ 300 mA	V_S - 15			mV

55473/75473
DUAL POSITIVE OR PERIPHERAL DRIVER

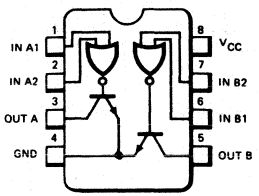
EQUIVALENT CIRCUIT (Each Driver)



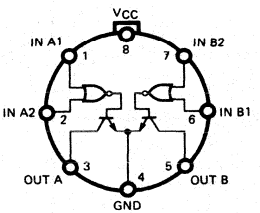
Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55473	55473RM
75473	75473RC
75473	75473TC

ORDER INFORMATION

TYPE	PART NO.
55473	55473HM
75473	75473HC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2.0			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 40 V, V_{IH} = 2 V	55473			300	μA
				75473			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55473		0.18	0.5	V
				75473		0.18	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55473		0.39	0.8	
				75473		0.39	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			63	76	mA

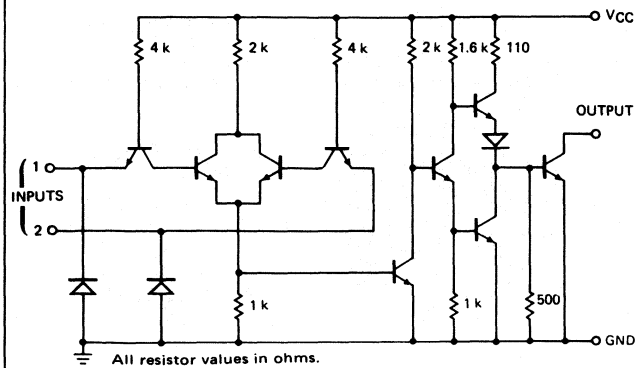
NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 40 V, $I_O \approx$ 300 mA	V_S - 15			mV

55474/75474
DUAL POSITIVE NOR PERIPHERAL DRIVER

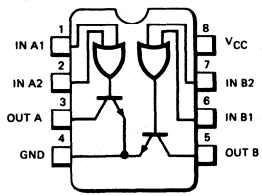
EQUIVALENT CIRCUIT (Each Driver)



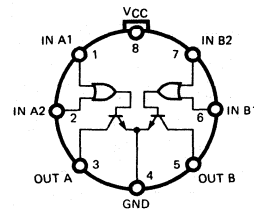
All resistor values in ohms.

CONNECTION DIAGRAMS

8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55474	55474RM
75474	75474RC
75474	75474TC

ORDER INFORMATION

TYPE	PART NO.
55474	55474HM
75474	75474HC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: (Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNIT
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 40 V V_{IL} = 0.8 V	55474			300	μA
				75474			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V I_{OL} = 100 mA	55474		0.17	0.5	V
				75474		0.17	0.4	
			V_{CC} = MIN, V_{IH} = 2 V I_{OL} = 300 mA	55474		0.38	0.8	
				75474		0.38	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			14	19	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			72	85	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

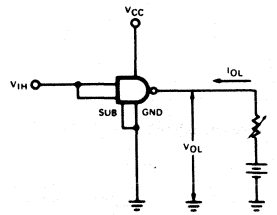
AC CHARACTERISTICS: (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		60	75	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				45	60	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 40 V, $I_O \approx$ 300 mA	V_S -15			mV

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT†

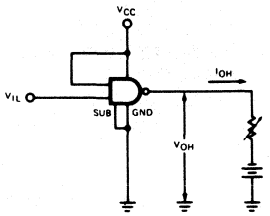
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

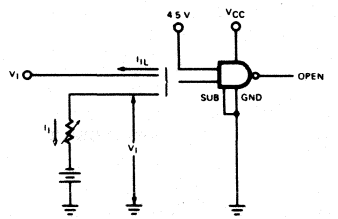
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

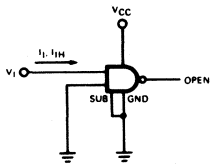
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

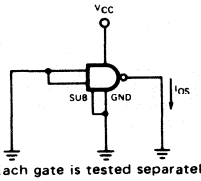
I_I, I_{IH}



Each input is tested separately

Fig. 4

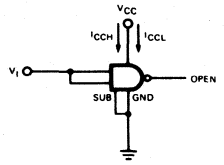
I_{OS}



Each gate is tested separately.
(55470/75470 only)

Fig. 5

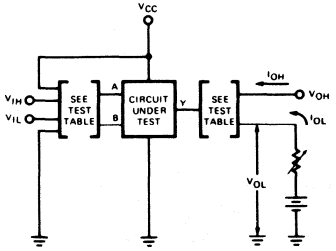
I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

Fig. 6

V_{IH}, V_{IL}, I_{OH}, V_{OL}



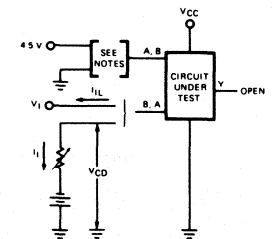
NOTE: Each input is tested separately.

Fig. 7

TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75471	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
55/75472	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
55/75473	V_{IH}	GND	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
55/75474	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

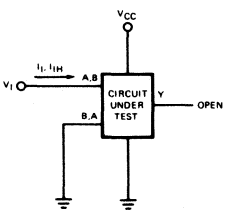
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing I_{IL} 55/75473 and 55/75474, the input not under test is grounded. For all other circuits it is at 4.5V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

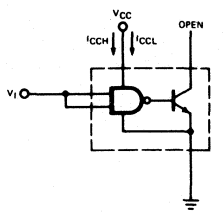
I_I, I_{IH}



Each input is tested separately.

Fig. 9

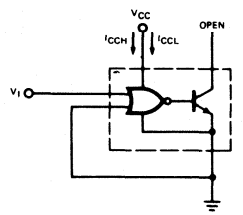
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

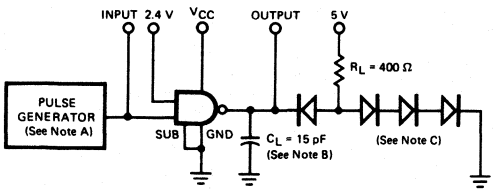
Fig. 11

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

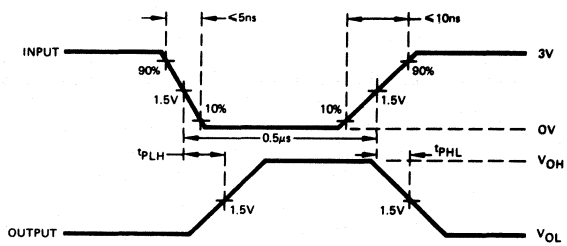
PARAMETER MEASUREMENT INFORMATION
SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE
(55470, 75470 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS

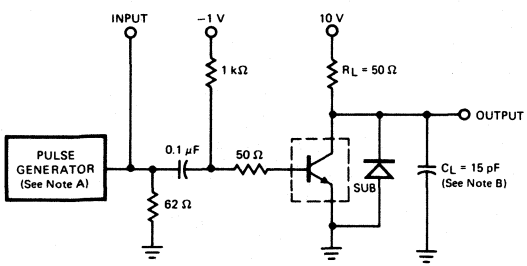


NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are FD777.

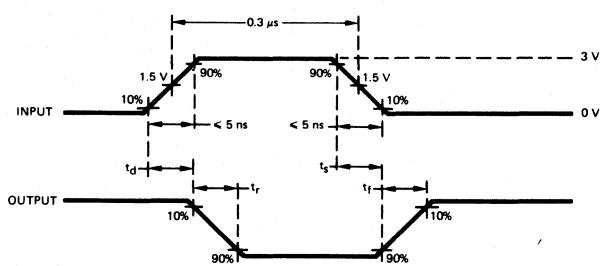
Fig. 12

SWITCHING TIMES, EACH TRANSISTOR
(55470, 75470 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS

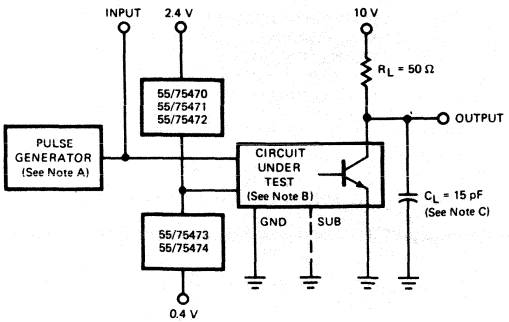


NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

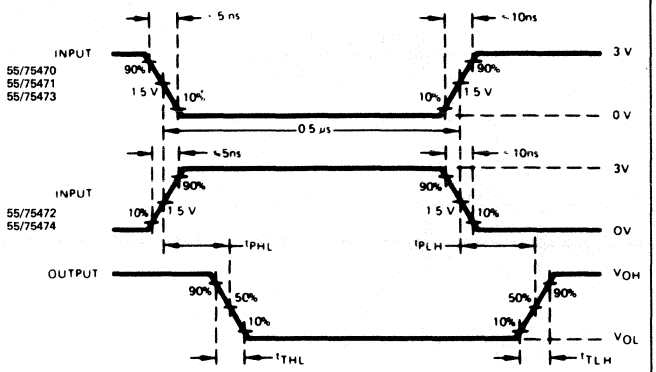
Fig. 13

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS



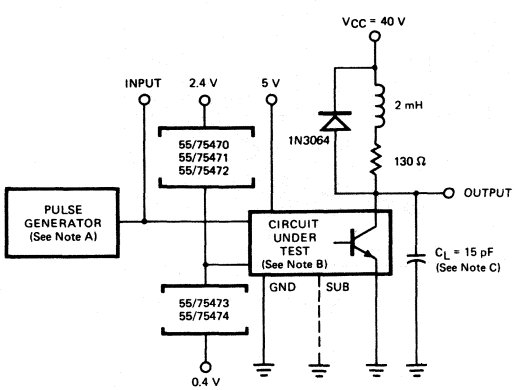
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing 55470/75470, connect output Y to transistor base and ground the substrate terminal
C. C_L includes probe and jig capacitance.

Fig. 14

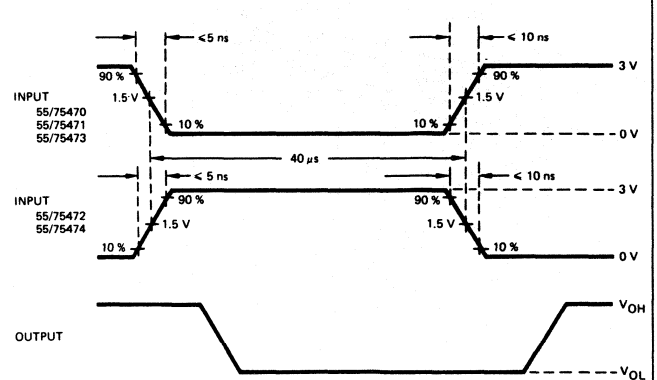
11

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

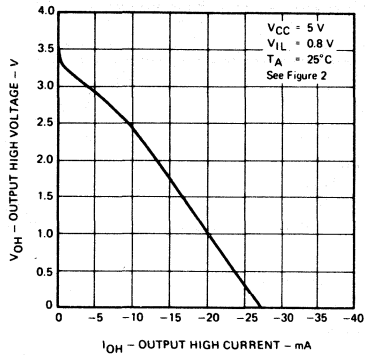


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55470 or 75470, connect output Y to transistor base with a 500 Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

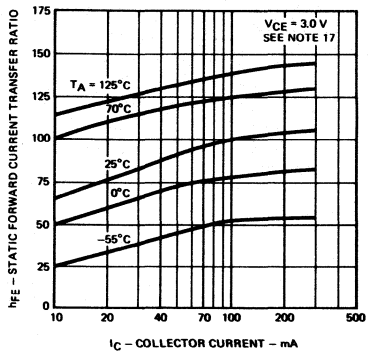
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 55470/75470 SERIES

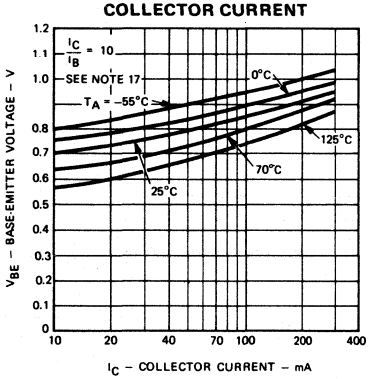
55470/75470 TTL GATE OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



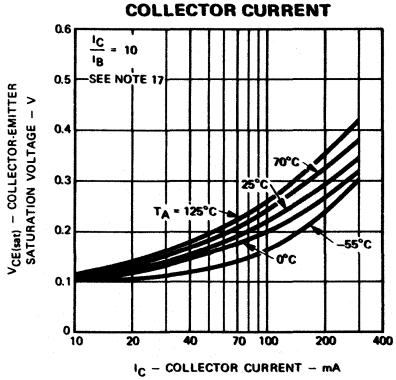
55470/75470 TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55470/75470 TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

75123

DUAL SINGLE-ENDED LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 75123 Dual Line Driver meets the requirements of the IBM System/360 I/O Interface Specification for interface drivers. Inputs are TTL/DTL compatible. Logic has been incorporated to ensure that no spurious noise is generated on the transmission line during the power-up and power-down sequence. The outputs are protected from short circuits and have uncommitted emitter outputs which allows DOT-OR logic to be performed in party line data bus applications.

- I_{OUT} = 59.3 mA AT 3.11 V
- UNCOMMITTED EMITTER OUTPUTS FOR PARTY LINE/WIRED-OR APPLICATIONS
- SHORT CIRCUIT PROTECTION
- SINGLE 5.0 V SUPPLY OPERATION
- AND-OR LOGIC CONFIGURATION
- DIRECT REPLACEMENT FOR 8T23

ABSOLUTE MAXIMUM RATINGS

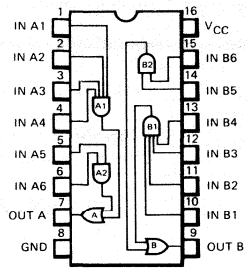
Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperatures	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	800 mW

FUNCTION TABLE

INPUTS						OUTPUT
1	2	3	4	5	6	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
ALL OTHER INPUT COMBINATIONS						L

H = HIGH
L = LOW
X = Don't Care

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P

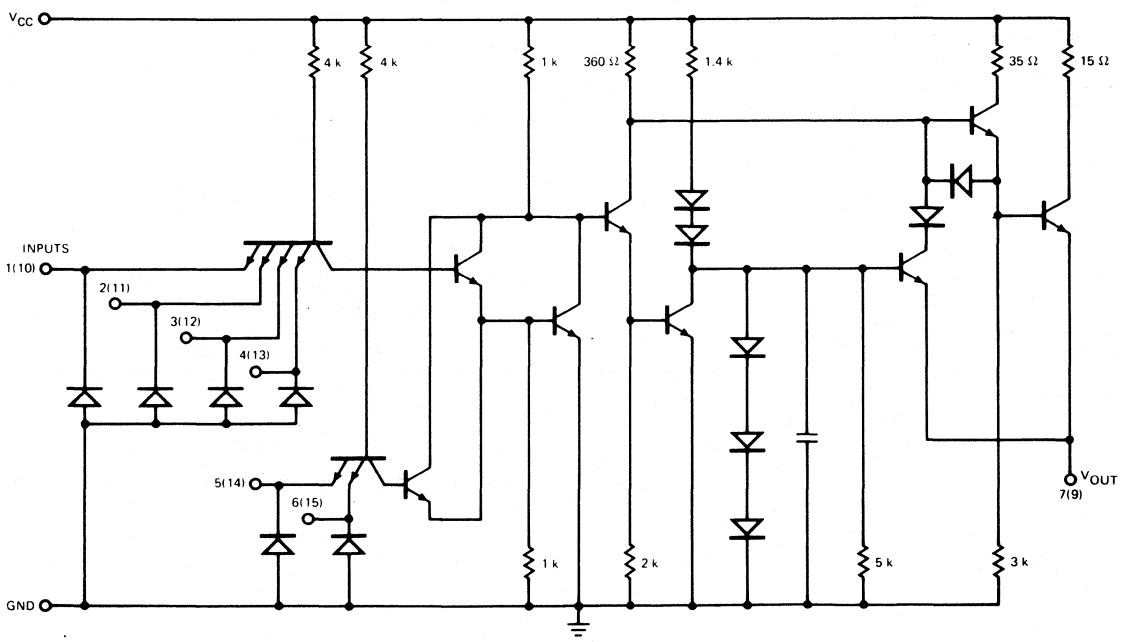


ORDER INFORMATION

TYPE	PART NO.
75123	75123DC
75123	75123PC

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 60°C. Above 60°C derate linearly at 8.3 mW/°C.

EQUIVALENT CIRCUIT (FOR EACH DRIVER)



RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5.0	5.25	V
Output HIGH Current, I_{OH}				−75	mA
Operating Ambient Temperature, T_A	75121	0		70	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0 V, I_{IN} = −12 mA				−1.5	V
$V_{(BR)I}$	Input Breakdown Voltage	V_{CC} = 5.0 V, I_{IN} = 10 mA		5.5			V
V_{OH}	Output HIGH Voltage	V_{CC} = 5.0 V, V_{IH} = 2.0 V,	T_A = 25°C	3.11			V
		I_{OH} = −59.3 mA, See Note 3	T_A = 0°C to 70°C	2.9			
I_{OH}	Output HIGH Current	V_{CC} = 5.0 V, V_{IH} = 4.5 V, V_{OH} = 2.0 V, T_A = 25°C, See Note 3		−100		−250	mA
V_{OL}	Output LOW Voltage	V_{IL} = 0.8 V, I_{OL} = −240 μA, See Note 3				0.15	V
$I_{OUT(off)}$	Off-State Output Current	V_{CC} = 0, V_{OUT} = 3.0 V				40	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V				40	μA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V		−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current	V_{CC} = 5.0 V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs HIGH	V_{CC} = 5.25 V, All Inputs at 2.0 V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs LOW	V_{CC} = 5.25 V, All Inputs at 0.8 V, Outputs Open				60	mA

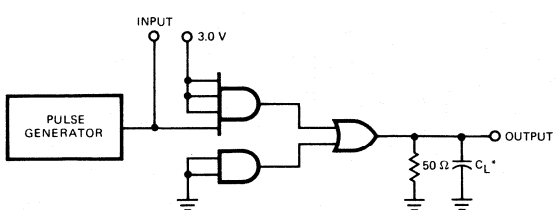
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	R_L = 50 Ω, C_L = 15 pF		12	20	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW	See Test Circuit		12	20	
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	R_L = 50 Ω, C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW	See Test Circuit		15	25	

3. The output voltage and current limits are guaranteed for any appropriate combination of HIGH and LOW inputs specified by the function table for the desired output.

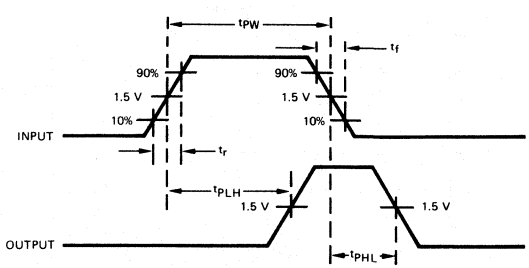
AC CHARACTERISTICS

TEST CIRCUIT



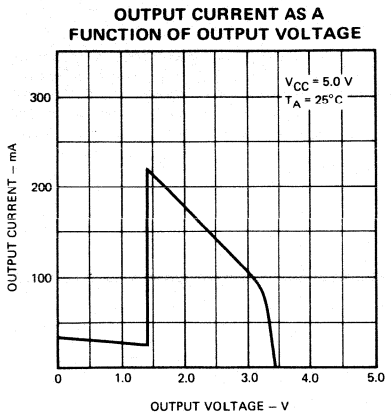
INPUT PULSE:
Amplitude = 2.6 V
t_{PW} = 50 ns (50% Duty Cycle)
$t_r = t_f \leq 5$ ns (10% and 90% measurement points)

WAVEFORMS

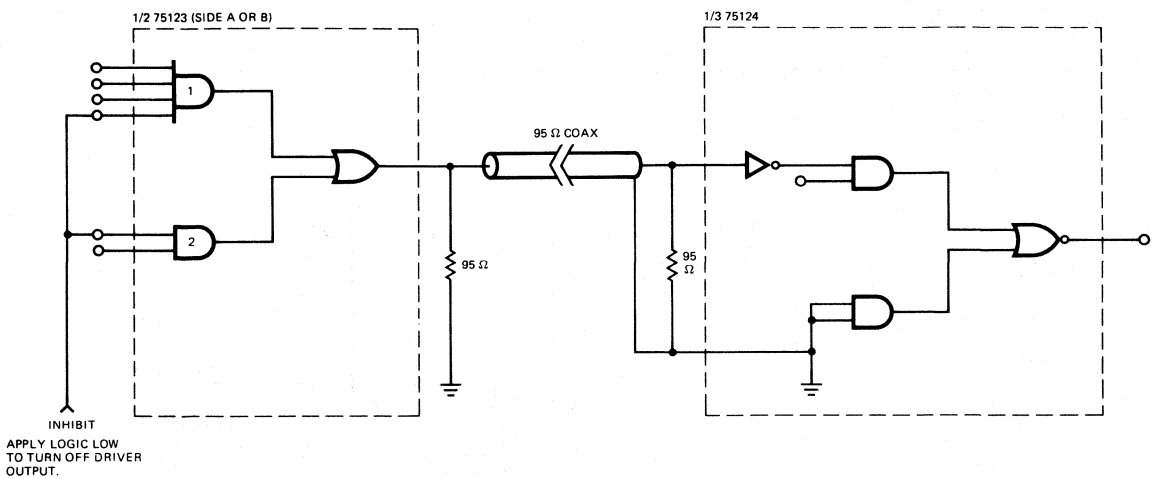


*Includes probe and jig capacitance

TYPICAL PERFORMANCE CURVE FOR 75123



TYPICAL APPLICATION



NOTE: To insure proper logic operation, unused inputs should not be left floating. Tie the unused inputs to V_{CC} through a current limit resistor (2.2kΩ).
To inhibit the driver, apply a logic LOW voltage to one input from gate 1 and 2 as shown above.

75124
TRIPLE LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 75124 Triple Line Receiver meets IBM System 360 I/O Interface Specifications (File No. S360-19). Logic inputs are fully TTL or DTL compatible. The R (Receive) input is designed to withstand a positive dc input of +7.0 V with power on (V_{CC+} = 5.0 V) and +6.0 V with power off, (V_{CC+} = 0 V) and a negative dc input of 0.15 V with power on or off. This protection allows normal bus operation even if one or more receivers have been powered down.

- **MEETS IBM SYSTEM/360 I/O INTERFACE SPECIFICATION**
- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5.0 V SUPPLY OPERATION**
- **DIRECT REPLACEMENT FOR 8T24**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	R Input with V_{CC} Applied	7.0 V
	R Input with V_{CC} not Applied	6.0 V
	Logic Inputs	5.5 V
Output Voltage (Note 1)		+7.0 V
Output Current		±100 mA
Supply Voltage (Note 1)		+7.0 V
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range		0°C to +70° C
Lead Temperatures		
Hermetic DIP (Soldering, 60 s)		300°C
Molded DIP (Soldering, 10 s)		260°C
Internal Power Dissipation (Note 2)		800 mW

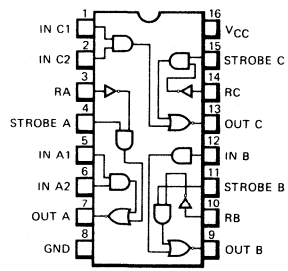
FUNCTION TABLE

INPUTS				OUTPUT
1	2*	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = HIGH
L = LOW
X = Don't Care

*Input 2 and last two lines of the Function Table are applicable to receivers A and C only.

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P

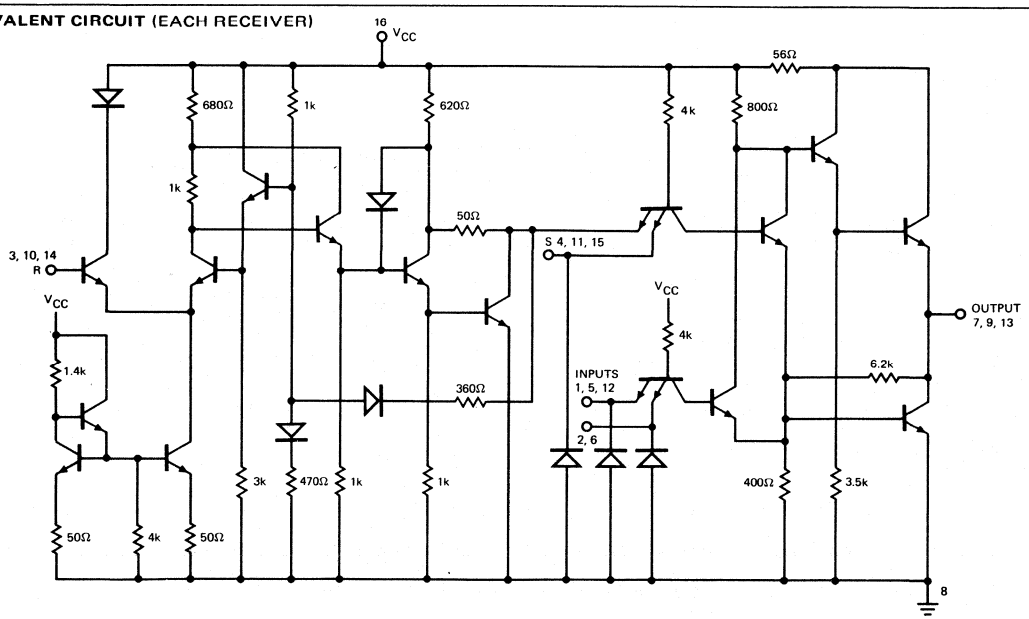


ORDER INFORMATION

TYPE	PART NO.
75124	75124DC
75124	75124PC

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 60°C. Above 60°C derate linearly at 8.3 mW/°C.

EQUIVALENT CIRCUIT (EACH RECEIVER)



RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}		4.75	5.0	5.25	V
Output HIGH Current, I_{OH}				−75	mA
Operating Ambient Temperature, T_A	75124	0		70	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 4.75 to 5.25 V, T_A = 0°C to 70°C (unless otherwise noted)

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage	In 1, 2, or S		2.0			V
		R		1.7			
V_{IL}	Input LOW Voltage	In 1, 2, or S				0.8	V
		R				0.7	
$V_{T+} - V_{T-}$	Hysteresis†	R	V_{CC} = 5.0 V, T_A = 25°C	0.2	0.4		V
V_{IN}	Input Clamp Voltage	In 1, 2, or S	V_{CC} = 5.0 V, I_{IN} = −12 mA			−1.5	V
$V_{(BR)IN}$	Input Breakdown Voltage	In 1, 2, or S	V_{CC} = 5.0 V, I_{IN} = 10 mA	5.5			V
V_{OH}	Output HIGH Voltage		V_{IH} = V_{IN} Min, V_{IL} = V_{IL} Max, I_{OH} = −800 μA, See Note 3	2.6			V
V_{OL}	Output LOW Voltage		V_{IH} = V_{IH} Min, V_{IL} = V_{IL} Max, I_{OL} = 16 mA, See Note 3			0.4	V
I_{IN}	Input Current at Maximum Input Voltage	R	V_{IN} = 7.0 V			5.0	mA
			V_{IN} = 6.0 V, V_{CC} = 0			5.0	
I_{IH}	Input HIGH Current	In 1, 2, or S	V_{IN} = 4.5 V			40	μA
		R	V_{IN} = 3.11 V			170	
I_{IL}	Input LOW Current	In 1, 2, or S	V_{IN} = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current‡		V_{CC} = 5.0 V, T_A = 25°C	−50		−100	mA
I_{CC}	Supply Current		V_{CC} = 5.25 V			72	mA

†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Hysteresis Test Circuit.

‡Not more than one output should be shorted at a time.

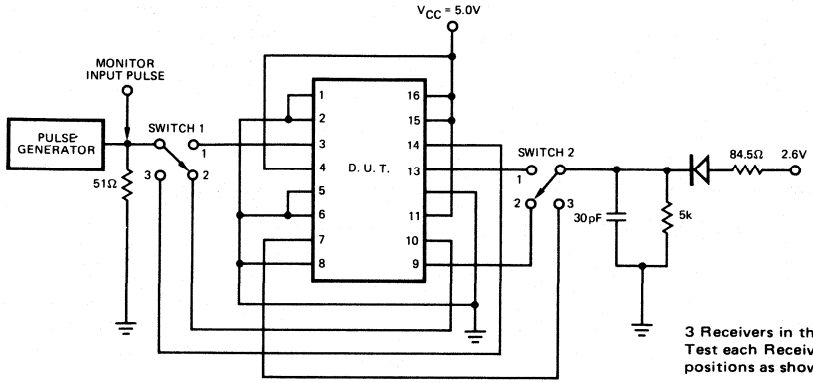
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH from R Input	See Test Circuit		20	30	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW from R Input			20	30	

3. The output voltage and current limits are guaranteed for any appropriate combination of HIGH and LOW Inputs specified by the Function Table for the desired output.

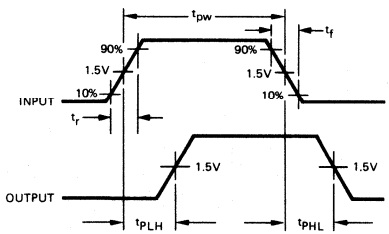
AC CHARACTERISTICS

TEST CIRCUIT



3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.

WAVEFORMS



INPUT PULSE:
Amplitude = 2.6V
Pulse width = 200ns
(50% Duty Cycle)
$t_r = t_f$ = 5ns (10% to 90%)

TABLE 1		
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

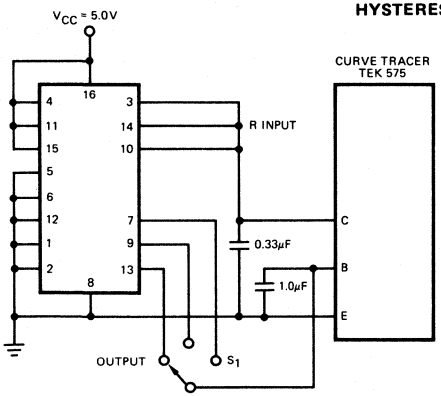
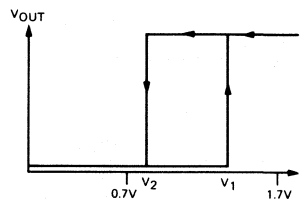


Fig. 1

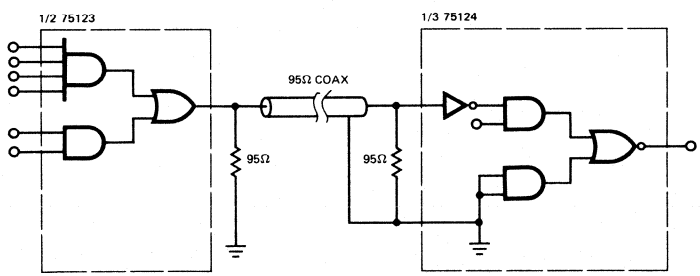


Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

1. V_1x and V_2 must be between 0.7V minimum and 1.7V maximum.
2. Hysteresis = $V_1 - V_2$

Fig. 2

TYPICAL APPLICATION



75154

QUAD LINE RECEIVER

FAIRCHILD INTEGRATED CIRCUIT

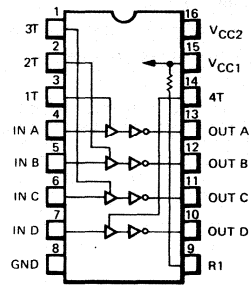
GENERAL DESCRIPTION — The 75154 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5 V supply; however, a built-in option allows operation from a 12 V supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode of operation, if the input voltage goes to zero, the output voltage will remain LOW or HIGH as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go HIGH regardless of the previous input condition.

The 75154 is characterized for operation from 0°C to 70°C.

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



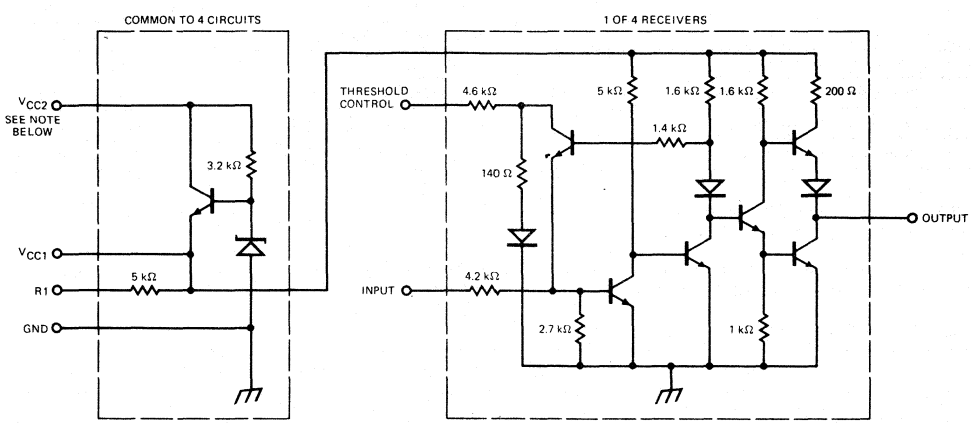
- **INPUT RESISTANCE . . . 3 kΩ TO 7 kΩ OVER FULL RS-232C VOLTAGE RANGE**
- **INPUT THRESHOLD ADJUSTABLE TO MEET FAIL-SAFE REQUIREMENTS WITHOUT USING EXTERNAL COMPONENTS**
- **BUILT-IN HYSTERESIS FOR INCREASED NOISE IMMUNITY**
- **INVERTING OUTPUT COMPATIBLE WITH DTL OR TTL**
- **OUTPUT WITH ACTIVE PULL-UP FOR SYMMETRICAL SWITCHING SPEEDS**
- **STANDARD SUPPLY VOLTAGES . . . 5 V OR 12 V**

ORDER INFORMATION

TYPE	PART NO.
75154	75154DC
75154	75154PC

11

EQUIVALENT CIRCUIT



Component values shown are nominal ⫽⫽⫽ ...Substrate

NOTE:
When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

ABSOLUTE MAXIMUM RATINGS

Normal Supply Voltage (Pin 15), V_{CC1} (Note 1)	7 V
Alternate Supply Voltage (Pin 16), V_{CC2} (Note 1)	14 V
Input Voltage (Note 1)	±25 V
Continous Total Power Dissipation (Note 2)	800 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperatures	
Molded DIP (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 60 s)	300°C

NOTES:
1. Voltage values are with respect to the network ground terminal.
2. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
Normal Supply Voltage (Pin 15), V_{CC1}	4.5	5	5.5	V
Alternate Supply Voltage (Pin 16), V_{CC2}	10.8	12	13.2	V
Input Voltage			±15	V
Normalized Fan Out from Each Output, N			10	
Operating Temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMENDED OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN (Note 3)	TYP†† (Note 3)	MAX (Note 3)	UNITS
V_{IH}	Input HIGH Voltage		1		3.0			V
V_{IL}	Input LOW Voltage		1				−3.0	V
V_{T+}	Positive-Going Threshold Voltage	Normal Operation	1		0.8	2.2	3.0	V
		Fail-Safe Operation			0.8	2.2	3.0	
V_{T-}	Negative-Going Threshold Voltage	Normal Operation	1		−3.0	−1.1	0	V
		Fail-Safe Operation			0.8	1.4	3.0	
$V_{T+} - V_{T-}$	Hysteresis	Normal Operation	1		0.8	3.3	6.0	V
		Fail-Safe Operation			0	0.8	2.2	
V_{OH}	Output HIGH Voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Output LOW Voltage		1	I_{OL} = 16 mA		0.23	0.4	V
R_I	Input Resistance		2	ΔV_I = −25 V to −14 V	3.0	5.0	7.0	kΩ
				ΔV_I = −14 V to −3 V	3.0	5.0	7.0	
				ΔV_I = −3 V to 3 V	3.0	6.0		
				ΔV_I = 3 V to 14 V	3.0	5.0	7.0	
				ΔV_I = 14 V to 25 V	3.0	5.0	7.0	
$V_{I(open)}$	Open-Circuit Input Voltage		3	I_I = 0	0	0.2	2.0	V
I_{OS}	Short-Circuit Output Current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply Current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply Current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

†Not more than one output should be shorted at a time.
‡All typical values are at V_{CC1} = 5 V, T_A = 25°C.

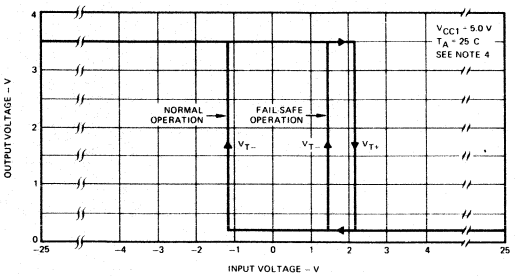
NOTE
3. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3 V is the maximum, the minimum limit is a more-negative voltage.

AC CHARACTERISTICS (V_{CC1} = 5.0 V, T_A = 25°C, N = 10)

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Output	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Output				20		ns
t_{TLH}	Transition Time, Low-to-High Output				9.0		ns
t_{THL}	Transition Time, High-to-Low Output				6.0		ns

TYPICAL CHARACTERISTICS

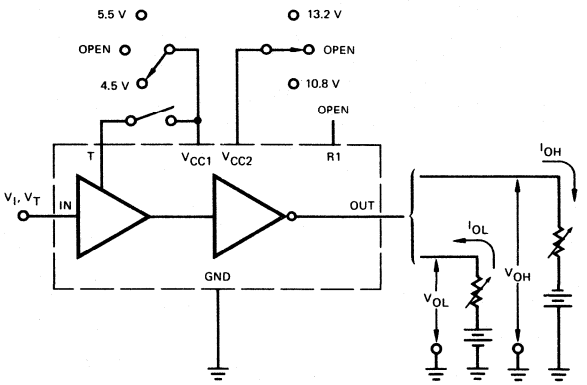
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



NOTE

4. For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open.

DC TEST CIRCUITS†



NOTES:
A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

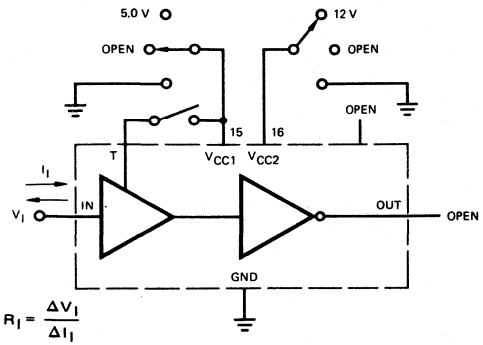
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEST TABLE

TEST	MEASURE	IN	T	OUT	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max, V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

Fig. 1 V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}.

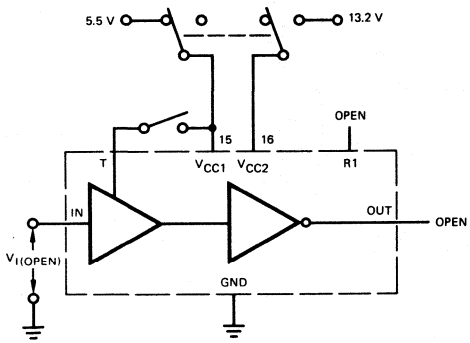
DC TEST CIRCUITS† (Cont'd)



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

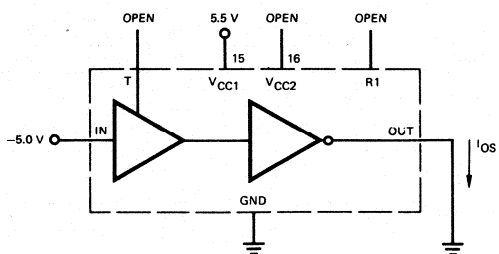
Fig. 2 R_I



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

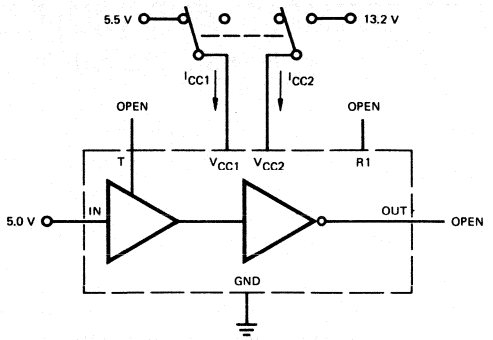
Fig. 3 $V_{I(open)}$



Each output is tested separately.

Fig. 4 I_{OS}

DC TEST CIRCUITS† (Cont'd)



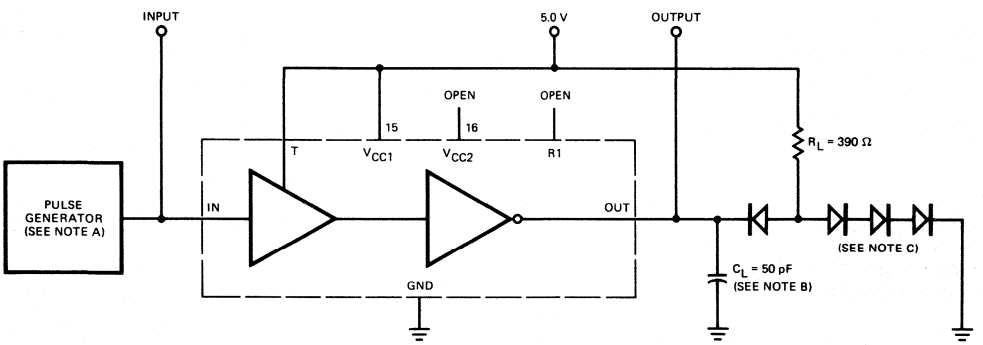
All four line receivers are tested simultaneously.

Fig. 5 I_{CC}

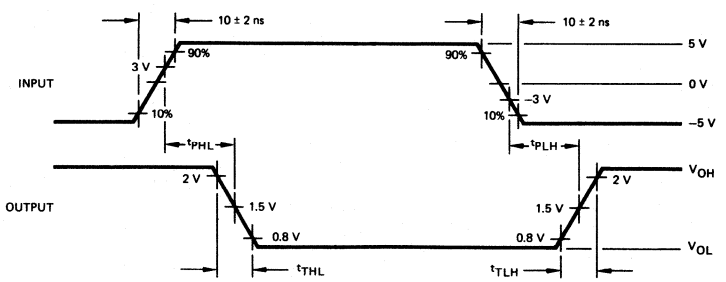
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

AC CHARACTERISTICS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064

75491•75491A•75492•75492A

MOS TO LED SEGMENT AND DIGIT DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

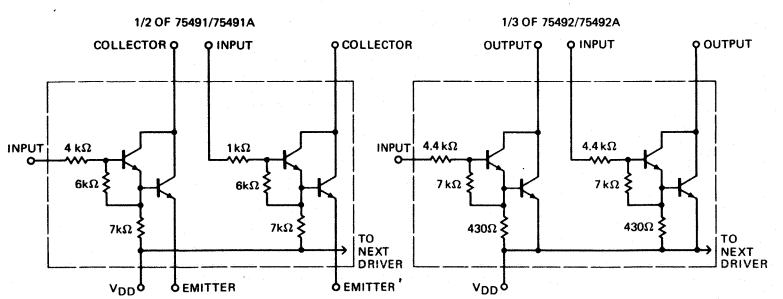
GENERAL DESCRIPTION — The 75491 and 75491A, LED Quad Segment Digit Drivers interface MOS signals to common cathode LED displays. High output current capability makes the devices ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

The 75492 and 75492A Hex LED/Lamp Drivers convert MOS signals to high output currents for LED display digit select or lamp select. The high output current capability makes the devices ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

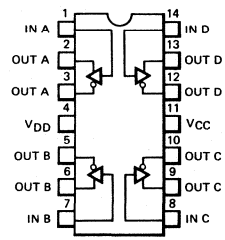
75491 • 75491A
- **50 mA SOURCE OR SINK CAPABILITY**
- **LOW INPUT CURRENTS FOR MOS COMPATIBILITY**
- **LOW STANDBY POWER**
- **FOUR HIGH GAIN DARLINGTON CIRCUITS**
- **10 V AND 20 V OPERATION**

75492 • 75492A
- **250 mA SINK CAPABILITY**
- **MOS COMPATIBLE INPUTS**
- **LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**
- **10 V AND 20 V OPERATION**

EQUIVALENT CIRCUITS



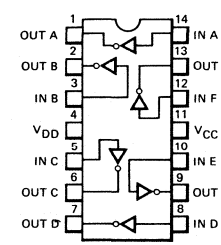
75491 • 75491A
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
75491	75491DC
75491	75491PC
75491A	75491ADC
75491A	75491APC

75492 • 75492A
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
75492	75492DC
75492	75492PC
75492	75492ADC
75492A	75492APC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (75491, 75492)	10 V
(75491A, 75492A)	20 V
Input Voltage (Note 1)	−5.0 to V_{SS}
Collector (Output) Voltage (Note 2) 75491, 75492	10 V
75491A, 75492A	20 V
Collector (Output) to Input Voltage 75491, 75492	10 V
75491A, 75492A	20 V
Emitter to Ground Voltage ($V_{IN} \geq 5.0$ V) 75491	10 V
75491A	20 V
Emitter to Input Voltage (75491, 75491A)	5.0 V
Continuous Collector Current (75491, 75491A)	50 mA
(75492, 75492A)	250 mA
Continuous V_{DD} Current (75492 and 75492A only)	600 mA
Continuous Total Power Dissipation (Note 3)	800 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

NOTES:
1. The input is the only device terminal which may be negative with respect to ground.
2. Voltage values are with respect to network ground terminal unless otherwise noted.
3. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C.

75491 • 75491A TRUTH TABLE

INPUT	OUTPUT E	OUTPUT C
L	L	H
H	H	L

75492 • 75492A TRUTH TABLE

INPUT	OUTPUT
L	H
H	L

11

75491 • 75491A

ELECTRICAL CHARACTERISTICS (V_{SS} = 10 V for 75491, V_{SS} = 20 V for 75491A, T_A = 0°C to 70°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
V_{CEL}	LOW Level Collector to Emitter Voltage	V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V, T_A = 25°C			0.9	1.2	V
		V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V			0.9	1.5	V
I_{CH}	Collector HIGH Current	V_{CH} = 10 V, 75491 V_{CH} = 20 V, 75491A	V_E = 0, V_{IN} = 0.7 V			100	μA
		V_{CH} = 10 V, 75491 V_{CH} = 20 V, 75491A	V_E = 0, I_{IN} = 40 μA			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V, 75491 V_{IN} = 20 V, 75491A	I_{OL} = 20 mA		2.0 4.0	3.3 6.6	mA
I_{ER}	Reverse Biased Emitter Current	I_C = 0, V_{IN} = 0, V_E = 5.0 V				100	μA
I_{SS}	Supply Current					1.0	mA

AC CHARACTERISTICS (V_{SS} = 7.5 V, T_A = 25°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time	R_L = 200 Ω, V_{INH} = 4.5 V C_L = 15 pF, V_E = 0		20		ns
t_{PLH}				100		ns

75492 • 75492A

ELECTRICAL CHARACTERISTICS (V_{SS} = 10 V for 75492, V_{SS} = 20 V for 75492A, T_A = 0°C to 70°C, unless otherwise specified)

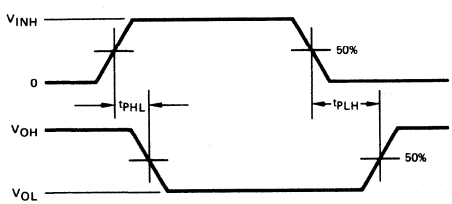
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output LOW Voltage	V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 250 mA, T_A = 25°C			0.9	1.2	V
		V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 250 mA			0.9	1.5	V
I_{OH}	Output HIGH Current	V_{OH} = 10 V, 75492	I_{IN} = 40 μA			200	μA
		V_{OH} = 20 V, 75492A					
		V_{OH} = 10 V, 75492	V_{IN} = 0.5 V			200	μA
		V_{OH} = 20 V, 75492A					
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V, 75492	I_{OL} = 20 mA			3.3	mA
		V_{IN} = 20 V, 75492A				6.6	mA
I_{SS}	Supply Current					1.0	mA

AC CHARACTERISTICS (V_{SS} = 7.5 V, T_A = 25°C)

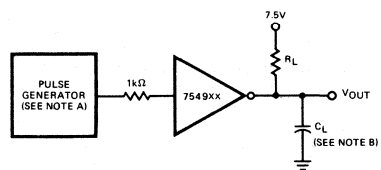
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time	R_L = 39 Ω, V_{IN} = 7.5 V C_L = 15 pF		30		ns
t_{PLH}				300		ns

NOTE:
All typical values are at T_A = 25°C.

WAVEFORMS

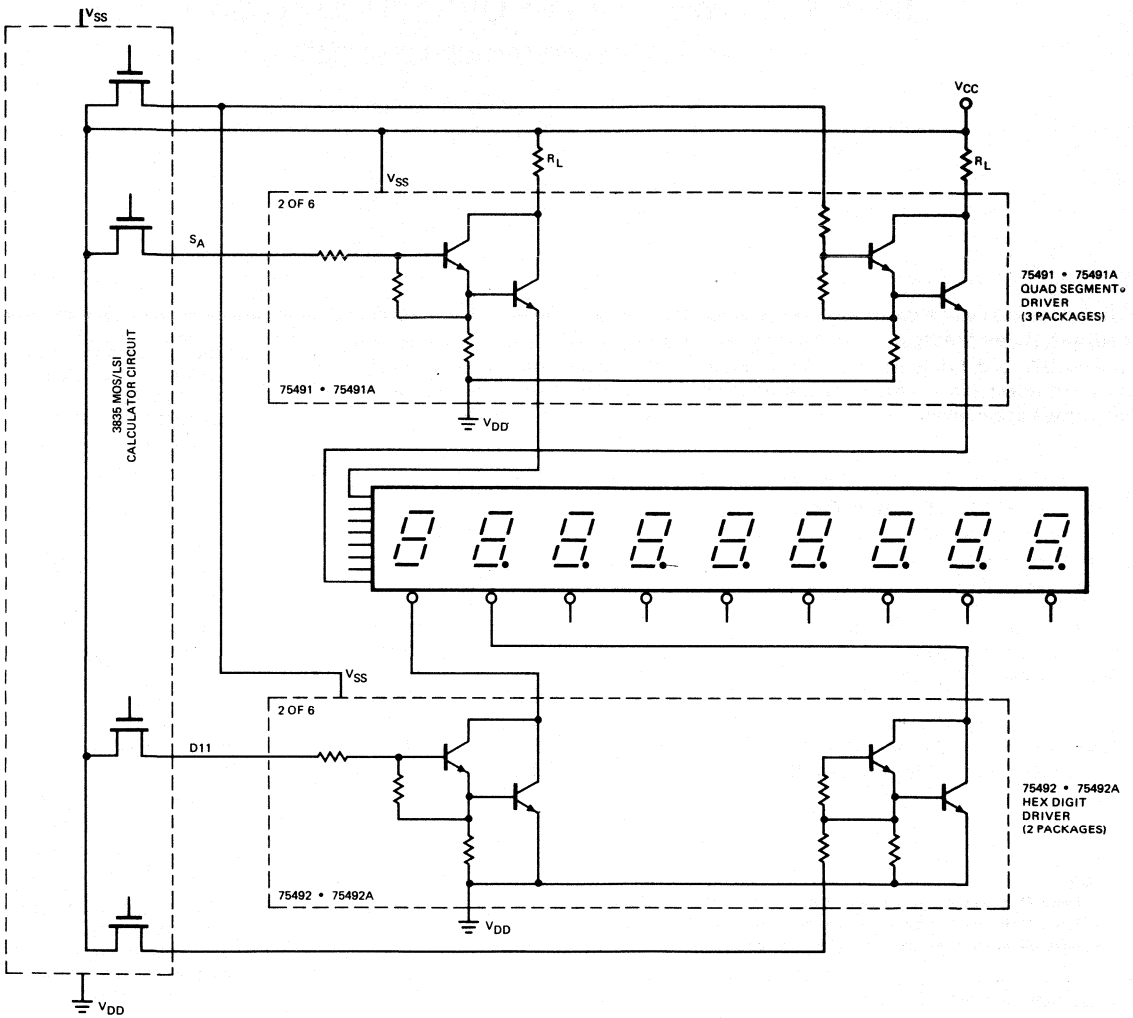


TEST CIRCUIT



NOTES:
A. The pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.
B. C_L includes probe and jig capacitance.

TYPICAL APPLICATION



INTERFACING BETWEEN MOS CALCULATOR CIRCUIT AND LED MULTI-DIGIT DISPLAY

This example of time multiplexing the individual digits in a visible display minimizes display circuitry. Up to twelve digits of a 7-segment display plus decimal point may be displayed using only two 75491/A and two 75492/A drivers.

SH2001 • SH2002

HIGH VOLTAGE HIGH CURRENT DRIVERS

FAIRCHILD INTEGRATED MICROSYSTEMS

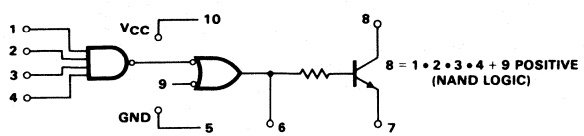
GENERAL DESCRIPTION – The SH2001 and SH2002 have inputs which are compatible with DTL and TTL logic levels. Their outputs are capable of driving cores, cables, lamps and relays. They feature fast switching speeds combined with high current and high voltage capabilities.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C	
Operating Temperature		
Military Grade	−55°C to +125°C	
Commercial Grade	0°C to +75°C	
Power Dissipation (Notes 1 and 2)	680 mW	
Input Reverse Current	1.0mA	
Supply Voltage (Pin 10)		
	SH2001	**SH2002**
Stand-off Voltage (Pin 8)	40 V	40 V
Peak Output Sink Current (Note 3)	1.0A	1.0A
Continuous Output Sink Current (Note 3)	500 mA	250 mA

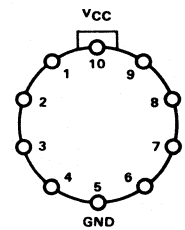
NOTES:
1. Above 25°C ambient temperature, derate linearly at 5.44 mW/°C.
2. Above 100°C case temperature, derate linearly at 13.6 mW/°C.
3. Power dissipation rating must not be exceeded.

FUNCTIONAL LOGIC DIAGRAM



Note: Pin numbers refer to both devices and both packages.

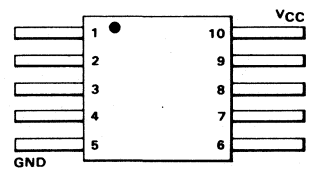
CONNECTION DIAGRAM
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5E
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
Commercial Grade	SH2001HC
	SH2002HC
Military Grade	SH2001HM
	SH2002HM

CONNECTION DIAGRAM
10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
Commercial Grade	SH2001FC
	SH2002FC
Military Grade	SH2001FM
	SH2002FM

GUARANTEED TEST SEQUENCE SH2001 AND SH2001C

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMIT MIN.	LIMIT MAX.
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL1}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL1}
3	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12					GND				V_R	V_{CCH}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18					GND		GND			V_{CCL}	V_6	V_{OH}	
19	GND				GND	I_{OL3}	GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22					GND					V_{PD}			t_{on}
23					GND					V_{PD}			t_{off}

FORCING FUNCTIONS (Temperature Range –55°C to +125°C)

SYMBOL	–55°C		+25°C		+125°C		UNITS
	SH2001	SH2002	SH2001	SH2002	SH2001	SH2002	
V_{CCL}	4.50	4.50	4.50	4.50	4.50	4.50	V
V_{CCH}	5.50	5.50	5.50	5.50	5.50	5.50	V
V_{PD}			5.00	5.00			V
V_{MAX}			8.00	8.00			V
V_{IL}	1.40	1.40	1.10	1.10	0.80	0.80	V
V_{IH}	2.10	2.10	1.90	1.90	1.70	1.70	V
V_R	4.00	4.00	4.00	4.00	4.00	4.00	V
V_F	0.00	0.40	0.00	0.40	0.00	0.40	V
I_{OL1}	250	150	250	150	250	150	mA
I_{OL2}	34.0	8.00	36.0	8.00	32.0	7.50	mA
I_{OL3}	8.0	—	8.0	—	8.0	—	mA
V_{OX}	40.0	40.0	40.0	40.0	40.0	40.0	V

FORCING FUNCTIONS (Temperature Range 0°C to +75°C)

SYMBOL	0°C		+25°C		+75°C		UNITS
	SH2001	SH2002	SH2001	SH2002	SH2001	SH2002	
V_{CCL}	5.00	5.00	5.00	5.00	5.00	5.00	V
V_{CCH}	5.00	5.00	5.00	5.00	5.00	5.00	V
V_{PD}			5.00	5.00			V
V_{MAX}			8.00	8.00			V
V_{IL}	1.20	1.20	1.10	1.10	.950	0.95	V
V_{IH}	2.00	2.00	1.90	1.90	1.80	1.80	V
V_R	4.00	4.00	4.00	4.00	4.00	4.00	V
V_F	0.45	0.45	0.45	0.45	0.50	0.50	V
I_{OL1}	250	150	250	150	250	150	mA
I_{OL2}	36.0	8.00	36.0	8.00	34.0	7.50	mA
I_{OL3}	8.0	—	8.0	—	8.0	—	mA
V_{OX}	40.0	40.0	40.0	40.0	40.0	40.0	V

TEST LIMITS (Temperature Range –55°C to +125°C)

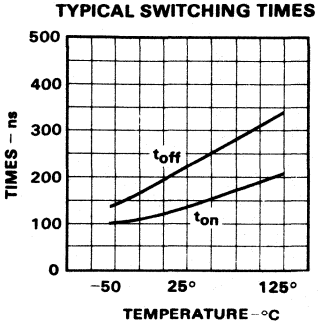
	–55°C		+25°C		+125°C		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
V_{OL1}		0.45		0.40		0.45	V
V_{OL2}		0.45		0.45		0.45	V
V_{OH}	2.20*		2.00		1.80		V
I_R				2.0		5.0	μA
$-I_F$		1.60		1.60		1.50	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				29.6			mA
t_{on} (SH2001 only)				160			ns
t_{off} (SH2001 only)				220			ns

*2.10 V for SH2002

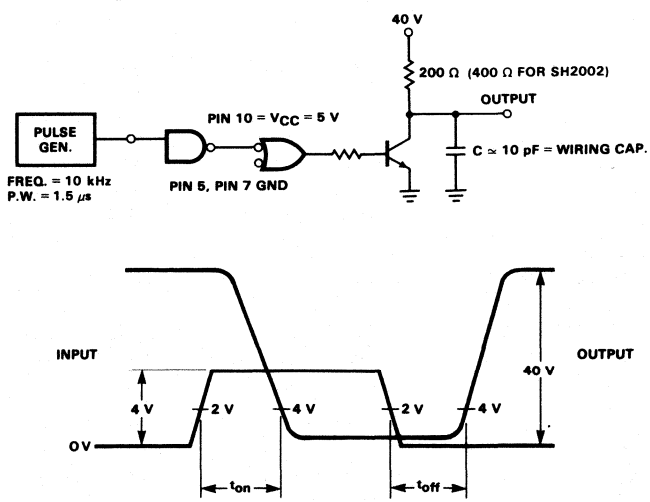
TEST LIMITS (Temperature Range 0°C to +75°C)

	0°C		+25°C		+75°C		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
V_{OL1}		0.45		0.45		0.5	V
V_{OL2}		0.45		0.45		0.5	V
V_{OH}	2.05		1.95		1.85		V
I_R				5.0		10.0	μA
$-I_F$		1.40		1.40		1.35	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				34.0			mA
t_{on} (SH2001only)				200			ns
t_{off} (SH2001only)				260			ns

TYPICAL SWITCHING TIMES

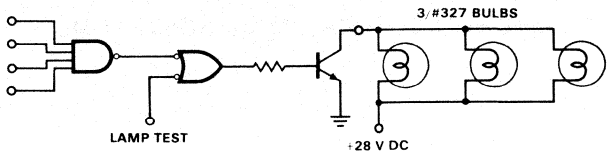


SWITCHING TIME TEST CONDITIONS

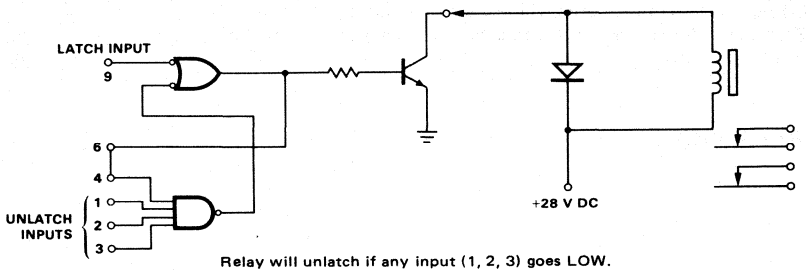


TYPICAL APPLICATIONS

LAMP DRIVER

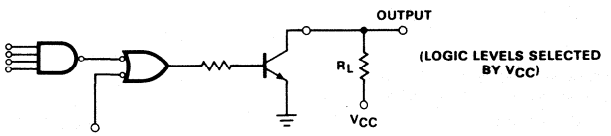


LATCHING RELAY



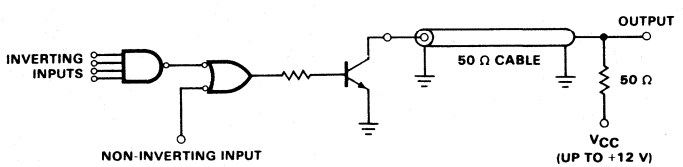
Relay will unlatch if any input (1, 2, 3) goes LOW.

DTL INTERFACE DRIVER



$R_L \geq 160\ \Omega$ AT $V_{CC} = 40$ V
$R_L \geq 80\ \Omega$ AT $V_{CC} = 20$ V

HIGH CURRENT LINE TRANSMITTER



Note: If only non-inverting input is used, one of the inverting inputs must be grounded.

SH2200 • SH2201

HIGH VOLTAGE HIGH CURRENT DRIVERS

FAIRCHILD INTEGRATED MICROSYSTEMS

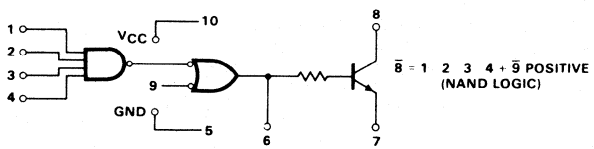
GENERAL DESCRIPTION – The SH2200 and SH2201 are high voltage, high current drivers designed for driving relays, lamps, cores, cables, etc. The input circuits are TTL and DTL compatible. Both devices feature a 3 A surge current rating and the SH2201 will withstand 100 V on the output.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	
Military Grade	−55°C to +125°C
Commercial Grade	0°C to +75°C
Power Dissipation (Notes 1 and 2)	680 mW
Input Reverse Current	1 mA
Supply Voltage (Pin 10)	8 V
Stand-off Voltage (Pin 8)	
SH2200	50 V
SH2201	100 V
Output Surge Current (Note 3)	3 A
Continuous Output Sink Current (Note 3)	500 mA

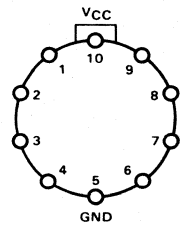
NOTES:
1. Above 25°C ambient temperature, derate linearly at 5.44 mW/°C.
2. Above 100°C case temperature, derate linearly at 13.6 mW/°C.
3. Power dissipation rating must not be exceeded.

FUNCTIONAL LOGIC DIAGRAM



Note: Above pin numbers apply to all package types, Top View

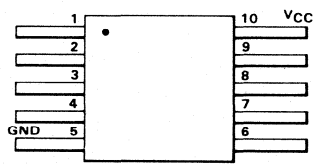
CONNECTION DIAGRAM
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5E
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
Commercial Grade	SH2200HC
	SH2201HC
Military Grade	SH2200HM
	SH2201HM

CONNECTION DIAGRAM
10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
Commercial Grade	SH2200FC
	SH2201FC
Military Grade	SH2200FM
	SH2201FM

GUARANTEED TEST SEQUENCE

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMITS MIN	LIMITS MAX
2	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
4		V_{IL}			GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
5			V_{IL}		GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
6				V_{IL}	GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
7	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
8		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
9			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
10				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
11				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
12	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
13	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
14	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
15	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
16					GND				V_R	V_{CC}	I_9		I_R
17	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
18	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
19	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
20	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
21				GND	GND				V_F	V_{CC}	I_9		$-I_F$
22					GND		GND			V_{CC}	V_6	V_{OH1}	
23	GND				GND	I_{OL3}	GND	V_{OX}		V_{CC}	I_8		I_{OX}
24					GND					V_{PD}	I_{10}		I_{PD}
25	GND				GND				GND	V_{MAX}	I_{10}		I_{MAX}
26	GND				GND		GND		GND	V_{CC}	I_{10}		I_{ON}

FORCING FUNCTIONS (Temperature Range 0°C to 70°C)

SYMBOL	0°C	+25°C	+75°C	UNITS
V_{CC}	5.0	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1.9	1.8	1.6	V
V_R	4.5	4.5	4.5	V
V_F	0.45	0.45	0.45	V
V_{OX}		50 (SH2201, 100 V)	50 (SH2201, 100 V)	V
I_{OL1}	500	500	500	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

TEST LIMITS (Temperature Range 0°C to 70°C)

SYMBOL	0°C	+25°C	+75°C	UNITS
V_{OL1}	0.6	0.6	0.6	V
V_{OL2}	0.45	0.45	0.45	V
V_{OH1}	1.95	1.85	1.65	V
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		12.2		mA
I_{MAX}		30		mA
I_{ON}		43		mA

11

FORCING FUNCTIONS (Temperature Range –55°C to +125°C)

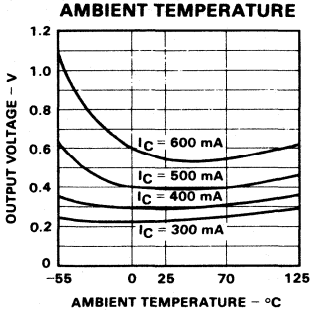
SYMBOL	–55°C	+25°C	+125°C	UNITS
V_{CC}	5.0	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.8	0.9	0.8	V
V_{IH}	2.0	1.7	1.4	V
V_R	4.5	4.5	4.5	V
V_F	0.4	0.4	0.4	V
V_{OX}		50 (SH2201, 100 V)	50 (SH2201, 100 V)	V
I_{OL1}	500	500	500	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

TEST LIMITS (Temperature Range –55°C to +125°C)

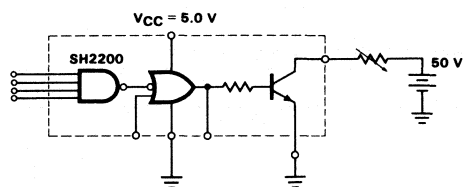
SYMBOL	–55°C	+25°C	+125°C	UNITS
V_{OL1}	0.8	0.6	0.7	V
V_{OL2}	0.4	0.4	0.4	V
V_{OH1}	2.05	1.75	1.45	V
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		11		mA
I_{MAX}		25		mA
I_{ON}		43		mA

PERFORMANCE CURVES

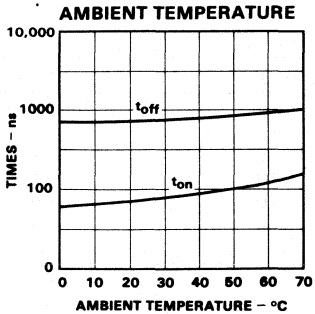
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



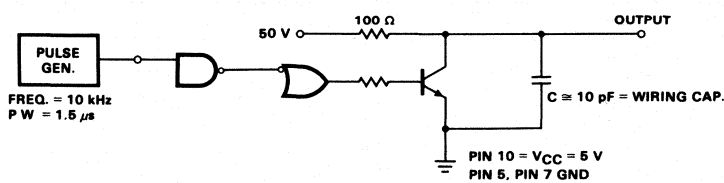
OUTPUT VOLTAGE TEST CIRCUIT



TYPICAL SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE

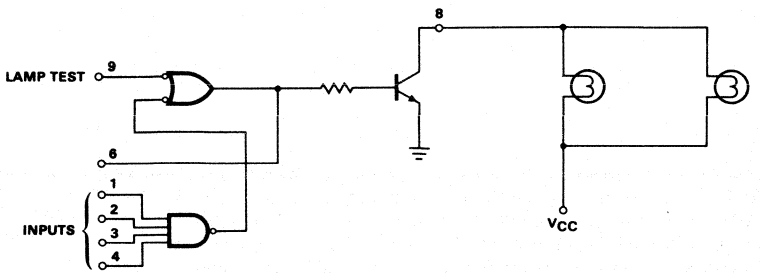


SWITCHING TIME TEST CIRCUIT

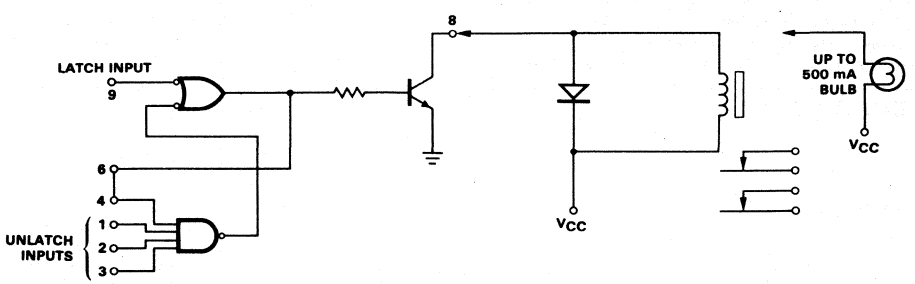


APPLICATIONS

LAMP DRIVER



LATCHING RELAY OR FAULT LAMP DRIVER



Relay will unlatch if any input (1, 2, 3) goes LOW.

SH3002 • SH3003

ANALOG SWITCHES

FAIRCHILD INTEGRATED MICROSYSTEMS

GENERAL DESCRIPTION – The SH3002 and SH3003 are analog switches each of which consists of a monolithic gate driving a pair of MOS switching devices. The SH3002 provides a SPDT function and the SH3003 has a DPST function. Typical applications include multiplexing, sample and hold circuits, scanning, chopping and A/D conversion systems.

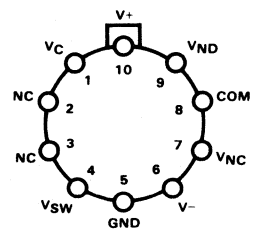
- **INPUTS TTL COMPATIBLE**
- **1 nA TYPICAL OFF LEAKAGE**
- **FAST SWITCHING**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	
Military Grade	−55°C to +125°C
Commercial Grade	0°C to +75°C
Power Dissipation (Notes 1 and 2)	500 mW
Voltage between Pin 10 and Pin 6	33 V
Voltage between Pin 10 and Ground	+18 V
Voltage between Pin 6 and Ground	−22 V
Voltage between Pins 1, 7, 8 or 9 (Note 4)	20 V
Voltage between Pin 4 and Ground	±6 V
Current through either switch	10 mA (continuous) 100 mA (peak) (Note 3)

NOTES:
1. Above 60°C ambient temperature, derate linearly at 5.5 mW/°C.
2. Above 114°C case temperature, derate linearly at 13.6 mW/°C.
3. Power dissipation rating must not be exceeded.
4. At no time may the voltages on Pins 1, 7, 8 and 9 exceed those on Pins 10 or 6.

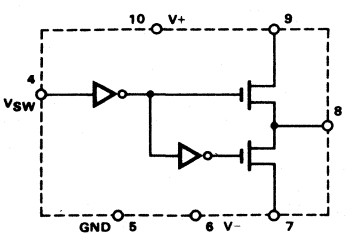
CONNECTION DIAGRAM
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5E
PACKAGE CODE H



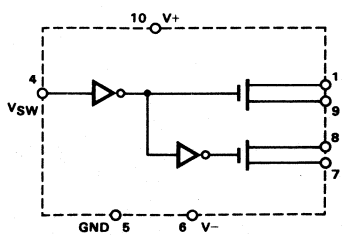
ORDER INFORMATION

TYPE	PART NO.
Commercial Grade	SH3002HC
	SH3003HC
Military Grade	SH3002HM
	SH3003HM

EQUIVALENT CIRCUITS



SH3002



SH3003

SWITCHING LOGIC

PIN 4	PIN 9	PIN 7
HIGH	CLOSED	OPEN
LOW	OPEN	CLOSED

MILITARY GRADE

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted).

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Switch Drive Voltage	V_{SWH}	T_A = 25°C	1.9			V
High Switch Drive Voltage	V_{SWH}	T_A = −55°C	2.2			V
High Switch Drive Voltage	V_{SWH}	T_A = 125°C	1.6			V
Low Switch Drive Voltage	V_{SWL}	T_A = 25°C			1.1	V
Low Switch Drive Voltage	V_{SWL}	T_A = −55°C			1.5	V
Low Switch Drive Voltage	V_{SWL}	T_A = 125°C			0.5	V
High Switch Input Current	I_{SWH}	V_{SW} = 5.0 V, V_{10} = 10 V, V_6 = −22 V		2.5	5.0	μA
Low Switch Input Current	I_{SWL}	V_{SW} = 0 V, V_{10} = 11 V, V_6 = −20 V		−1.0	−1.5	mA
Channel "On" Resistance	R_{ON}/CHANNEL	V_8 = GND, I_7 or I_9 = 100 μA		140	200	Ω
Channel "Off" Leakage	I_{OFF}	V_8 = ±10 V, V_7 = ±10 V, V_9 = ±10 V, T_A = 25°C		1.0	25	nA
		V_8 = ±10 V, V_7 = ±10 V, V_9 = ±10 V, T_A = 125°C			1.0	μA
Analog Peak Signal Input	V_{IN}				±10	V
Positive Supply Current	I_{10}	V_{SW} = 4.0 V, V_{10} = 11 V, V_6 = −22 V		4.0	8.0	mA
Positive Supply Current	I_{10}	V_{SW} = 0 V, V_{10} = 11 V, V_6 = −22 V			8.0	mA
Negative Supply Current	I_6	V_{SW} = 4.0 V, V_{10} = 11 V, V_6 = −22 V		3.0	6.5	mA
Turn-on Time (Pin 9)	t_{on+}	See Fig. 1 and 2		40	150	ns
Turn-off Time (Pin 7)	t_{off+}	See Fig. 1 and 2		360	500	ns
Turn-on Time (Pin 9)	t_{on-}	See Fig. 1 and 3		50	150	ns
Turn-off Time (Pin 7)	t_{off-}	See Fig. 1 and 3		300	500	ns
Turn-off Time (Pin 9)	t_{off+}	See Fig. 1 and 2		320	500	ns
Turn-on Time (Pin 7)	t_{on+}	See Fig. 1 and 2		200	350	ns
Turn-off Time (Pin 9)	t_{off-}	See Fig. 1 and 3		240	350	ns
Turn-on Time (Pin 7)	t_{on-}	See Fig. 1 and 3		210	350	ns

11

SWITCHING TEST CIRCUIT

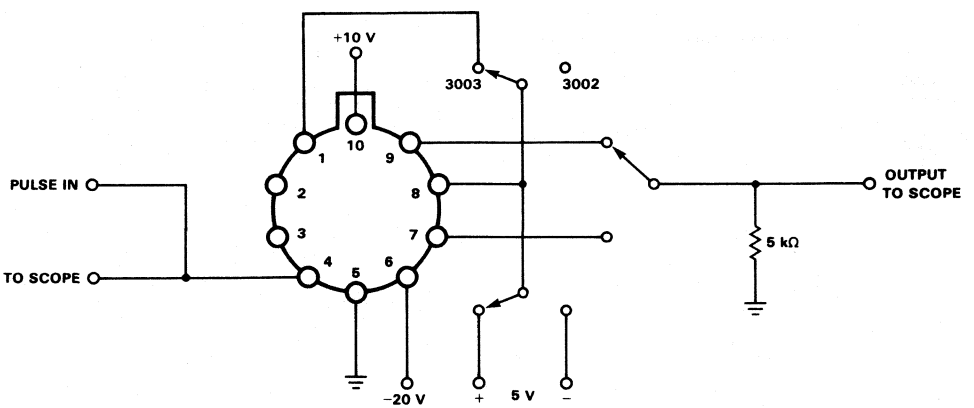


Fig. 1

COMMERCIAL GRADE

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted).

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Switch Drive Voltage	V_{SWH}	$T_A = 25°C$	1.9			V
High Switch Drive Voltage	V_{SWH}	$T_A = 0°C$	2.0			V
High Switch Drive Voltage	V_{SWH}	$T_A = 70°C$	1.7			V
Low Switch Drive Voltage	V_{SWL}	$T_A = 25°C$			1.1	V
Low Switch Drive Voltage	V_{SWL}	$T_A = 0°C$			1.3	V
Low Switch Drive Voltage	V_{SWL}	$T_A = 70°C$			0.8	V
High Switch Input Current	I_{SWH}	$V_{SW} = 5.0$ V, $V_{10} = 10$ V, $V_6 = -22$ V		2.5	5.0	μA
Low Switch Input Current	I_{SWL}	$V_{SW} = 0$ V, $V_{10} = 11$ V, $V_6 = -20$ V		−1.0	−1.5	mA
Channel "On" Resistance	R_{ON}/CHANNEL	V_8 = GND, I_7 or $I_9 = 100$ μA		140	200	Ω
Channel "Off" Leakage	I_{OFF}	$V_8 = \pm 10$ V, $V_7 = \pm 10$ V, $V_9 = \pm 10$ V, $T_A = 25°C$		1.0	25	nA
		$V_8 = \pm 10$ V, $V_7 = \pm 10$ V, $V_9 = \pm 10$ V, $T_A = 75°C$			1.0	μA
Analog Peak Signal Input	V_{IN}				±10	V
Positive Supply Current	I_{10}	$V_{SW} = 4.0$ V, $V_{10} = 11$ V, $V_6 = -22$ V		4.0	8.0	mA
Positive Supply Current	I_{10}	$V_{SW} = 0$ V, $V_{10} = 11$ V, $V_6 = -22$ V		4.0	8.0	mA
Negative Supply Current	I_6	$V_{SW} = 4.0$ V, $V_{10} = 11$ V, $V_6 = -22$ V		3.0	6.5	mA
Turn-on Time (Pin 9)	t_{on+}	See Fig. 1 and 2		75	200	ns
Turn-off Time (Pin 7)	t_{off+}	See Fig. 1 and 2		400	600	ns
Turn-on Time (Pin 9)	t_{on-}	See Fig. 1 and 3		75	200	ns
Turn-off Time (Pin 7)	t_{off-}	See Fig. 1 and 3		320	600	ns
Turn-off Time (Pin 9)	t_{off+}	See Fig. 1 and 2		360	600	ns
Turn-on Time (Pin 7)	t_{on+}	See Fig. 1 and 2		240	400	ns
Turn-off Time (Pin 9)	t_{off-}	See Fig. 1 and 3		280	400	ns
Turn-on Time (Pin 7)	t_{on-}	See Fig. 1 and 3		250	400	ns

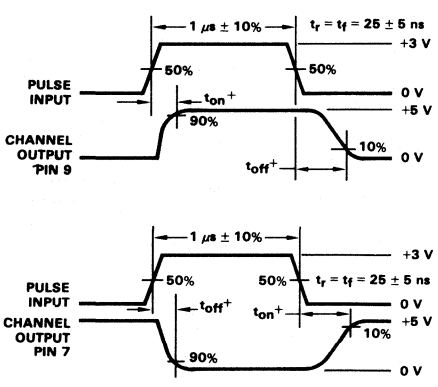


Fig. 2 (with +5 V on Pin 8)

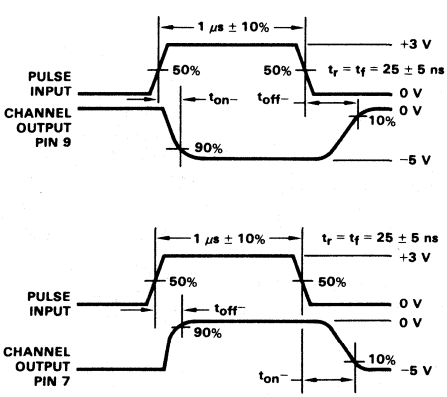
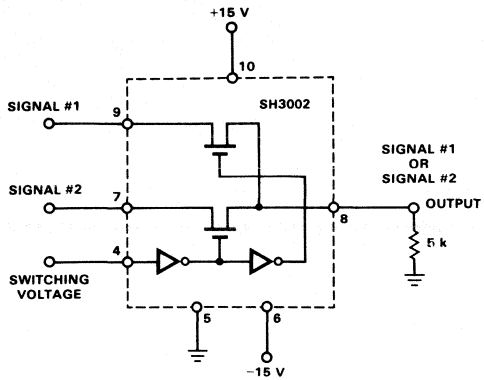


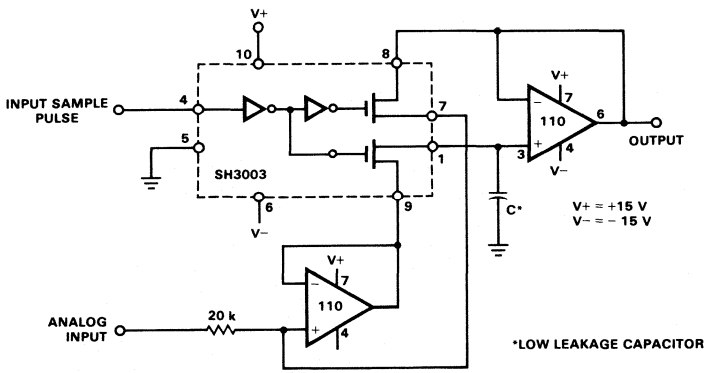
Fig. 3 (with −5 V on Pin 8)

TYPICAL APPLICATIONS

ANALOG SIGNAL MULTIPLEXER



SAMPLE AND HOLD CIRCUIT



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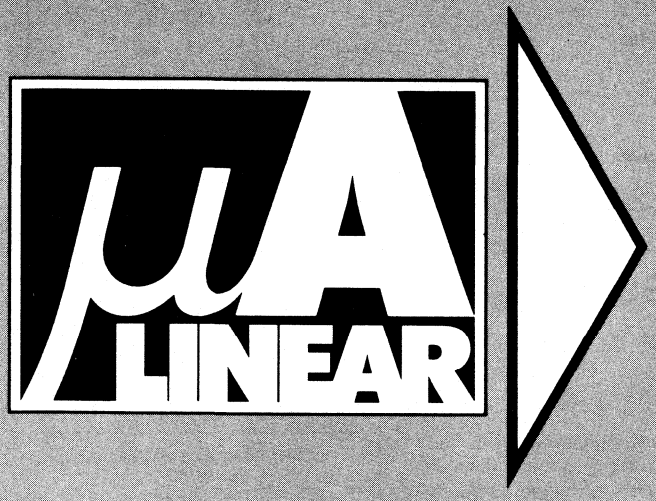


INTERFACE –
NEW PRODUCTS TO BE ANNOUNCED

NEW PRODUCTS

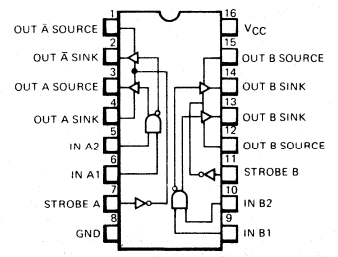
9634

DUAL 3-STATE DIFFERENTIAL LINE DRIVER

The 9634 Dual 3-state line driver is designed specifically to meet the EIA standard RS-422. It provides unipolar differential drive to twisted-pair or parallel-wire transmission lines. The outputs are similar to totem-pole TTL circuits but with the active pull-up and pull-down circuits split and brought out to adjacent pins. The active pull-up circuit is short circuit protected. In addition to the normal low impedance HIGH and LOW states, the 9634 outputs provide a high impedance OFF state, which is controlled by the output STROBE function. When the output control (STROBE) is LOW, the associated outputs are in high-impedance states neither driving nor loading the line permitting flexibility in party-line or buss applications. The 9634 is specified to drive 50 Ω terminated transmission lines at high speeds while guaranteeing a skew between outputs of less than 3 ns for applications requiring high performance drivers. The inputs are TTL and CMOS compatible.

- **High-Impedance Output State for Party-Line Applications**
- **Output Short Circuit Protection**
- **High Output Drive Capability for 50 Ω Transmission Lines**
- **Individual Output Controls**
- **Input Clamp Diodes**
- **Schottky Technology**
- **Complementary Outputs**
- **Meets the EIA-RS-422 Specification for a Balanced Driver**

CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



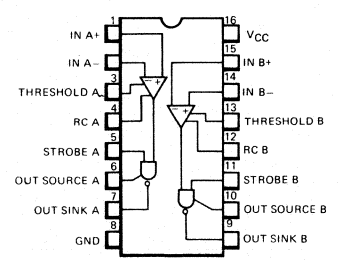
9635

DUAL DIFFERENTIAL LINE RECEIVER

The 9635 Dual Differential Line Receiver receives differential digital data from transmission lines and provides a TTL compatible output. Operating over the military and industrial temperature ranges, it requires a single 5 V supply and features threshold adjustment, ac response control, and an output strobe capability. This line receiver has a guaranteed input threshold accuracy of ±450 mV over a ±15 V common-mode range. The adjustable Threshold Control permits selection of the input switching threshold over a 0 to 5 V range with an external resistor divider, as well as the fixed thresholds of 0 and 1.4 V without external components. The response control function allows the noise immunity to be increased without introducing asymmetrical propagation delays or degrading output transition times. The output is a split totem-pole type, so both normal TTL and open-collector output operation is available as a wiring option.

- **Dual Channels**
- **Single 5 V Supply**
- **High Common-Mode Input-Voltage Range**
- **Choice of an Uncommitted Collector or Active Pull-up Output**
- **Output Strobe Capability**
- **Frequency Response Control**
- **Adjustable Input Threshold**
- **TTL Compatible Output**
- **High Input Impedance**

CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



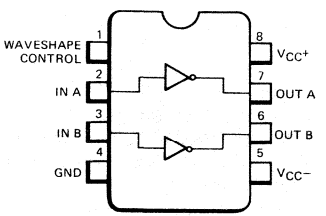
9636

DUAL SINGLE-ENDED LINE DRIVER

The 9636 Dual Single-Ended Line Driver meets the driver requirements of EIA standards RS-423 and RS-232C, provides TTL and CMOS compatible inputs and operates over the military and industrial temperature ranges. It also meets the CCITT standard X.26 driver requirements. The output slew rate can be controlled with a single external resistor; all outputs are short circuit protected and can withstand EIA-RS-232C fault conditions. The mini DIP provides high package density.

- **Output Short-Circuit Current Limiting**
- **Adjustable Slew Rate Limiting**
- **TTL and CMOS Input Compatible**
- **Meets EIA-RS-423 and RS-232C**
- **Meets CCITT X.26**
- **Wide Supply Range (± 9 V to ± 15 V)**

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



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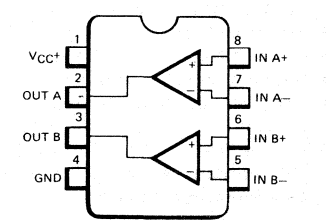
9637

DUAL DIFFERENTIAL LINE RECEIVER

The 9637 Dual Differential Line Receiver meets the receiver requirements of EIA standards RS-422 and RS-423 and provides a TTL compatible output while operating over the military and industrial temperature ranges. It uses a single 5 V power supply. This receiver has an input threshold accuracy of ±200 mV over a ±7 V common mode range. It also converts the CCITT X.26 and X.27 standard signals to TTL levels and can withstand RS-232C fault conditions. The mini DIP provides high package density.

- **Dual Channels**
- **Single 5 V Supply**
- **Satisfies EIA Standards RS-422 and RS-423**
- **Converts CCITT Standards X.26 and X.27 to TTL**
- **Withstands EIA Standard RS-232C Signal Levels**
- **High Common Mode Range**
- **High Input Impedance**
- **TTL Compatible Output**

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R

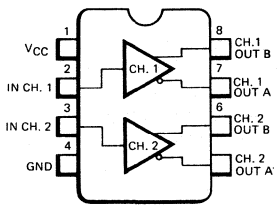


9638

DUAL HIGH SPEED DIFFERENTIAL LINE DRIVER

The 9638 is a Schottky, TTL-compatible Dual Channel Differential Line Driver, designed specifically to meet the EIA-RS-422 specifications. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The inputs are TTL and CMOS compatible. The outputs are similar to totem-pole TTL outputs, with active pull-up and pull-down. The device features a short-circuit protected active pull-up with low output impedance. The 9638 is specified to drive 50Ω transmission lines at high speed while guaranteeing a skew between outputs of less than 3 ns for applications requiring high performance line drivers. The mini DIP provides high package density.

CONNECTION DIAGRAM
8-LEAD DIP
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



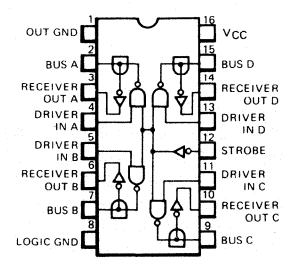
- **Single 5 V Supply**
- **Schottky Technology**
- **TTL and CMOS Compatible Inputs**
- **Output Short-Circuit Protection**
- **Input Clamp Diodes**
- **Complementary Outputs**
- **Minimum Output Skew**
- **High Output Drive Capability for 50Ω Transmission Lines**
- **Meets EIA-RS-422 Specifications**
- **Propagation Delay of Less Than 10 ns**

9640

QUAD TRANSCEIVER

The 9640 Quad Bus Transceiver is designed for use in instrumentation interface systems. It meets the recently adopted IEEE Standard Instrumentation Interface Specification. Each transceiver consists of a separate driver and receiver combination which can either drive an instrument bus or sense the logic state on the same bus line.

CONNECTION DIAGRAM
16-LEAD
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



- **Pin Compatible with Competitive Devices**
- **Schottky Process for Highest Speed**
- **Open Collector Bus Driver**
- **Receiver Input Hysteresis Provides Wide Noise Margin**
- **TTL Compatible Driver Input and Receiver Output**
- **Four Independent Driver/Receiver Channels**
- **Enable Feature Common to all Four Devices**
- **Circuit Meets Proposed IEEE and IEC Standard for Digital Interface for Programmable Instrumentation System Components**

9665 • 9666 • 9667
HIGH VOLTAGE, HIGH CURRENT DARLINGTON DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 9665, 9666 and 9667 are comprised of seven high voltage, high current npn Darlington transistor pairs. All units feature common emitter, open collector outputs. To maximize their versatility and effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter-base resistors for leakage.

The 9665 is a general purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. Input current limiting is done by connecting an appropriate discrete resistor to each input.

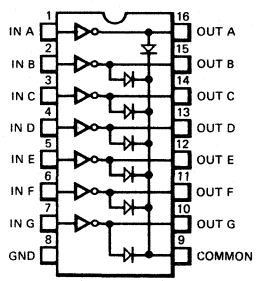
The 9666 version does away with the need for any external discrete resistors, since each unit has a resistor and a Zener diode in series with the input. The 9666 was specifically designed for direct interface from PMOS logic (operating at supply voltages from 14 to 25 V) to solenoids or relays.

The 9667 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V.

9665, 9666 and 9667 offer solutions to a great many interface needs, including solenoids, relays, lamps, small motors and LEDs. Applications requiring sink currents beyond the capability of a single output may be accomodated by paralleling the outputs.

- **SEVEN HIGH GAIN DARLINGTON TRANSISTOR PAIRS**
- **HIGH OUTPUT VOLTAGE (V_{CE} = 50 V)**
- **HIGH OUTPUT CURRENT (I_C = 350 mA)**
- **DTL, TTL, PMOS, CMOS COMPATIBLE**
- **SUPPRESSION DIODES FOR INDUCTIVE LOADS**

CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B 9B
PACKAGE CODE D P



11

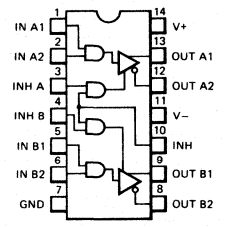
75112

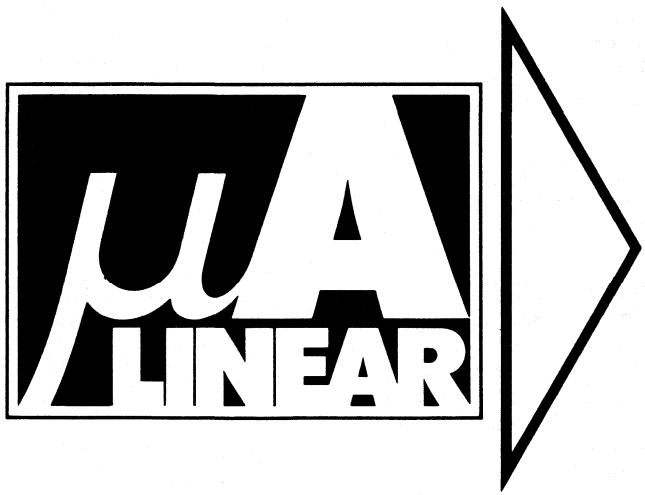
DUAL HIGH CURRENT LINE DRIVER

The 75112 Dual High Current Line Driver features two independent channels, each with a high current (24 mA) output stage. The output current can be switched between two terminals by a TTL input logic signal. The output current can also be turned off by either an independent or a common strobe input. The 75112 also provides improved strobe performance which prevents output transients under any combination of supply voltage power-down conditions.

- **High Speed**
- **Standard Supply Voltages**
- **High Output Current (18-30 mA)**
- **TTL Input Compatible**
- **Differential Outputs**
- **Single or Dual Channel Inhibit Performance**
- **No Line Transients During Power Up or Power Down When Inhibited**
- **Two Independent Channels**

CONNECTION DIAGRAM
14-Lead DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F





INDEX

GENERAL PURPOSE

LOW INPUT CURRENT/LOW DRIFT

INDEX

μAF155/A • μAF355/A
LOW SUPPLY CURRENT
μAF156/A • μAF356/A
WIDEBAND
μAF157/A • μAF357/A
WIDEBAND UNCOMPENSATED
MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

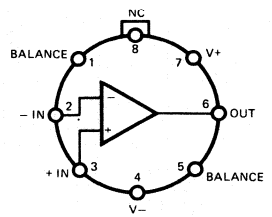
FAIRCHILD INTEGRATED CIRCUITS

GENERAL DESCRIPTION – These monolithic JFET input operational amplifiers incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

- **LOW INPUT BIAS CURRENT . . . 30 pA**
- **HIGH INPUT IMPEDANCE . . . $10^{12}\ \Omega$**
- **LOW INPUT OFFSET VOLTAGE . . . 2 mV**
- **LOW INPUT OFFSET VOLTAGE TEMPERATURE DRIFT . . . 5 μV/°C**
- **LOW INPUT NOISE CURRENT . . . 0.01 pA/$\sqrt{\text{Hz}}$**
- **HIGH COMMON MODE REJECTION RATIO . . . 100 dB**
- **LARGE DC VOLTAGE GAIN . . . 106 dB**

	μAF155	μAF156	μAF157	Units
• EXTREMELY FAST SETTLING TIME TO 0.01%	4	1.5	1.5	μs
• FAST SLEW RATE	5	15	75	V/μs
• WIDE GAIN BANDWIDTH (μAF157 AV_{MIN} = 5)	2.5	5	25	MHz
• LOW INPUT NOISE VOLTAGE	20	12	12	nV/$\sqrt{\text{Hz}}$
• LOW SUPPLY CURRENT	2	5	5	mA

CONNECTION DIAGRAM
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



Note: Lead 4 connected to case.

ORDER INFORMATION

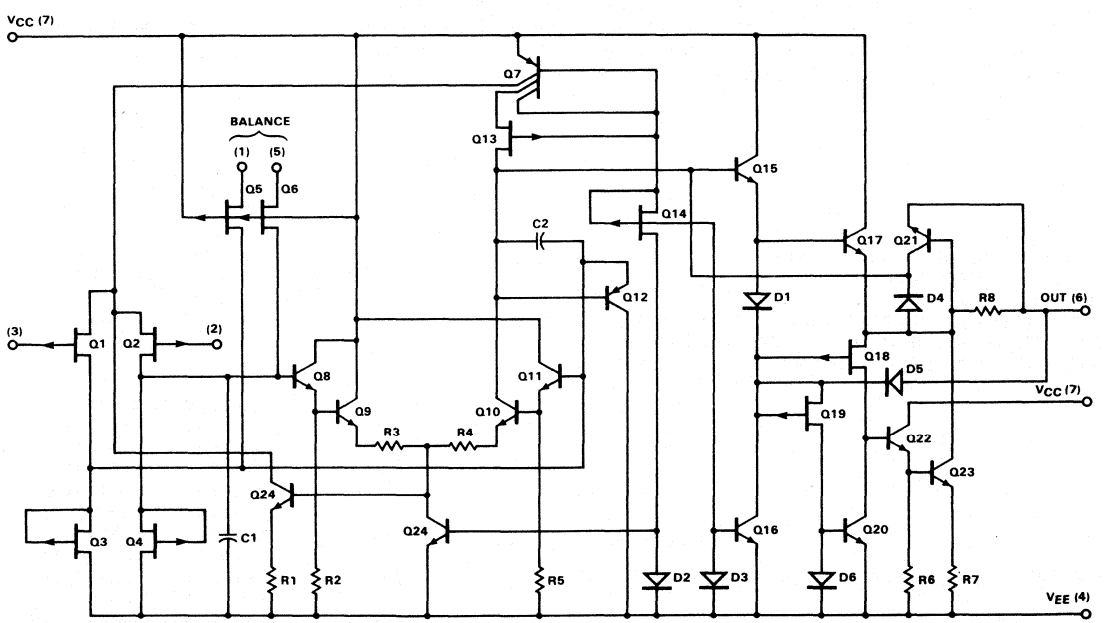
TYPE	PART NO.
μAF155	μAF155HM
μAF355	μAF355HC
μAF156	μAF156HM
μAF356	μAF356HC
μAF157	μAF157HM
μAF357	μAF357HC
μAF155A	μA155AHM
μAF355A	μAF355AHC
μAF156A	μAF156AHM
μAF356A	μAF356AHC
μAF157A	μAF157AHM
μAF357A	μAF357AHC

12

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μAF155/6/7 series, μAF355A/6A/7A series	±22 V
μAF355/6/7 series	±18 V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	
μAF155/6/7 series, μAF355A/6A/7A series	±40 V
μA355/6/7 series	±30 V
Input Voltage Range (Note 2)	
μAF155/6/7 series, μAF355A/6A/7A series	±20 V
μAF355/6/7 series	±16 V
Output Short Circuit Duration	Continuous
Operating Temperature Range	
μAF155/6/7 series	−55°C to +125°C
μAF355A/6A/7A series, μAF355/6/7 series	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 s)	300°C
Maximum Junction Temperature, $T_{J(MAX)}$	
μAF155/6/7 series	150°C
μAF355A/6A/7A series, μAF355/6/7 series	100°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: T_A = +25°C unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS	μAF155/156/157			μAF355/356/357			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{OS})	R_S = 50 Ω		3	5		3	10	mV
Average Input Offset Drift	R_S = 50 Ω		5			5		μV/°C
Change in Offset Drift with V_{OS} Adj.	R_S = 50 Ω (Note 6)		1			1		μV/°C/mV
Input Offset Current	T_J = 25°C (Note 4)		3	20		3	50	pA
Input Bias Current	T_J = 25°C (Note 4)		30	100		30	200	pA
Differential Input Resistance and Common Mode Input Resistance	T_J = 25°C		10^{12}			10^{12}		Ω
Large Signal Voltage Gain	V_S = ±15 V, R_L = 2 kΩ V_O = ±10 V	50	200		50	200		V/mV
The following specifications apply for T_C = −55°C to +125°C for μAF155/156/157 T_C = 0°C to 70°C for μAF355/356/357								
Input Offset Voltage	R_S = 50 Ω			7			13	mV
Input Offset Current				20			2	nA
Input Bias Current				50			8	nA
Large Signal Voltage Gain		25			15			V/mV
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ	±12	±13		±12	±13		V
Common Mode Voltage Range	V_S = ±15 V	±11	+15.1 −12		±10	±12	+15.1 −12	V
CMRR		85	100		85	100		dB
PSRR		85	100		85	100		dB

The following specifications apply for T_C = +25°C

PARAMETER	μAF155		μAF355		μAF156		μAF356		μAF157		μAF357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

PARAMETER	CONDITIONS	μAF155			μAF156			μAF157			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	V_S = ±15 V, A_V = +1 except A_V = 5 for μAF157 series		5			15			75		V/μs
Gain Bandwidth Product			2.5			5.0			25		MHz
Setting Time to 0.01% (Note 5)			4			1.5			1.5		μs
Equivalent Input Noise Voltage (e_n)	f = 100 Hz		25			15			15		$nV/\sqrt{Hz}$
	f = 1 kHz		20			12			12		$nV/\sqrt{Hz}$
Equivalent Input Noise Current (i_n)	f = 100 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
	f = 1 kHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Input Capacitance (C_{IN})			3			3			3		pF

12

ELECTRICAL CHARACTERISTICS: T_A = +25°C unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS	μAF155A/156A/157A			μAF355A/356A/357A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{OS})	R_S = 50 Ω			2.0			2.0	mV
Average Input Offset Drift	R_S = 50 Ω			5			5	μV/°C
Change in Offset Drift with V_{OS} Adj.	R_S = 50 Ω (Note 6)		1.0			1.0		μV/°C/mV
Input Offset Current	T_J = 25°C (Note 4)		3	10		3	10	pA
Input Bias Current	T_J = 25°C (Note 4)		30	50		30	50	pA
Differential Input Resistance and Common Mode Input Resistance	T_J = 25°C		10^{12}			10^{12}		Ω
Large Signal Voltage Gain	V_S = ±15 V, R_L = 2 kΩ V_O = ±10 V	50	200		50	200		V/mV
The following specifications apply for T_C = −55°C to +125°C for μAF155A/156A/157A T_C = 0°C to 70°C for μAF355A/356A/357A								
Input Offset Voltage	R_S = 50 Ω			2.5			2.3	mV
Input Offset Current				10			1	nA
Input Bias Current				25			5	nA
Large Signal Voltage Gain		25			25			V/mV
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ	±12	±13		±12	±13		V
Common Mode Voltage Range	V_S = ±15 V	±11	+15.1 −12		±11	+15.1 −12		V
CMRR		85	100		85	100		dB
PSRR		85	100		85	100		dB

The following specifications apply for T_C = +25°C

PARAMETER	CONDITIONS	μAF155A/355A		μAF156A/356A		μAF157A/357A		UNITS
		TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current		2	4	5	7	5	7	mA

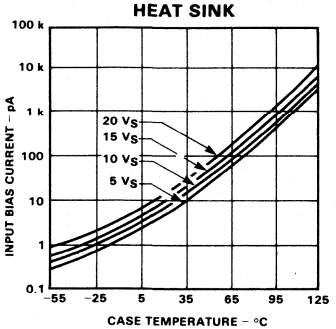
PARAMETER	CONDITIONS	μAF155A/355A			μAF156A/356A			μAF157A/357A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	V_S = ±15 V, A_V = +1 except A_V = 5 for μAF157 series	3	5		10	15		40	75		V/μs
Gain Bandwidth Product			2.5		4	5		15	25		MHz
Setting Time to 0.01% (Note 5)			4			1.5			1.5		μs
Equivalent Input Noise Voltage (e_n)	f = 100 Hz f = 1 kHz		25 20			15 12			15 12		nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$
Equivalent Input Noise Current (i_n)	f = 100 Hz f = 1 kHz		0.01 0.01			0.01 0.01			0.01 0.01		pA/$\sqrt{Hz}$ pA/$\sqrt{Hz}$
Input Capacitance (C_{IN})			3			3			3		pF

NOTES FOR ELECTRICAL CHARACTERISTICS:

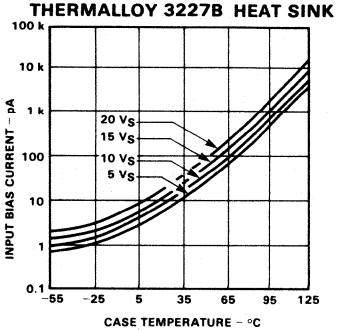
1. For operating at high temperature the package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. These specifications apply for ±15 V ≤ 20 V, unless otherwise stated for the μAF155/6/7 series.
   With the μAF355A/6A/7A series the specifications apply for ±15 V ≤ V_S ≤ ±20 V.
   For the μAF355/6/7 series the temperature specifications are the same as for the μAF355A/6A/7A series, but V_S = ±15 V.
4. The input bias currents are junction package currents which approximately double for every 10°C increase in the junction temperature (T_J). Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation (P_D). $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
5. Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the μAF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.10% of its final value from the time a 10 V step input is applied to the inverter. For the μAF157, A_V = 5, the feedback resistor from output to input is 2 kΩ and the output steps is 10 V.
6. For voltages across the external resistors used in the offset adjust circuitry of greater than a volt (R_{EXT} = 100 k), the Temperature Coefficient of the adjusted input offset voltage changes only a small amount (1 μV/C typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.

DC TYPICAL PERFORMANCE CHARACTERISTICS

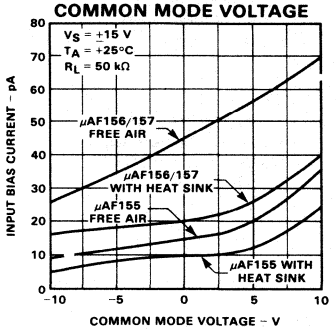
μAF155 INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE WITH THERMALLOY 3227B HEAT SINK



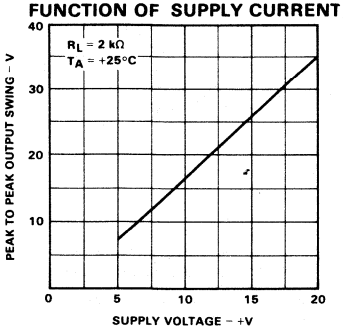
μAF156/157 INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE WITH THERMALLOY 3227B HEAT SINK



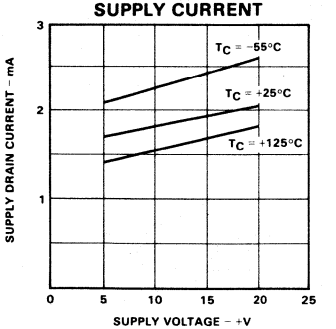
μAF155/156 INPUT BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



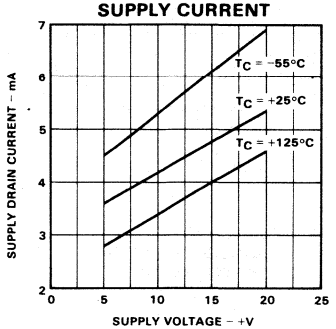
μAF155/156/157 MAXIMUM VOLTAGE SWING AS A FUNCTION OF SUPPLY CURRENT



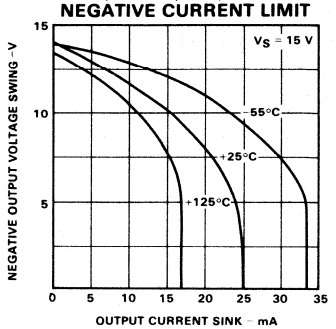
μAF155 SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



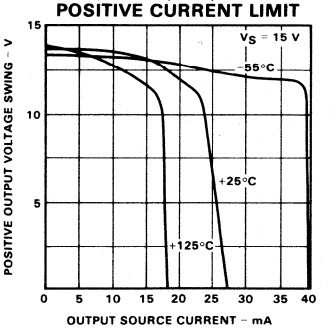
μAF156/157 SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



μAF155/156/157 NEGATIVE CURRENT LIMIT



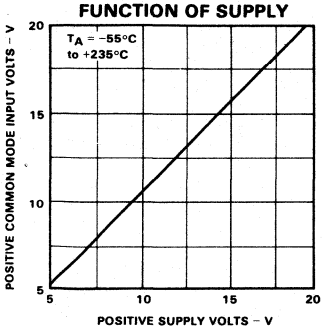
μAF155/156/157 POSITIVE CURRENT LIMIT



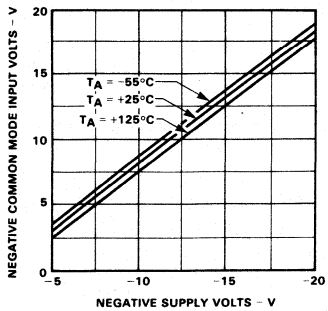
12

DC TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

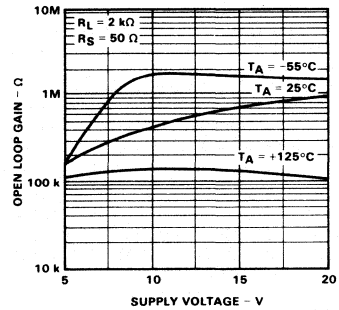
μAF155/156/157 POSITIVE COMMON MODE INPUT VOLTAGE AS A FUNCTION OF SUPPLY



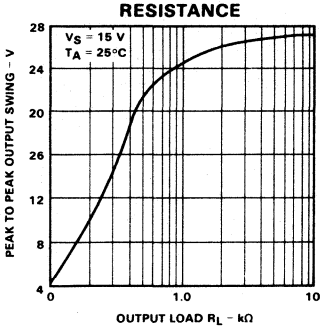
μAF155/156/157 NEGATIVE COMMON MODE INPUT VOLTAGE AS A FUNCTION OF SUPPLY



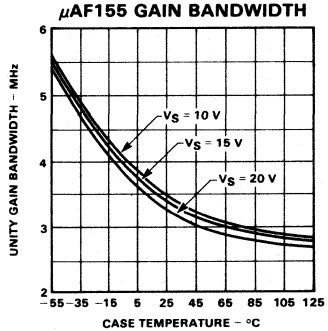
μAF155/156/157 LOOP GAIN AS A FUNCTION OF SUPPLY VOLTAGE



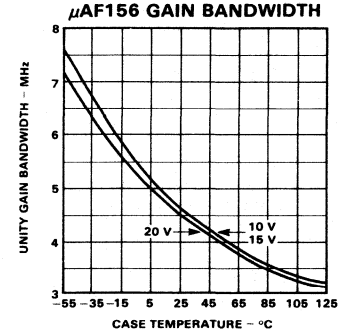
μAF155/156/157 VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



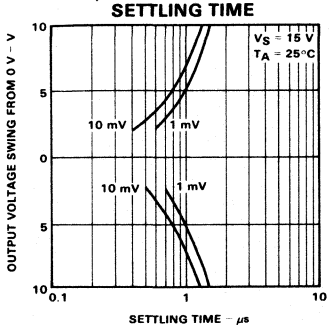
μAF155 GAIN BANDWIDTH



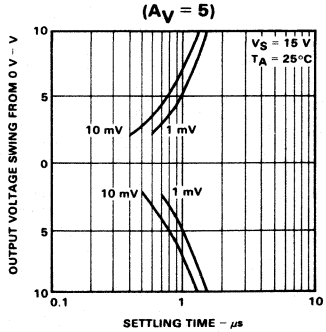
μAF156 GAIN BANDWIDTH



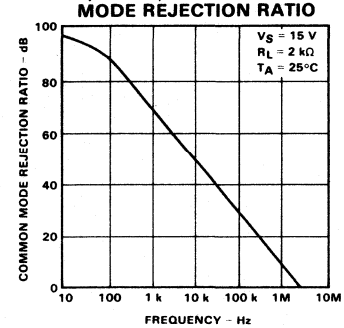
μAF156 INVERTER SETTLING TIME



μAF157 INVERTING SETTLING TIME (A_V = 5)

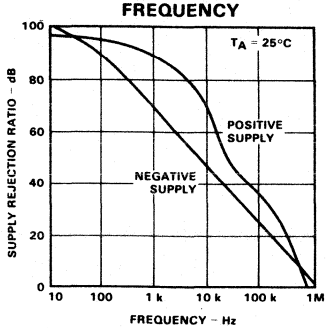


μAF155/156 COMMON MODE REJECTION RATIO

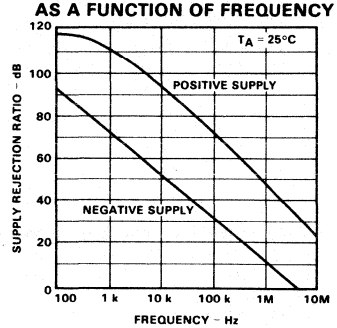


DC TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

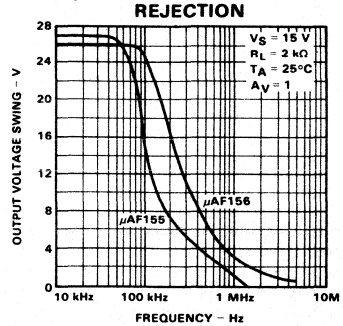
MAXIMUM UNDISTORTED SWING AS A FUNCTION OF FREQUENCY



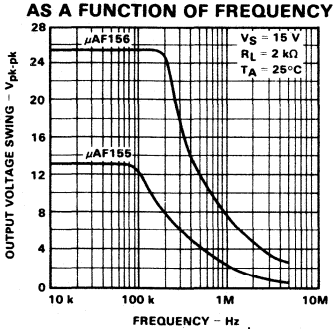
μAF156 SUPPLY REJECTION AS A FUNCTION OF FREQUENCY



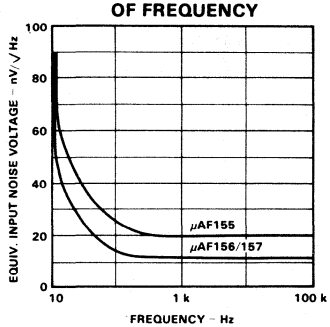
μAF155 POWER SUPPLY REJECTION



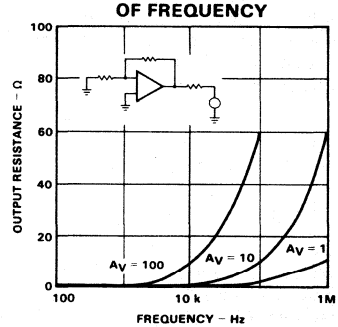
MAXIMUM OUTPUT SWING AS A FUNCTION OF FREQUENCY



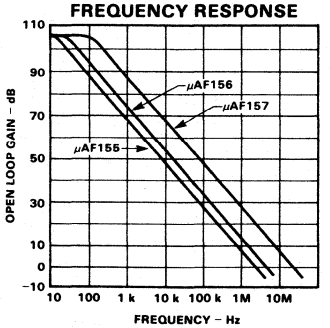
EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



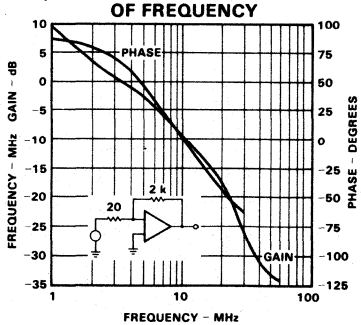
μAF155/156/157 OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



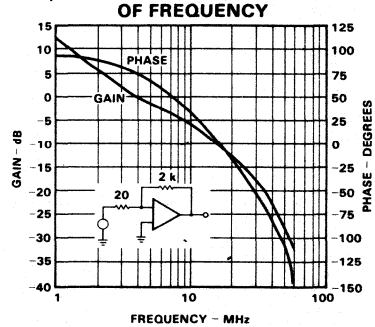
OPEN LOOP FREQUENCY RESPONSE



μAF155 GAIN AS A FUNCTION OF FREQUENCY



μAF156 GAIN AS A FUNCTION OF FREQUENCY



12

μA101 • μA201

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

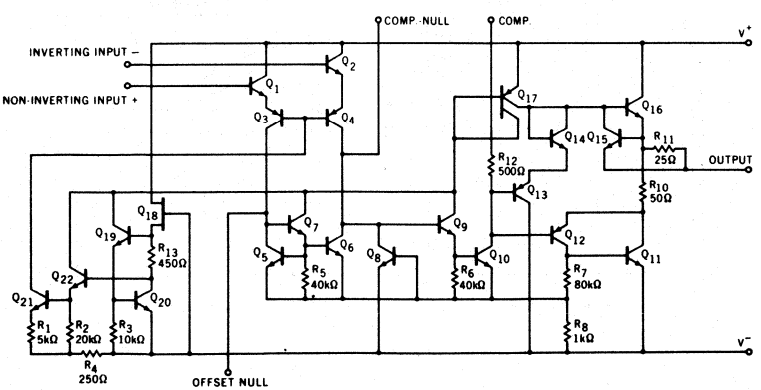
GENERAL DESCRIPTION — The 101 and 201 are General Purpose monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. The 101 and 201 compensate easily with a single external component. High common mode voltage range and absence of "latch-up" make the 101 and 201 ideal for use as voltage followers. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 101 and 201 are short-circuit protected and have the same pin configuration as the popular μA741, μA748 and μA709.

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

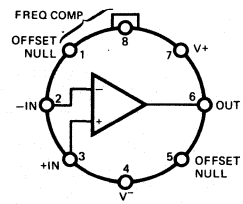
Supply Voltage	±22V
Internal Power Dissipation (Note 1)	
Metal Can	500mW
DIP	670mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Operating Temperature Range (Note 3)	
Military (μA101)	−55°C to +125°C
Commercial (μA201)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

EQUIVALENT CIRCUIT



Notes on following pages

CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

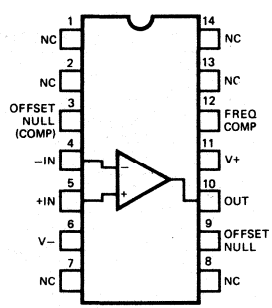


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA101	μA101H
μA201	μA201H

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA101	μA101D
μA201	μA201D

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS FOR μA101 ($\pm 5.0\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current			40	200	nA
Input Bias Current			120	500	nA
Input Resistance		300	800		kΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		V/mV
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		3.0		μV/°C
	$R_S \leq 10k\Omega$		6.0		μV/°C
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		100	500	nA
Average Temperature Coefficient of Input Offset Current	$+25°C \leq T_A \leq +125°C$ $-55°C \leq T_A \leq +25°C$		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		0.28	1.5	μA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = +15V$, $V_{OUT} = +10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB

NOTES

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the Metal Can and 8.3mW/°C for the DIP.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. The 101 ratings apply to +125°C case temperature or +75°C ambient temperature. The 201 ratings apply to case temperatures up to +70°C.

ELECTRICAL CHARACTERISTICS FOR μA201 ($\pm 5.0\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$			2.0	7.5	mV
Input Offset Current				100	500	nA
Input Bias Current				0.25	1.5	μA
Input Resistance			100	400		kΩ
Supply Current	$V_S = \pm 15V$			1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$		20	150		V/mV
The following specifications apply for $0°C \leq T_A \leq 70°C$:						
Input Offset Voltage	$R_S \leq 10\,k\Omega$				10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$			6.0		μV/°C
	$R_S \leq 10\,k\Omega$			10.0		μV/°C
Input Offset Current	$T_A = 70°C$			50	400	nA
	$T_A = 0°C$			150	750	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$			0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current	$T_A = 0°C$			0.32	2.0	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$		15			V/mV
Output Voltage Swing	$V_S = \pm 15V$	$R_L = 10\,k\Omega$	±12	±14		V
		$R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$		±12			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$		65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		70	90		dB

μA101A · μA201A · μA301A

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 101A, 201A and 301A are General Purpose monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. These integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents of the 101A, 201A, or 301A. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of "latch-up" coupled with internal short circuit protection make the 101A, 201A and 301A virtually foolproof.

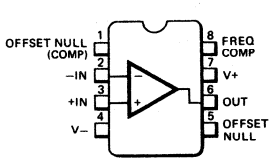
- **LOW OFFSET CURRENT AND VOLTAGE**
- **LOW OFFSET CURRENT DRIFT**
- **LOW BIAS CURRENT**
- **SHORT CIRCUIT PROTECTED**
- **LOW POWER CONSUMPTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military and Instrument (μA101A and μA201A)	±22V
Commercial (μA301A)	±18V
Internal Power Dissipation (Note 1)	
Metal Can	500mW
DIP	670mW
Flatpak	570mW
Mini DIP	310mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	–65°C to +150°C
Mini DIP	–55°C to +125°C
Operating Temperature Range	
Military (μA101A)	–55°C to +125°C
Instrument (μA201A)	–25°C to +85°C
Commercial (μA301A)	0°C to +70°C
Lead Temperature (Soldering)	
Metal Can, DIP and Flatpak (60 seconds)	300°C
Mini DIP (10 seconds)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

CONNECTION DIAGRAMS

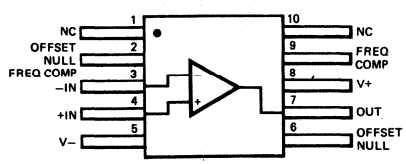
8-LEAD MINIDIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA301A	μA301AT

10-LEAD FLATPACK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



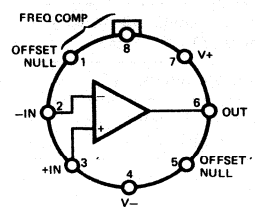
Available on special request.

ORDER INFORMATION

TYPE	PART NO.
μA101A	μA101AF
μA201A	μA201AF

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

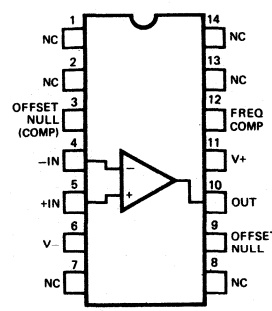


NOTE: Pin Connected to Case.

ORDER INFORMATION

TYPE	PART NO.
μA101A	μA101AH
μA201A	μA201AH
μA301A	μA301AH

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA101A	μA101AD
μA201A	μA201AD
μA301A	μA301AD

*Planar is a patented Fairchild process.

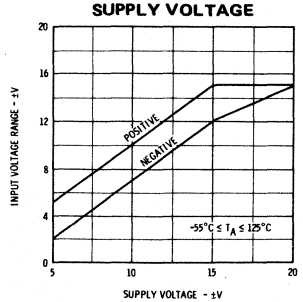
Notes on page 3

ELECTRICAL CHARACTERISTICS FOR μA101A and μA201A ($\pm 5.0\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified)

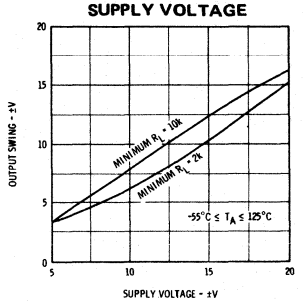
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		0.7	2.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			30	75	nA
Input Resistance		1.5	4.0		MΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		V/mV
The following specifications apply for $-55°C \leq T_A \leq +125°C$: (Note 4)					
Input Offset Voltage	$R_S \leq 10k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$+25°C \leq T_A \leq +125°C$		0.01	0.1	nA/°C
	$-55°C \leq T_A \leq +25°C$		0.02	0.2	nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	80	96		dB

GUARANTEED PERFORMANCE CURVES FOR μA101A AND μA201A

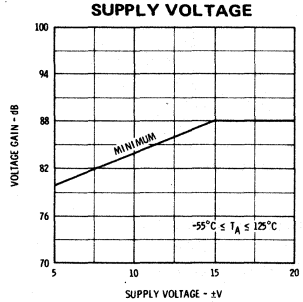
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



ELECTRICAL CHARACTERISTICS FOR μA301A ($\pm 5.0\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, C1 = 30 pF unless otherwise specified)

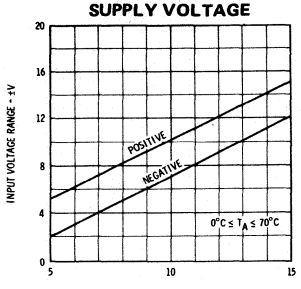
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	7.5	mV
Input Offset Current			3	50	nA
Input Bias Current			70	250	nA
Input Resistance		0.5	2		MΩ
Supply Current	$V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	25	160		V/mV
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage	$R_S \leq 10k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	μV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$		0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$		0.02	0.6	nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 10k\Omega$	±12	±14		V
	$V_S = \pm 15V, R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB

NOTES:
(1) Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. 101A and 201A ratings apply to +125°C case temperature or +75°C ambient temperature. 301A ratings apply for case temperatures to 70°C.
(4) All 201A specifications apply for $-25°C \leq T_A \leq +85°C$ unless otherwise specified.

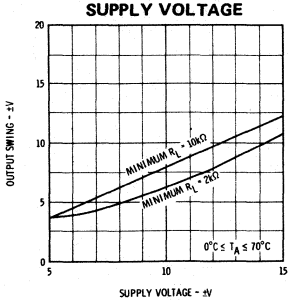
12

GUARANTEED PERFORMANCE CURVES FOR μA301A

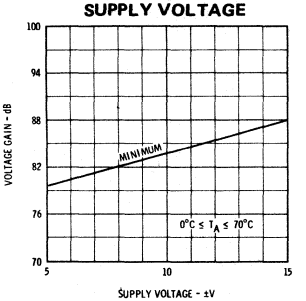
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

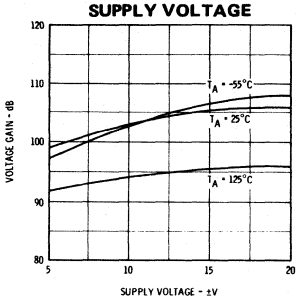


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

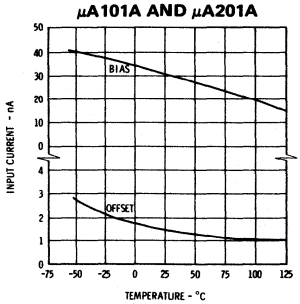


TYPICAL PERFORMANCE CURVES FOR μA101A, μA201A AND μA301A

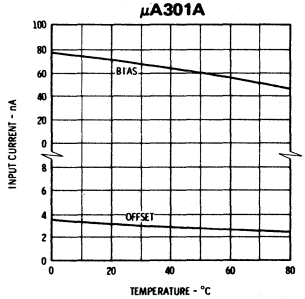
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



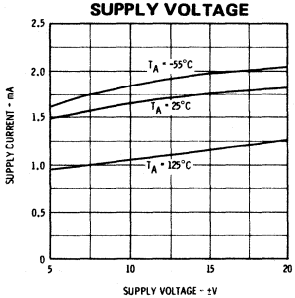
INPUT CURRENT AS A FUNCTION OF TEMPERATURE μA101A AND μA201A



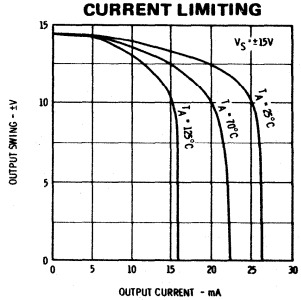
INPUT CURRENT AS A FUNCTION OF TEMPERATURE μA301A



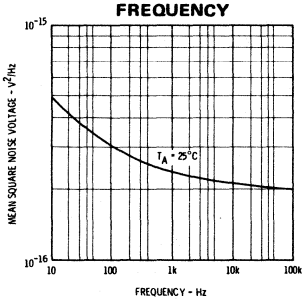
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



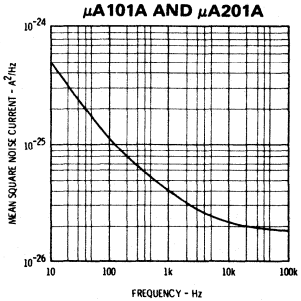
CURRENT LIMITING



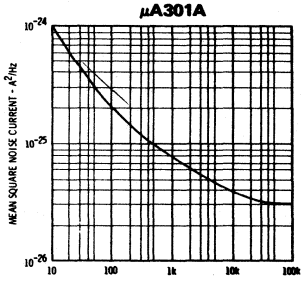
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



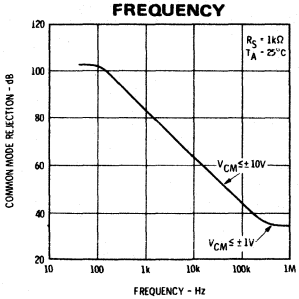
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY μA101A AND μA201A



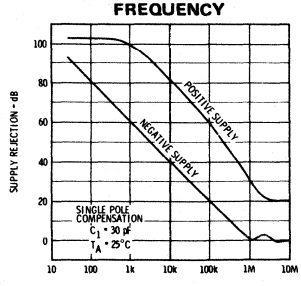
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY μA301A



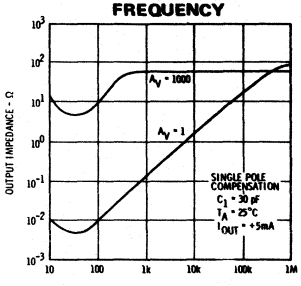
COMMON MODE REJECTION AS A FUNCTION OF FREQUENCY



POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY

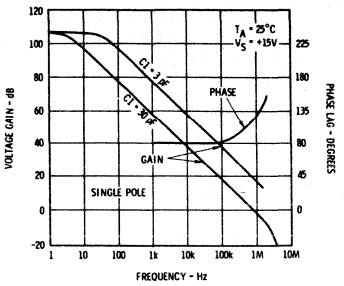


CLOSED LOOP OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

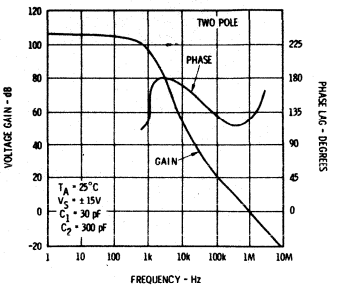


TYPICAL PERFORMANCE CURVES FOR μA101A, μA201A AND μA301A

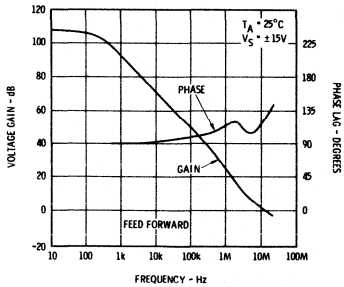
OPEN LOOP FREQUENCY RESPONSE



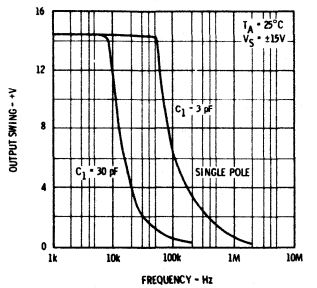
OPEN LOOP FREQUENCY RESPONSE



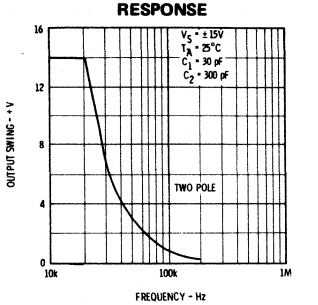
OPEN LOOP FREQUENCY RESPONSE



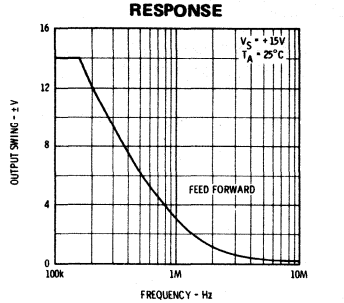
LARGE SIGNAL FREQUENCY RESPONSE



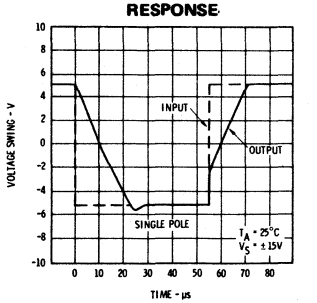
LARGE SIGNAL FREQUENCY RESPONSE



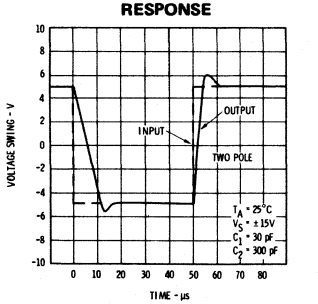
LARGE SIGNAL FREQUENCY RESPONSE



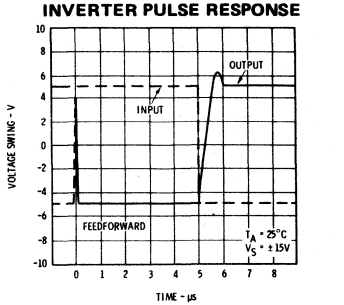
VOLTAGE FOLLOWER PULSE RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



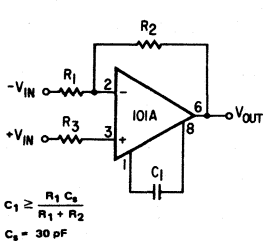
INVERTER PULSE RESPONSE



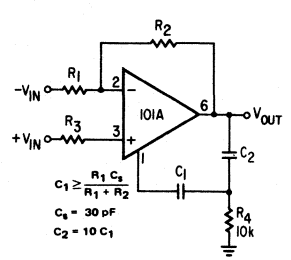
COMPENSATION CIRCUITS

(All pin numbers shown refer to 8-lead TO-5 package)

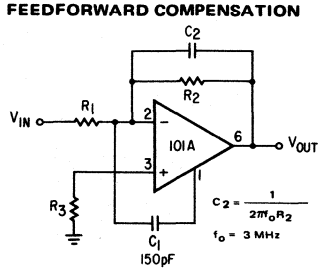
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION



FEEDFORWARD COMPENSATION

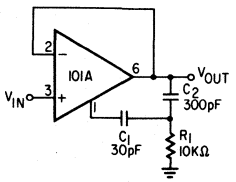


12

TYPICAL APPLICATIONS

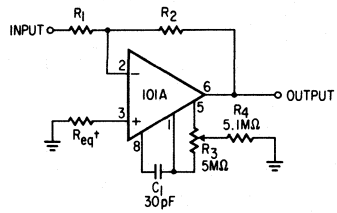
(All pin numbers shown refer to 8-lead TO-5 package)

FAST VOLTAGE FOLLOWER



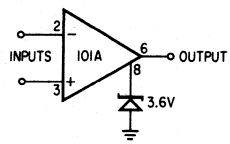
Power Bandwidth: 15 kHz
Slew Rate: 1 V/μs

INVERTING AMPLIFIER WITH BALACING CIRCUIT

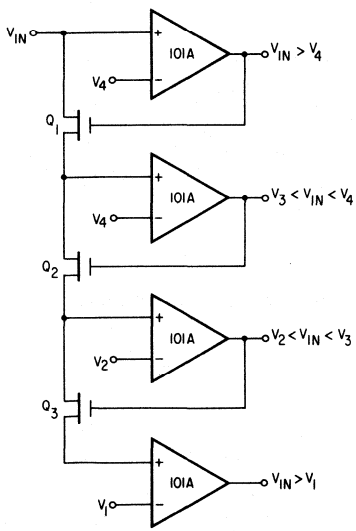


† May be zero or equal to parallel combination of R1 and R2 for minimum offset.

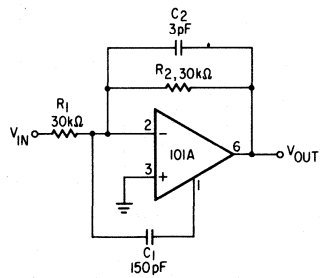
VOLTAGE COMPARATOR FOR DRIVING DTL OR TTL INTEGRATED CIRCUITS



MULTIPLE APERTURE WINDOW DISCRIMINATOR

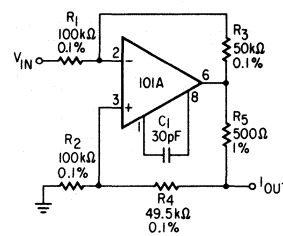


FAST SUMMING AMPLIFIER



Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

BILATERAL CURRENT SOURCE

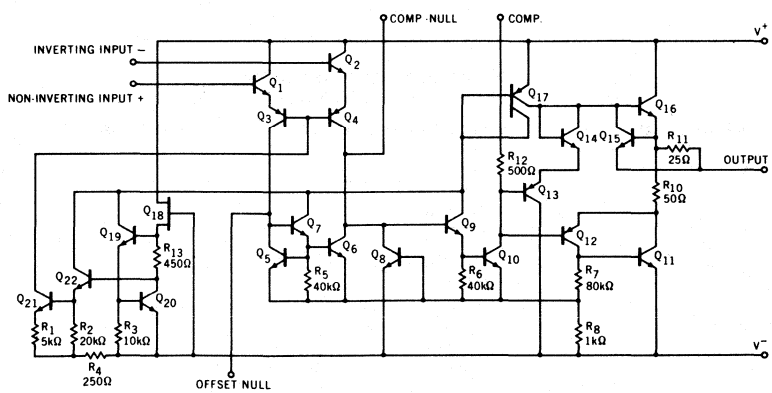


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$$

$R_3 = R_3 + R_5$

$R_1 = R_2$

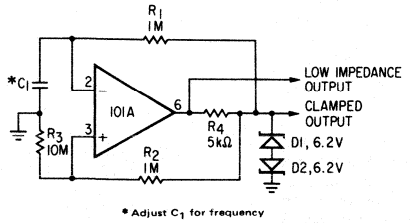
EQUIVALENT CIRCUIT



TYPICAL APPLICATIONS (Cont'd)

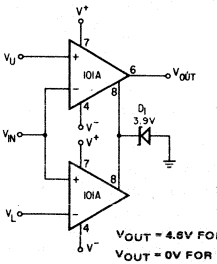
(All pin numbers shown refer to 8-lead TO-5 package)

LOW FREQUENCY SQUARE WAVE GENERATOR



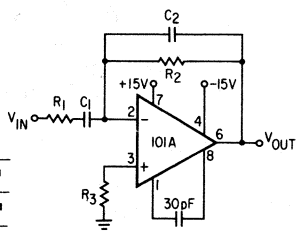
* Adjust C_1 for frequency

DOUBLE ENDED LIMIT DETECTOR



V_{OUT} = 4.6V FOR $V_L \leq V_{IN} \leq V_U$
V_{OUT} = 0V FOR $V_{IN} < V_L$ OR $V_{IN} < V_U$

PRACTICAL DIFFERENTIATOR

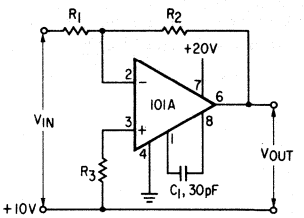


$f_c = \frac{1}{2\pi R_2 C_1}$

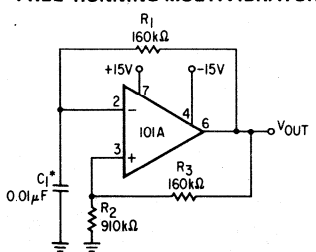
$f_h = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2}$

$f_c < f_h < f_{unity\ gain}$

CIRCUIT FOR OPERATING WITHOUT A NEGATIVE SUPPLY

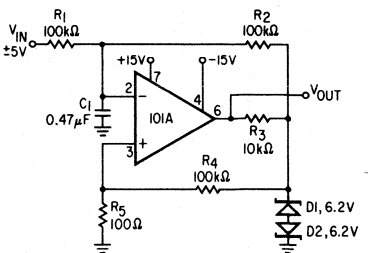


FREE-RUNNING MULTIVIBRATOR

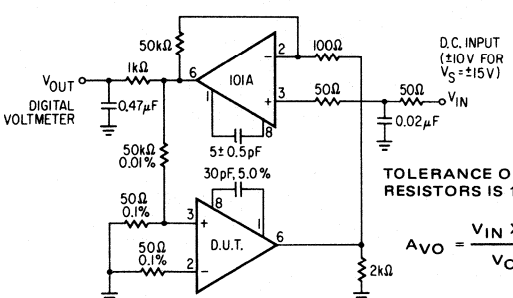


*Chosen for oscillation at 100 Hz

PULSE WIDTH MODULATOR



GAIN TEST CIRCUIT



TOLERANCE OF ALL UNMARKED RESISTORS IS 1%

$$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}} = \frac{10 \times 10^3}{V_{OUT}} \quad \text{FOR } \pm 10V \text{ INPUT}$$

μA102 • μA302 • μA110 • μA310

VOLTAGE FOLLOWERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

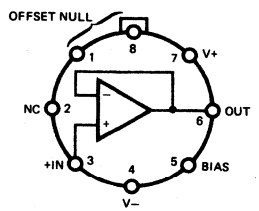
GENERAL DESCRIPTION – The 102/302 and 110/310 are monolithic Operational Amplifiers internally connected as unity gain non-inverting amplifiers. They are constructed using the Fairchild Planar* epitaxial process. These circuits are ideal for such applications as fast sample and hold circuits, active filters, or as general purpose buffers. Super-beta transistors are used allowing the devices to operate at very low input currents without sacrificing speed. They may be used interchangeably with the 101 and the μA741 in voltage follower applications. The 110/310 are suggested for new designs and are direct replacements for the 102/302. They feature lower offset voltage, drift, bias current, noise, plus higher speed and a wider operating voltage range.

- **HIGH SLEW RATE – 30 V/μs**
- **LOW INPUT CURRENT**
- **INTERNALLY COMPENSATED**
- **PLUG-IN REPLACEMENT FOR BOTH THE 101 AND μA741 VOLTAGE FOLLOWER APPLICATIONS**
- **WIDE RANGE OF SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15 V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA102, μA310)	−55°C to +125°C
Commercial (μA302, μA310)	0°C to +70°C
Lead Temperature (soldering, 60 seconds)	300°C

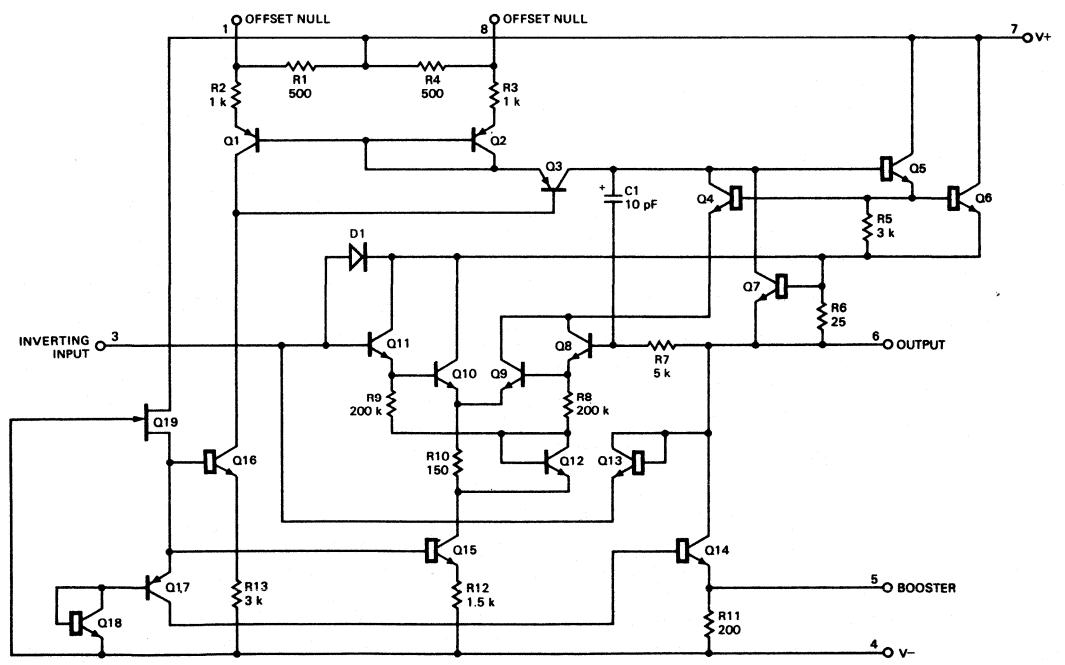
CONNECTION DIAGRAM
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA102	μA102M
μA302	μA302C
μA110	μA110M
μA310	μA310C

EQUIVALENT CIRCUIT



See notes on following pages

*Planar is a patented Fairchild process.

μA102

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, $C_L \leq$ 100 pF, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Voltage			2.0	5.0	mV
Average Temperature Coefficient of Offset Voltage			6.0		μV/°C
Input Current			3.0	10	nA
Input Resistance		10^{10}	10^{12}		Ω
Voltage Gain	$R_L \geq$ 10 kΩ	0.999	0.9996		
Output Resistance			0.8	2.5	Ω
Output Voltage Swing (Note 4)	$R_L \geq$ 8 kΩ	±10	±13		V
Supply Current			3.5	5.5	mA
Positive Supply Rejection		60			dB
Negative Supply Rejection		70			dB
Input Capacitance				3.0	pF
Offset Voltage	$-55°C \leq T_A \leq 125°C$			7.5	mV
Input Current	T_A = 125°C		3.0	10	nA
	T_A = −55°C		30	100	nA
Voltage Gain	$-55°C \leq T_A \leq 125°C$, $R_L \geq$ 10 kΩ	0.999			
Output Voltage Swing	$R_L \geq$ 10 kΩ	±10			V
Supply Current	T_A = 125°C		2.6	4.0	mA

μA302

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, $C_L \leq$ 100 pF, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Voltage			5.0	15	mV
Average Temperature Coefficient of Offset Voltage			20		μV/°C
Input Current			10	30	nA
Input Resistance		10^{9}	10^{12}		Ω
Voltage Gain	$R_L >$ 8 kΩ	0.9985	0.9995	1.000	
Output Resistance			0.8	2.5	Ω
Output Voltage Swing (Note 4)	$R_L \geq$ 8 kΩ	±10			V
Supply Current			3.5	5.5	mA
Positive Supply Rejection		60			dB
Negative Supply Rejection		70			dB
Input Capacitance			3.0		pF
Offset Voltage	$0°C \leq T_A \leq 70°C$			20	mV
Input Current	T_A = 70°C		3.0	15	nA
	T_A = 0°C		20	50	nA

μA110

ELECTRICAL CHARACTERISTICS ($\pm 5\ V \leq V_S \leq \pm 18\ V$, $-55°C < T_A \leq 125°C$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		1.5	4.0	mV
Input Bias Current	$T_A = 25°C$		1.0	3.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		Ω
Input Capacitance			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15\ V$ $V_{OUT} = \pm 10\ V$, $R_L = 8\ k\Omega$	0.999	0.9999		
Output Resistance	$T_A = 25°C$		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5	mA
Input Offset Voltage				6.0	mV
Offset Voltage Temperature Drift	$-55°C \leq T_A \leq 85°C$		6.0		μV/°C
	$T_A = 125°C$		12		μV/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$ $R_L = 10\ k\Omega$	0.999			
Output Voltage Swing (Note 4)	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±10			V
Supply Current	$T_A = 125°C$		2.0	4.0	mA
Supply Voltage Rejection Ratio	$\pm 5\ V \leq V_S \leq \pm 18\ V$	70	80		dB

μA310

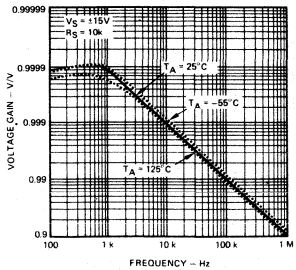
ELECTRICAL CHARACTERISTICS ($\pm 5\ V \leq V_S \leq \pm 18\ V$, $0°C \leq T_A \leq 70°C$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		2.5	7.5	mV
Input Bias Current	$T_A = 25°C$		2.0	7.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		Ω
Input Capacitance			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15\ V$ $V_{OUT} = \pm 10\ V$, $R_L = 8\ k\Omega$	0.999	0.9999		
Output Resistance	$T_A = 25°C$		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5	mA
Input Offset Voltage				10	mV
Offset Voltage Temperature Drift			10		μV/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$ $R_L = 10\ k\Omega$	0.999			
Output Voltage Swing (Note 4)	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±10			V
Supply Voltage Rejection Ratio	$\pm 5\ V \leq V_S \leq \pm 18\ V$	70	80		dB

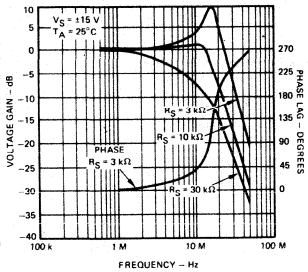
NOTES:
1. Rating applies to ambient temperatures up to +70°C. Above +70°C ambient, derate linearly at 6.3 mW/°C.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. For 102 and 110 continuous short circuit is allowed for case temperature of +125°C and ambient temperature to +70°C. For 302 and 310 continuous short circuit is allowed for case temperature to +70°C and ambient temperature to +55°C. It is necessary to insert a resistor greater than '2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.
4. Increased output swing under load can be obtained by connecting an external resistor between the booster and V– terminals (see curve).

TYPICAL PERFORMANCE CURVES FOR μA102 • μA302 • μA110 • μA310

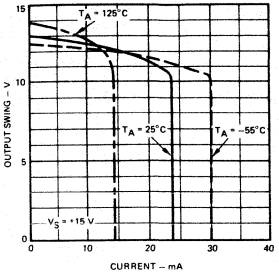
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



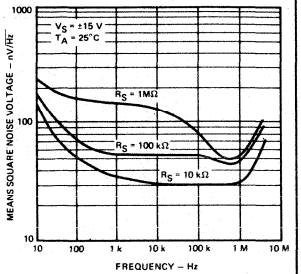
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



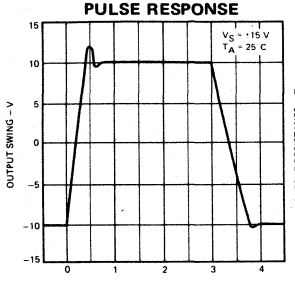
POSITIVE OUTPUT SWING AS A FUNCTION OF CURRENT



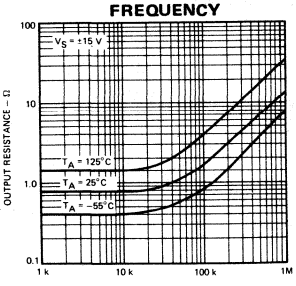
OUTPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



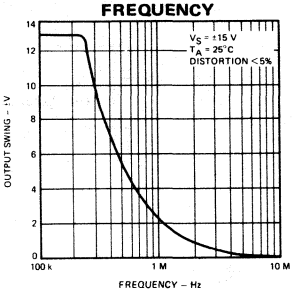
LARGE SIGNAL PULSE RESPONSE



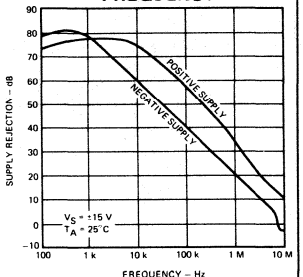
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



LARGE SIGNAL FREQUENCY RESPONSE AS A FUNCTION OF FREQUENCY

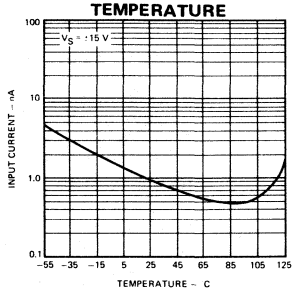


POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY

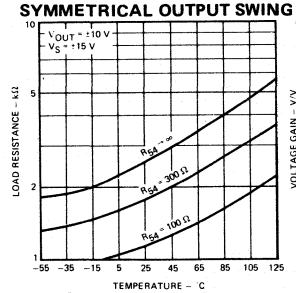


TYPICAL PERFORMANCE CURVES FOR μA102 • μA110

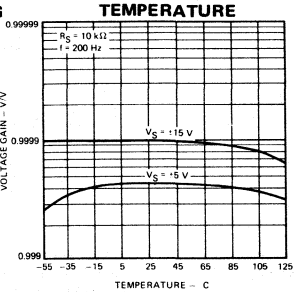
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



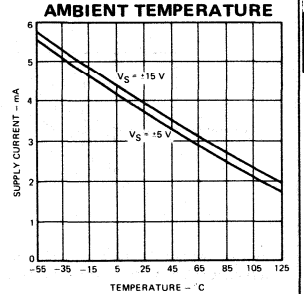
SYMMETRICAL OUTPUT SWING



VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE

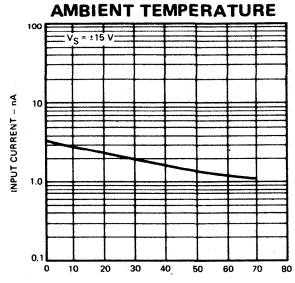


SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

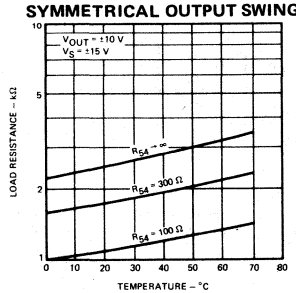


TYPICAL PERFORMANCE CURVES FOR μA302 • μA310

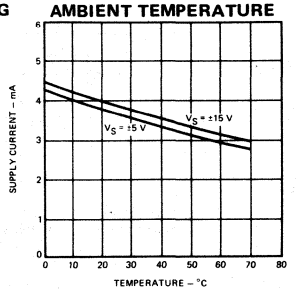
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



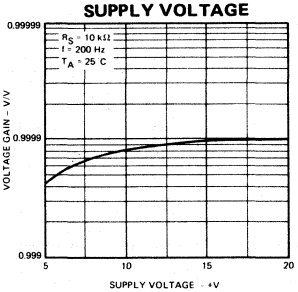
SYMMETRICAL OUTPUT SWING



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

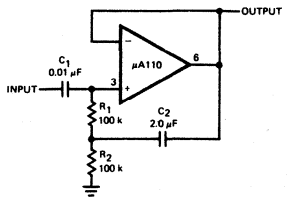


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

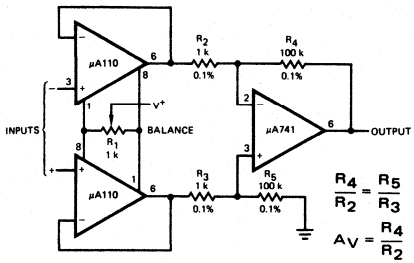


TYPICAL APPLICATIONS

HIGH INPUT IMPEDANCE AC AMPLIFIER



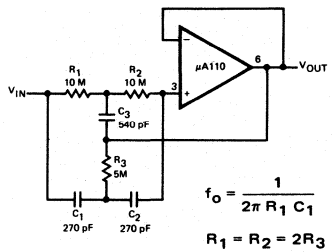
DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



$$\frac{R_4}{R_2} = \frac{R_5}{R_3}$$

$$A_V = \frac{R_4}{R_2}$$

HIGH Q NOTCH FILTER

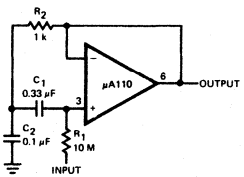


$$f_o = \frac{1}{2\pi R_1 C_1}$$

$$R_1 = R_2 = 2R_3$$

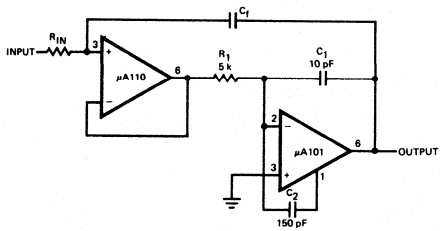
$$C_1 = C_2 = \frac{C_3}{2}$$

BANDPASS FILTER

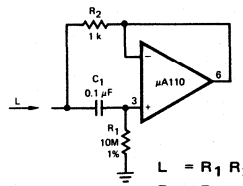


$$f_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

FAST INTEGRATOR WITH LOW INPUT CURRENT



SIMULATED INDUCTOR

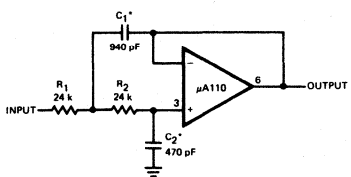


$$L = R_1 R_2 C_1$$

$$R_S = R_2$$

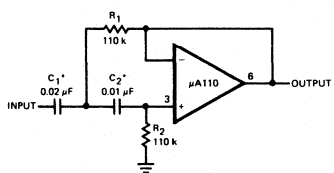
$$R_P = R_1$$

LOW PASS ACTIVE FILTER



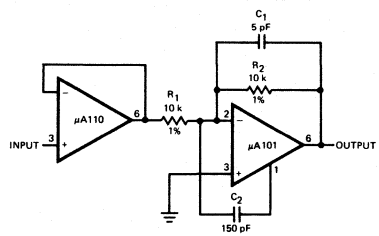
*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

HIGH PASS ACTIVE FILTER

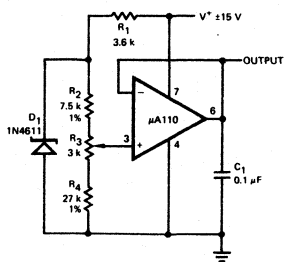


*Values are 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability

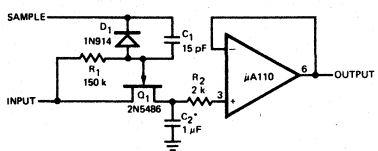
FAST INVERTING AMPLIFIER WITH HIGH INPUT IMPEDANCE



BUFFERED REFERENCE SOURCE

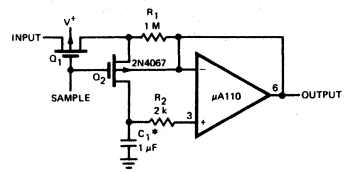


SAMPLE AND HOLD



*Use capacitor with polycarbonate teflon or polyethylene dielectric.

LOW DRIFT SAMPLE AND HOLD**



*Teflon, polyethylene or polycarbonate dielectric capacitor

**Worst case drift less than 3 mV/s

μA107 • μA207 • μA307

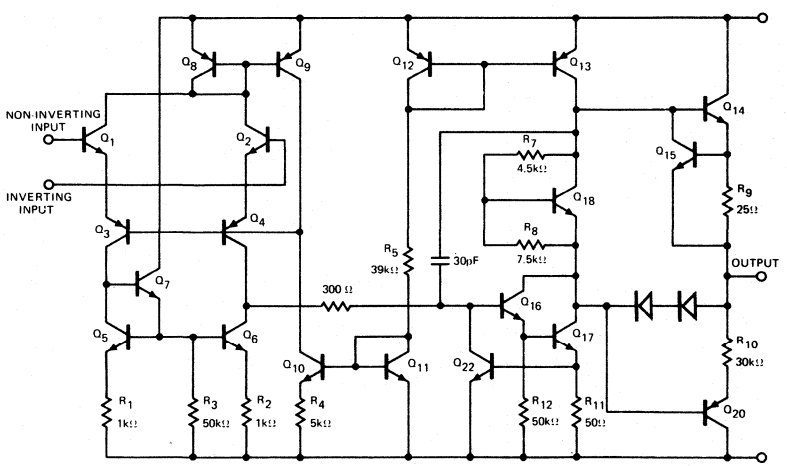
GENERAL PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 107 General Purpose Operational Amplifier series is constructed using the Fairchild Planar* epitaxial process. Advanced processing techniques have reduced the 107 input current an order of magnitude below industry standards such as the μA709 while still replacing, pin-for-pin, μA709, 101, 101A, and μA741. The 107, 207, and 307 offer better accuracy, internal compensation, and lower noise for high impedance circuit applications while providing features similar to the 101A. The low input currents allow the device to be used in slow-charge applications such as long period integrators, slow ramps, and sample-and-hold circuits. The 207 is identical to the 107 except that 207 performance is guaranteed from −25°C to +85°C while the 107 performance is guaranteed over a −55°C to +125°C temperature range. The 307 is available in both TO-99 and 8-lead mini DIP packages and is guaranteed over a 0°C to +70°C temperature range.

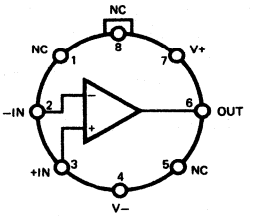
- **LOW OFFSET VOLTAGE**
- **LOW INPUT CURRENT**
- **LOW OFFSET CURRENT**
- **GUARANTEED DRIFT CHARACTERISTICS**
- **GUARANTEED OFFSETS OVER COMMON MODE RANGE**

EQUIVALENT CIRCUIT



Pin connections shown are for metal can.

CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

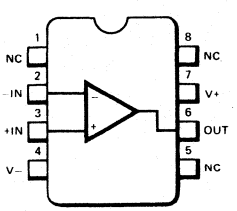


Note: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA107	μA107H
μA207	μA207H
μA307	μA307H

8-LEAD MINIDIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA307	μA307T

Dual In-line Package and Flatpak Available By Special Request

*Planar is patented Fairchild process.

12

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military and Instrument (μA107 and μA207)	±22 V
Commercial (μA307)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA107)	−55°C to +125°C
Instrument (μA207)	−25°C to +85°C
Commercial (μA307)	0°C to +70°C
Lead Temperature (Soldering)	
Metal Can (60 seconds)	300°C
Mini DIP (10 seconds)	260°C
Output Short Circuit Duration (μA107 and μA207)	Indefinite
(μA307, Note 3)	Indefinite

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and 5.6 mW/°C for the mini DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.

μA107 and μA207

ELECTRICAL CHARACTERISTICS ($\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$ for μA107 and μA207 unless otherwise specified).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.7	2.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			30	75	nA
Input Resistance		1.5	4.0		MΩ
Supply Current	$V_S = \pm 20\ V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$	50	160		V/mV
The following applies for $55°C \leq T_A \leq 125°C$ unless otherwise specified					
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		0.01	0.1	nA/°C
	$-55°C \leq T_A \leq 25°C$		0.02	0.2	nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20\ V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±12	±14		V
	$V_S = \pm 15\ V$, $R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 20\ V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		dB

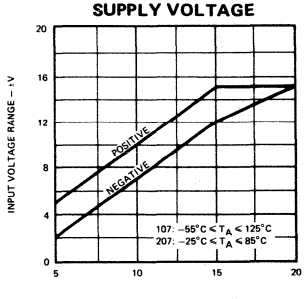
μA307

ELECTRICAL CHARACTERISTICS ($\pm 5\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$ unless otherwise specified.)

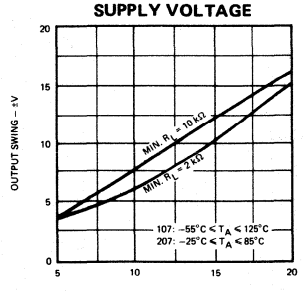
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$			2.0	7.5	mV
Input Offset Current				3.0	50	nA
Input Bias Current				70	250	nA
Input Resistance			0.5	2.0		MΩ
Supply Current	$V_S = \pm 15\ V$			1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$ $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$		25	160		V/mV
The following specifications apply for $0°C \leq TA \leq 70°C$						
Input Offset Voltage	$R_S \leq 50\ k\Omega$				10	mV
Average Temperature Coefficient of Input Offset Voltage				6.0	30	μV/°C
Input Offset Current					70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$			0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$			0.02	0.6	nA/°C
Input Bias Current					300	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$ $R_L \geq 2\ k\Omega$		15			V/mV
Output Voltage Swing	$V_S = \pm 15\ V$	$R_L = 10\ k\Omega$	±12	±14		V
		$R_L = 2\ k\Omega$	± 10	±13		V
Input Voltage Range	$V_S = \pm 15\ V$		±12			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		70	96		dB

GUARANTEED PERFORMANCE CURVES FOR μA107 AND μA207

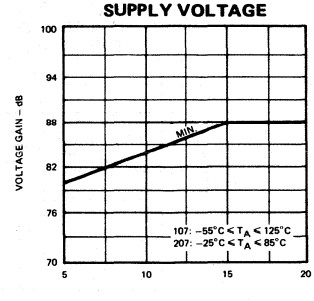
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

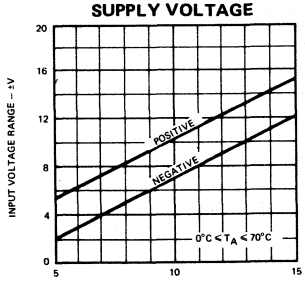


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

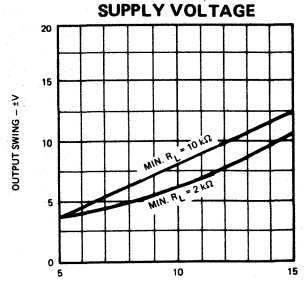


GUARANTEED PERFORMANCE CURVES FOR μA307

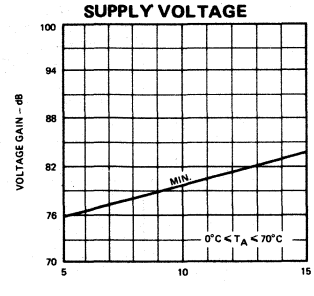
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

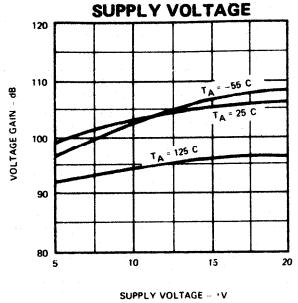


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

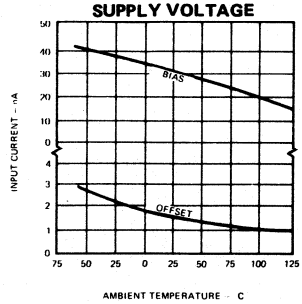


TYPICAL PERFORMANCE CURVES FOR μA107 AND μA207

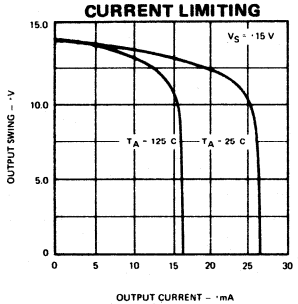
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



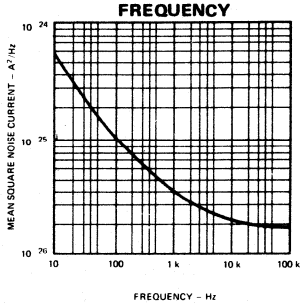
INPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



CURRENT LIMITING

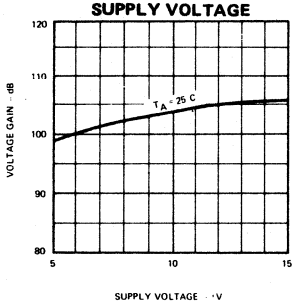


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

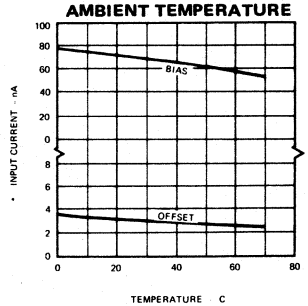


TYPICAL PERFORMANCE CURVES FOR μA307

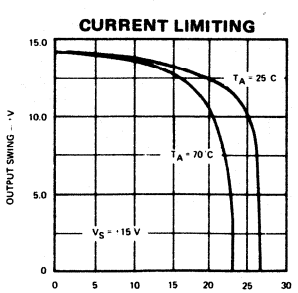
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



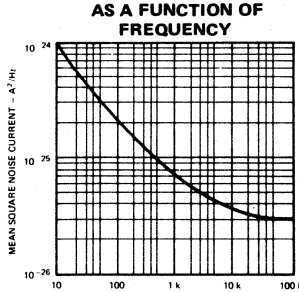
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



CURRENT LIMITING

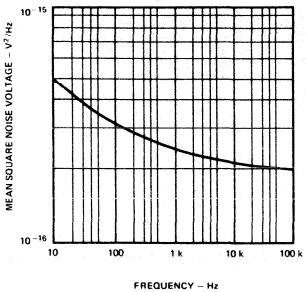


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

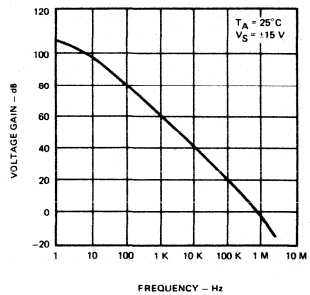


TYPICAL PERFORMANCE CURVES

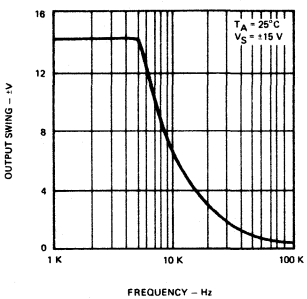
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



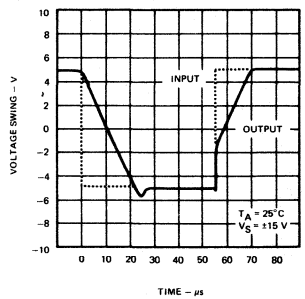
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



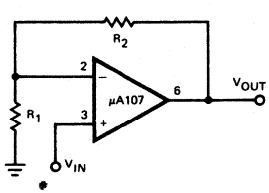
VOLTAGE FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

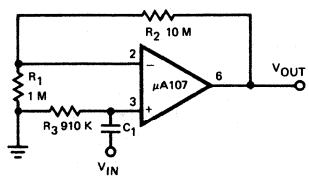
(All pin numbers shown refer to 8-lead TO-5 package)

NON-INVERTING AMPLIFIER



$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

NON-INVERTING AC AMPLIFIER

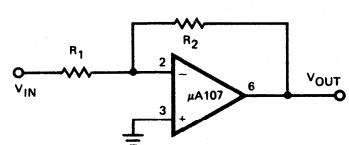


$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

$$R_{IN} = R_3$$

$$R_3 = R_1 R_2$$

INVERTING AMPLIFIER



$$V_{OUT} = \frac{R_2}{R_1} V_{IN}$$

$$R_{IN} = R_1$$

12

μA108A • μA208A • μA308A
μA108 • μA208 • μA308
SUPER BETA OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

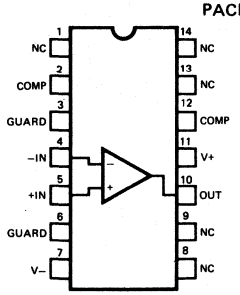
GENERAL DESCRIPTION – The 108 Super Beta Operational Amplifier series is constructed using the Fairchild Planar* epitaxial process. High input impedance, low noise, input offsets, and temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The 108A series is specially selected for extremely low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- **GUARANTEED LOW INPUT OFFSET CHARACTERISTICS**
- **HIGH INPUT IMPEDANCE**
- **LOW OFFSET CURRENT**
- **LOW BIAS CURRENT**
- **OPERATION OVER WIDE SUPPLY RANGE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA108A, μA108, μA208A, μA208	±20 V
μA308A, μA308	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA108A, μA108)	−55°C to +125°C
Industrial (μA208A, μA208)	−25°C to +85°C
Commercial (μA308A, μA308)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	300°C
Output Short Circuit Duration (Note 4)	Indefinite

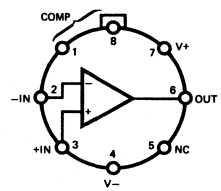
14-LEAD DIP **
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA108A	μA108AD
μA108	μA108D
μA208A	μA208AD
μA208	μA208D
μA308A	μA308AD
μA308	μA308D

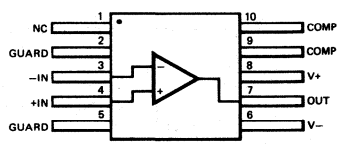
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA108A	μA108AH
μA108	μA108H
μA208A	μA208AH
μA208	μA208H
μA308A	μA308AH
μA308	μA308H

10-LEAD FLATPAK**
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

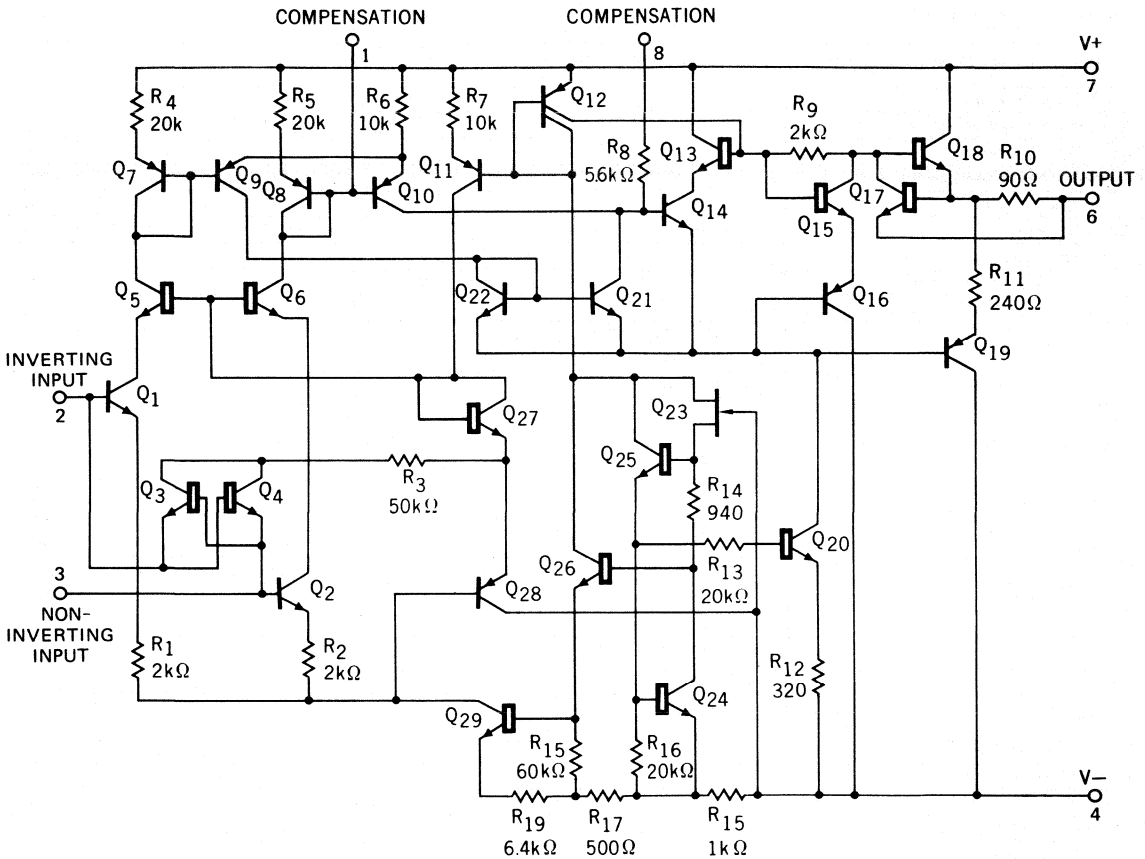
TYPE	PART NO.
μA108A	μA108AF
μA108	μA108F
μA208A	μA208AF
μA208	μA208F

** Available on special order

See notes on following pages.

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



Pin numbers are for metal can only

12

ELECTRICAL CHARACTERISTICS FOR μA108A AND μA208A ($\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.6	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	80,000	300,000		V/V
The following specifications apply for $-55°C \leq T_A \leq +125°C$ (Note 5)					
Input Offset Voltage				1.0	mV
Average Input Offset Voltage Drift			1.0	5.0	μV/°C
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	pA/°C
Input Bias Current			0.8	3.0	nA
Supply Current	$T_A = +125°C$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$ $V_{OUT} = \pm 10\ V$	40,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$	±13	±14		V

ELECTRICAL CHARACTERISTICS FOR μA308A ($\pm 5\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	80,000	300,000		V/V
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage				0.73	mV
Average Input Offset Voltage Drift			1.0	5.0	μV/°C
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	pA/°C
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	60,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$	±13	±14		V

NOTES:

1. The maximum junction temperature of the 108A/108 is 150°C, while that of the 208A/208 is 100°C, and 308A/308 is 85°C. For operating at elevated temperatures, devices in the TO-99 package must be derated based on thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flatpak a maximum rating of 300 mW applies and derating is based on a thermal resistance of 185°C/W when mounted on a 1/16 inch thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the Dual In-line Package is 100°C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless adequate limiting resistance is used.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.
5. For the 208A/208, all temperature specifications apply over $-25°C \leq T_A \leq 85°C$.

ELECTRICAL CHARACTERISTICS FOR μA108 AND μA208 ($\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

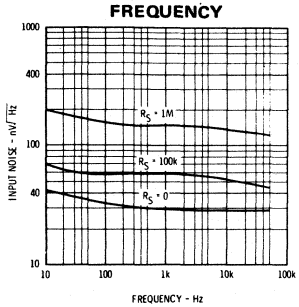
PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.7	2.0	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.6	mA
Large Signal Voltage Gain	$R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$ $V_S = \pm 15\ V$	50,000	300,000		V/V
The following specifications apply for $-55°C \leq T_A \leq 125°C$ (Note 5)					
Input Offset Voltage				3.0	mV
Average Input Offset Voltage Drift			3.0	15	μV/°C
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	pA/°C
Input Bias Current				3.0	nA
Supply Current	$T_A = +125°C$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		85	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	25,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±13	±14		V

ELECTRICAL CHARACTERISTICS FOR μA308 ($\pm 5\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

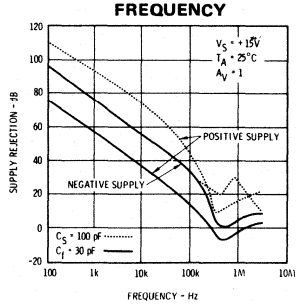
PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	25,000	300,000		V/V
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage				10	mV
Average Input Offset Voltage Drift			6.0	30	μV/°C
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	pA/°C
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		80	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	15,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±13	±14		V

TYPICAL PERFORMANCE CURVES FOR μA108 SERIES

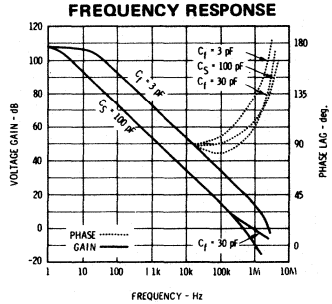
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



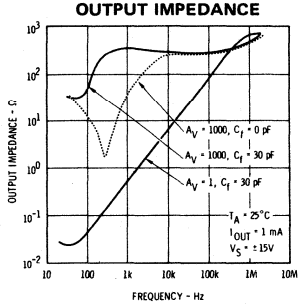
POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY



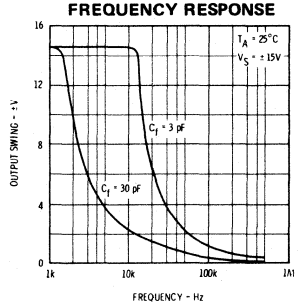
OPEN LOOP FREQUENCY RESPONSE



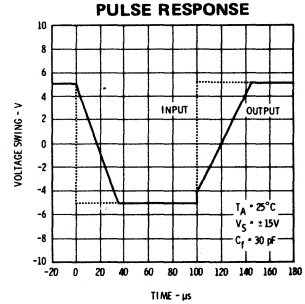
CLOSED LOOP OUTPUT IMPEDANCE



LARGE SIGNAL FREQUENCY RESPONSE

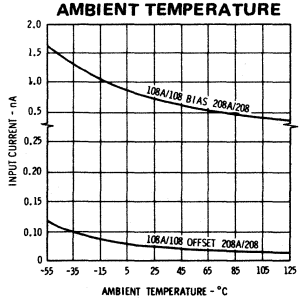


VOLTAGE FOLLOWER PULSE RESPONSE

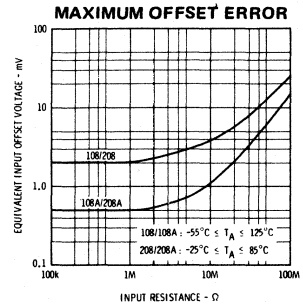


TYPICAL PERFORMANCE CURVES FOR μA108A • μA208A • μA108 • μA208 (Unless Otherwise Specified)

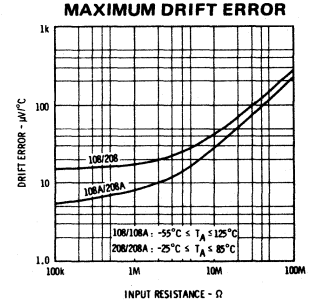
INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



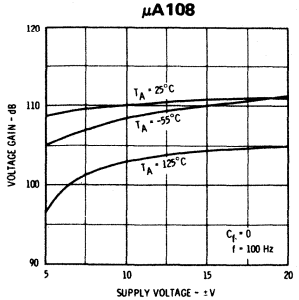
MAXIMUM OFFSET ERROR



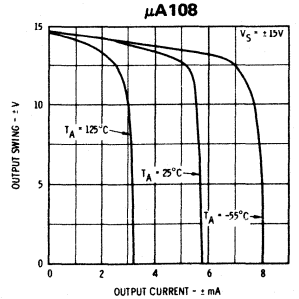
MAXIMUM DRIFT ERROR



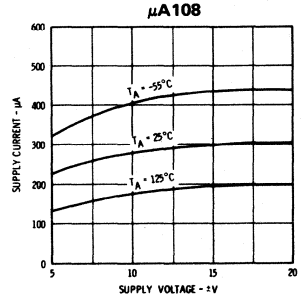
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE μA108



OUTPUT SWING AS A FUNCTION OF OUTPUT CURRENT μA108

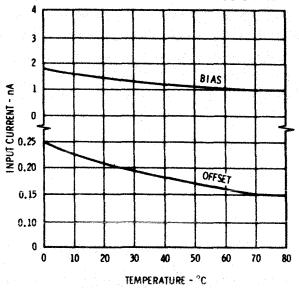


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE μA108

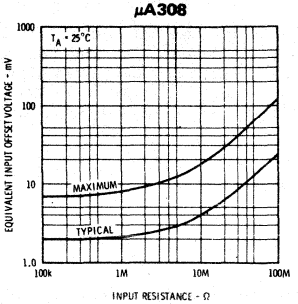


TYPICAL PERFORMANCE CURVES FOR μA308A AND μA308 (Unless Otherwise Specified)

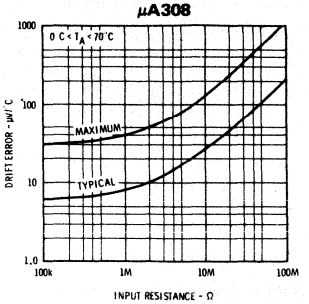
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



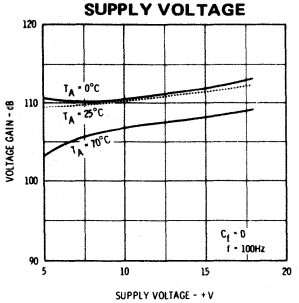
MAXIMUM OFFSET ERROR μA308



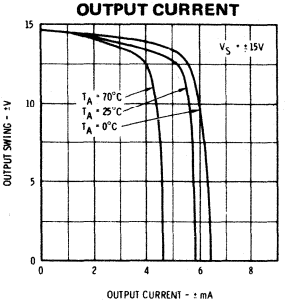
MAXIMUM DRIFT ERROR μA308



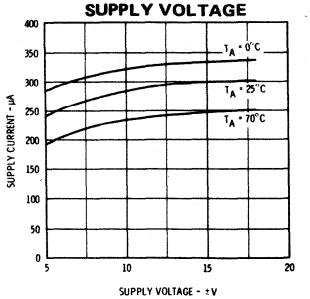
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



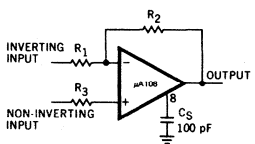
OUTPUT SWING AS A FUNCTION OF OUTPUT CURRENT

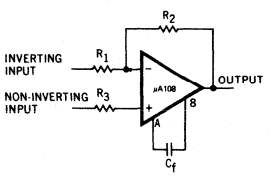


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



STANDARD COMPENSATION CIRCUITS

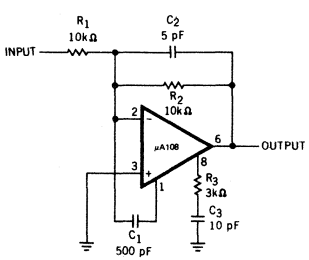




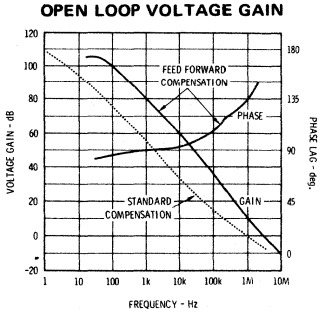
$$C_f \geq 30 \left(\frac{1}{1 + \frac{R_2}{R_1}} \right)$$

FEEDFORWARD COMPENSATION HIGHER SLEW RATES AND WIDER BANDWIDTH

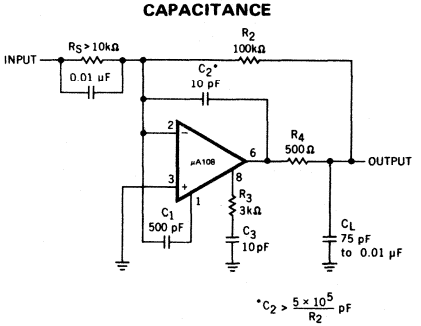
STANDARD FEEDFORWARD



OPEN LOOP VOLTAGE GAIN



FEEDFORWARD COMPENSATION FOR DECOUPLING LOAD CAPACITANCE



$$^*C_2 > \frac{5 \times 10^5}{R_2} \text{ pF}$$

12

GUARDING

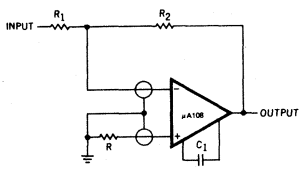
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

The pin configuration of the Dual In-line Package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard μA741 and 101A pin configuration).

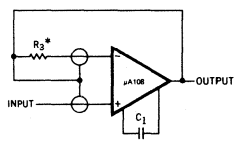
CONNECTION OF INPUT GUARDS

INVERTING AMPLIFIER



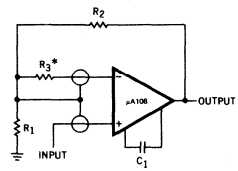
$$R = \frac{R_1 R_2}{R_1 + R_2}$$

FOLLOWER



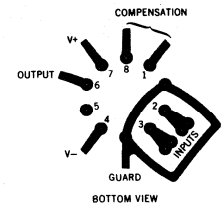
*Use to compensate for large source resistances.

NON-INVERTING AMPLIFIER



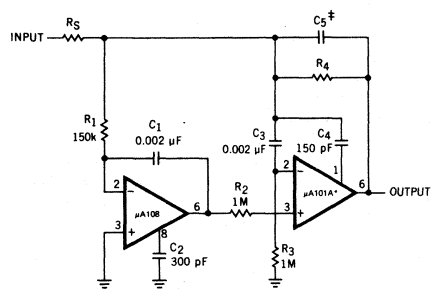
NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be low impedance

BOARD LAYOUT FOR INPUT GUARDING WITH TO-99 PACKAGE (BOTTOM VIEW)



TYPICAL APPLICATIONS

FAST† SUMMING AMPLIFIER WITH LOW INPUT CURRENT

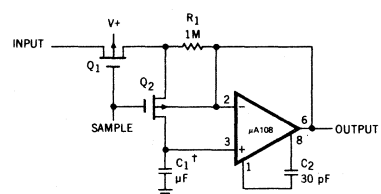


*In addition to increasing speed, the 101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/μs

‡ $C_5 = \frac{6 \times 10^{-8}}{R_1}$

SAMPLE AND HOLD



* Worst case drift less than 2.5 mV/s
† Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

μA702
WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA702 is a monolithic DC Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from dc to 30 MHz.

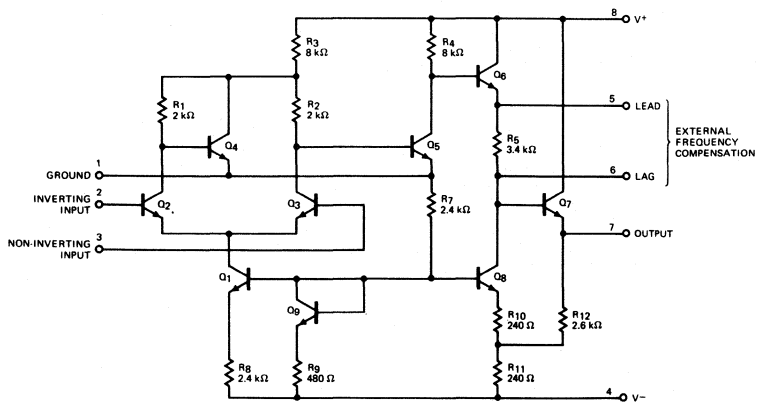
- **LOW OFFSET VOLTAGE**
- **LOW OFFSET VOLTAGE DRIFT**
- **WIDE BANDWIDTH – 20 MHz TYP**
- **HIGH SLEW RATE – 5 V/μs TYP**

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to –6.0 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (μA702)	–55°C to +125°C
Commercial (μA702C)	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

NOTE
Rating applies to ambient temperature up to 70 C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for DIP and 7.1 mW/°C for the Flatpak.

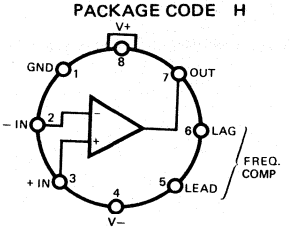
EQUIVALENT CIRCUIT



Pin numbers are shown for metal can only.

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

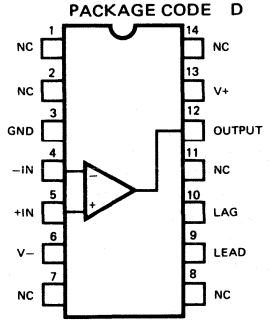


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA702	μA702HM
μA702C	μA702HC

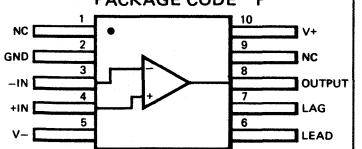
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA702	μA702DM
μA702C	μA702DC

10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA702	μA702FM

*Planar is a patented Fairchild process.

12

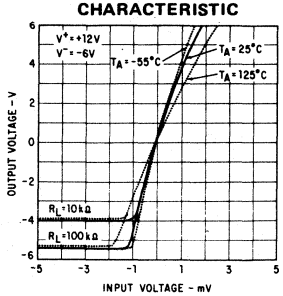
μA702

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

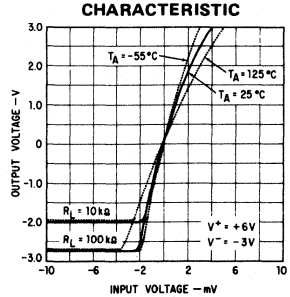
PARAMETER		CONDITIONS	V+ = 12.0V, V− = −6.0V			V+ = 6.0V, V− = −3.0V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage		$R_S \leq 2\,k\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current				180	500		120	500	nA
Input Bias Current				2.0	5.0		1.2	3.5	μA
Input Resistance			16	40		22	67		kΩ
Input Voltage Range			−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio		$R_S \leq 2\,k\Omega$, f ≤ 1 kHz	80	100		80	100		dB
Large Signal Voltage Gain		$R_L \geq 100\,k\Omega$, V_{OUT} = ±5.0 V	2500	3600	6000				
		$R_L \geq 100\,k\Omega$, V_{OUT} = ±2.5 V				600	900	1500	
Output Resistance				200	500		300	700	Ω
Supply Current		V_{OUT} = 0		5.0	6.7		2.1	3.3	mA
Power Consumption		V_{OUT} = 0		90	120		19	30	mW
Transient Response (unity-gain)	Rise Time	CI = 0.01 μF, RI = 20 Ω, $R_L \geq 100\,k\Omega$, V_{IN} = 10 mV		25	120				ns
	Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (x100 gain)	Rise Time	C3 = 50 pF, $R_L \geq 100\,k\Omega$,		10	30				ns
	Overshoot	V_{IN} = 1 mV		20	40				%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:									
Input Offset Voltage		$R_S \leq 2\,k\Omega$			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50 Ω, T_A = 25°C to +125°C		2.5	10		3.5	15	μV/°C
		R_S = 50 Ω, T_A = 25°C to −55°C		2.0	10		3.0	15	μV/°C
Input Offset Current		T_A = +125°C		80	500		50	500	nA
		T_A = −55°C		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current		T_A = 25°C to +125°C		1.0	5.0		0.7	4.0	nA/°C
		T_A = 25°C to −55°C		3.0	16		2.0	13	nA/°C
Input Bias Current		T_A = −55°C		4.3	10		2.6	7.5	μA
Input Resistance			6.0			8.0			kΩ
Common Mode Rejection Ratio		$R_S \leq 2\,k\Omega$, f ≤ 1 kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio		V+ = 12 V, V− = −6.0 V to V+ = 6.0 V, V− = −3.0 V $R_S \leq 2\,k\Omega$		75	200		75	200	μV/V
Large Signal Voltage Gain		$R_L \geq 100\,k\Omega$, V_{OUT} = ±5.0 V	2000		7000				
		$R_L \geq 100\,k\Omega$, V_{OUT} = ±2.5 V				500		1750	
Output Voltage Swing		$R_L \geq 100\,k\Omega$	±5.0	±5.3		±2.5	±2.7		V
		$R_L \geq 10\,k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current		T_A = +125°C, V_{OUT} = 0		4.4	6.7		1.7	3.3	mA
		T_A = −55°C, V_{OUT} = 0		5.0	7.5		2.1	3.9	mA
Power Consumption		T_A = +125°C, V_{OUT} = 0		80	120		15	30	mW
		T_A = −55°C, V_{OUT} = 0		90	135		19	35	mW

TYPICAL PERFORMANCE CURVE FOR μA702

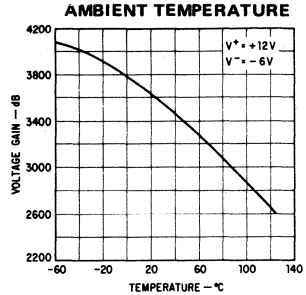
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



μA702C

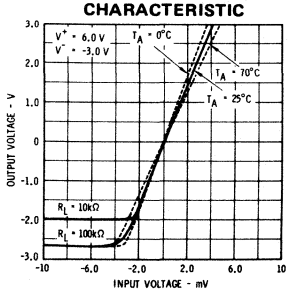
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	V+ = 12.0 V, V− = −6.0 V			V+ = 6.0 V, V− = −3.0 V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage		$R_S \leq 2k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current				0.5	2.0		0.3	2.0	μA
Input Bias Current				2.5	7.5		1.5	5.0	μA
Input Resistance			10	32		16	55		kΩ
Input Voltage Range			−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio		$R_S \leq 2$ kΩ, f ≤ 1 kHz	70	92		70	92		dB
Large Signal Voltage Gain		$R_L \geq 100$ kΩ, V_{OUT} = ±5.0 V	2000	3400	6000				
		$R_L \geq 100$ kΩ, V_{OUT} = ±2.5 V				500	800	1500	
Output Resistance				200	600		300	800	Ω
Supply Current		V_{OUT} = 0		5.0	6.7		2.1	3.3	mA
Power Consumption		V_{OUT} = 0		90	120		19	30	mW
Transient Response (unity gain)	Rise Time	C1 = 0.01 μF, R_I = 20 Ω $R_L \leq 100$ kΩ, V_{IN} = 10 mV		25	120				ns
	Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (x100 gain)	Rise Time	C3 = 50 pF, $R_L \geq 100$ kΩ,		10	30				ns
	Overshoot	V_{IN} = 1 mV		20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:									
Input Offset Voltage		$R_S \leq 2$ kΩ			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50 Ω, T_A = +70°C to 0°C		5.0	20		7.5	25	μV/°C
Input Offset Current					2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current		T_A = 25°C to +70°C		4.0	10		3.0	8.0	nA/°C
		T_A = 25°C to 0°C		6.0	20		5.5	18	nA/°C
Input Bias Current		T_A = 0°C		4.0	12		2.7	8	μA
Input Resistance			6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio		$R_S \leq 2$ kΩ, f ≤ 1 kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio		V+ = 12 V, V− = −6.0 V to V+ = 6.0 V, V− = −3.0 V $R_S \leq 2$ kΩ		90	300		90	300	μV/V
Large Signal Voltage Gain		$R_L \geq 100$ kΩ, V_{OUT} = ±5.0 V	1500		7000				
		$R_L \geq 100$ kΩ, V_{OUT} = ±2.5 V				400		1750	
Output Voltage Swing		$R_L \geq 100$ kΩ	±5.0	±5.3		±2.5	±2.7		V
		$R_L \geq$ 10 kΩ	±3.5	±4.0		±1.5	±2.0		V
Supply Current		V_{OUT} = 0		5.0	7.0		2.1	3.9	mA
Power Consumption		V_{OUT} = 0		90	125		19	35	mW

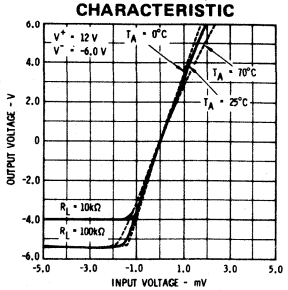
12

TYPICAL PERFORMANCE CURVES FOR μA702C

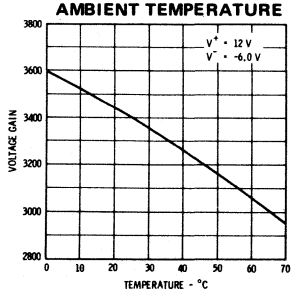
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE TRANSFER CHARACTERISTIC

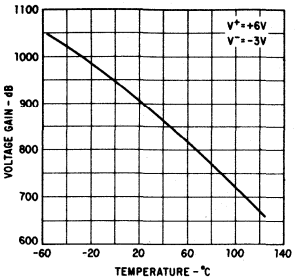


VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

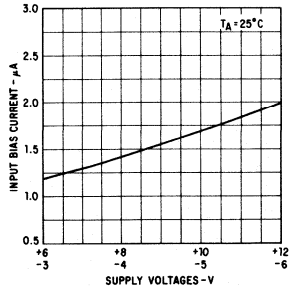


TYPICAL PERFORMANCE CURVES FOR μA702

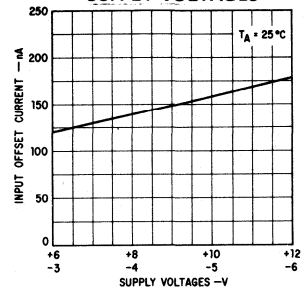
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



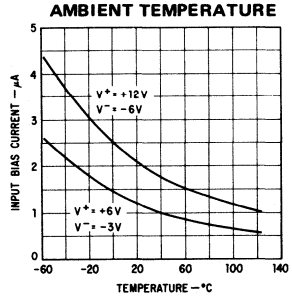
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



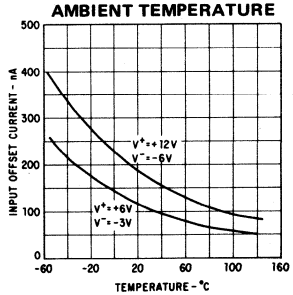
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



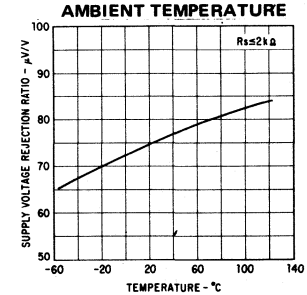
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



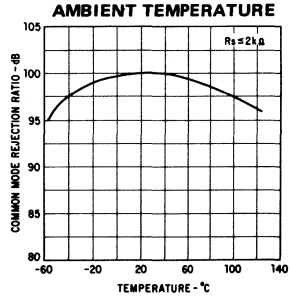
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



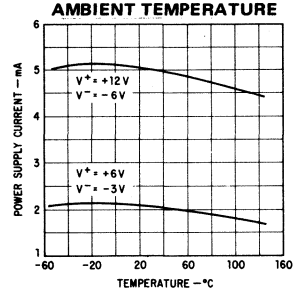
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



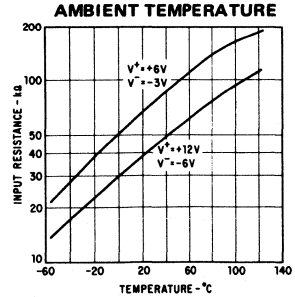
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



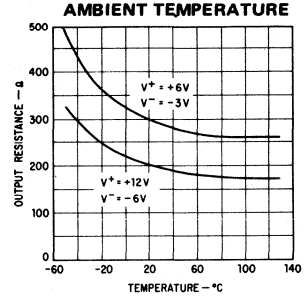
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

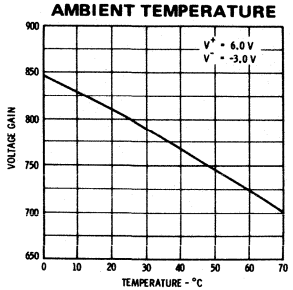


OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

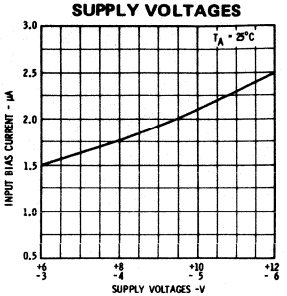


TYPICAL PERFORMANCE CURVES FOR μA702C

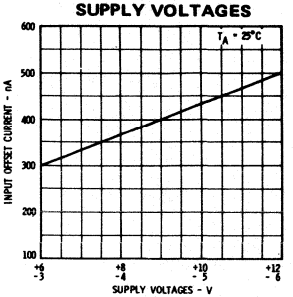
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



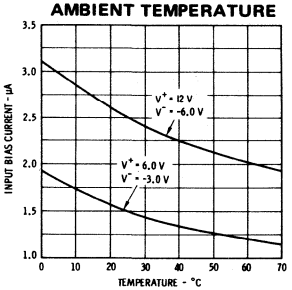
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



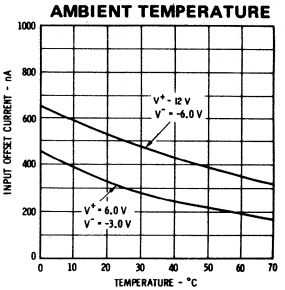
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



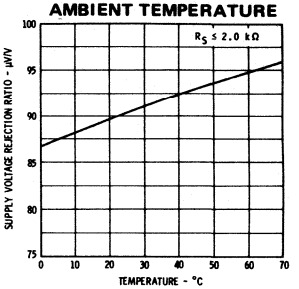
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



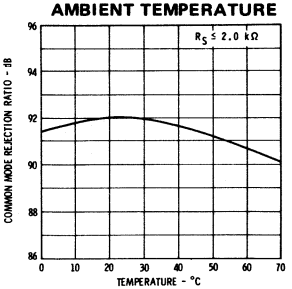
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



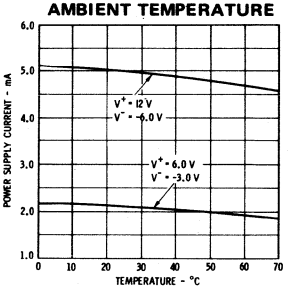
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



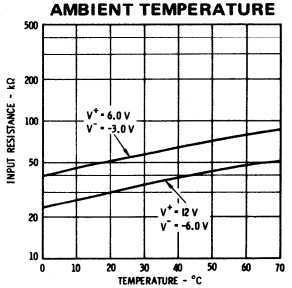
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



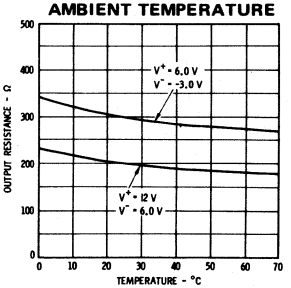
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



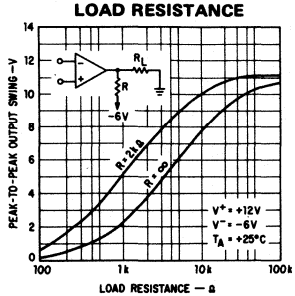
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



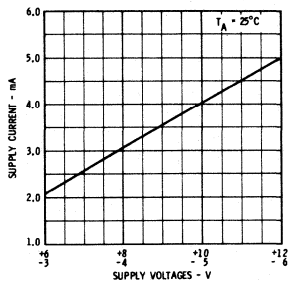
12

TYPICAL PERFORMANCE CURVES FOR μA702 AND μA702C

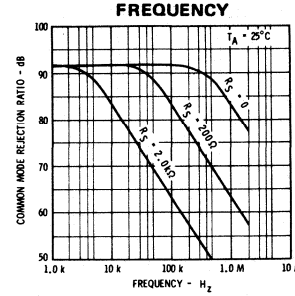
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



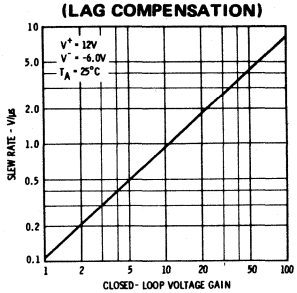
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



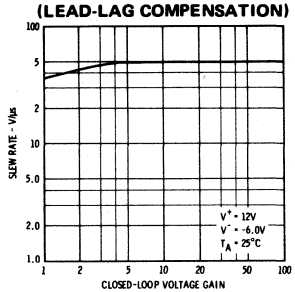
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



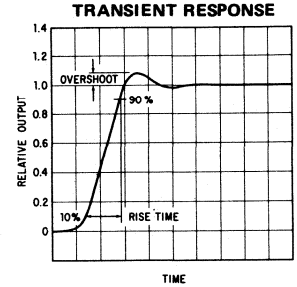
SLEW RATE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN (LAG COMPENSATION)



SLEW RATE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

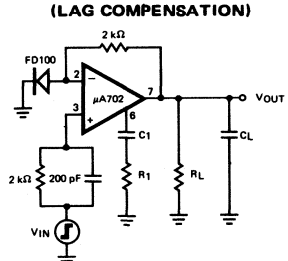


TRANSIENT RESPONSE

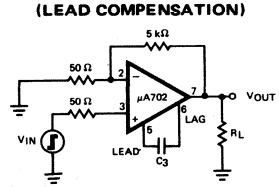


TRANSIENT RESPONSE TEST CIRCUITS

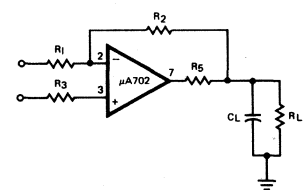
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



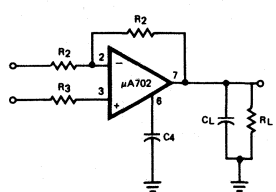
X100 AMPLIFIER (LEAD COMPENSATION)



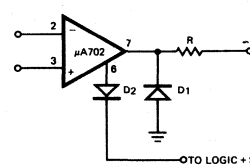
SERIES RESISTANCE LIMITING*



OUTPUT RISE TIME LIMITING*



LOGIC COMPATIBILITY

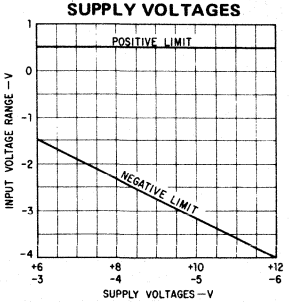


*Peak current limiting with capacitive loads.

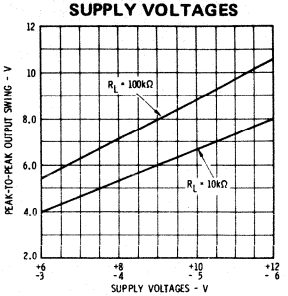
Pin numbers are shown for metal can only.

TYPICAL PERFORMANCE CURVES FOR μA702 AND μA702C

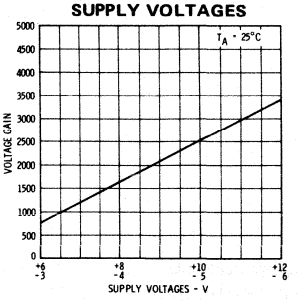
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



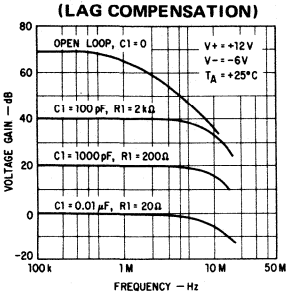
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



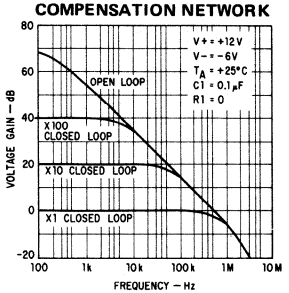
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



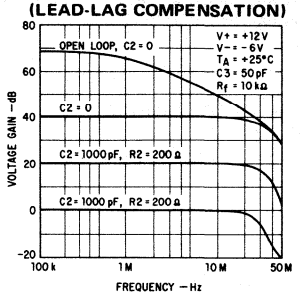
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



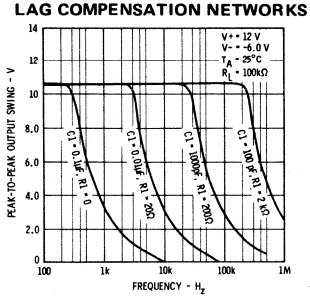
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



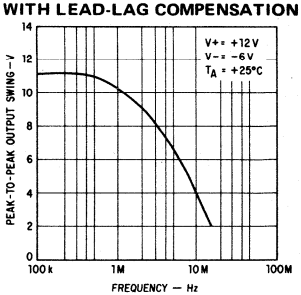
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

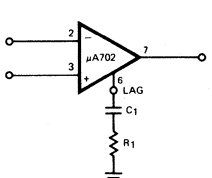


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION

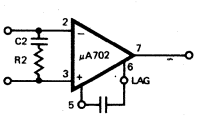


FREQUENCY COMPENSATION CIRCUITS

LAG COMPENSATION



LEAD-LAG COMPENSATION



Pin numbers are shown for metal can only.

μA709

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA709 is a monolithic High Gain Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little performance degradation. The amplifier is intended for use in dc servo systems, high impedance analog computers, low level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

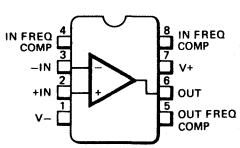
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Storage Temperature Range	
Metal, Hermetic DIP, and Flatpak	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA709A and μA709)	−55°C to +125°C
Commercial (μA709C)	0°C to +70°C
Lead Temperature	
Metal Can, Hermetic DIP, and Flatpak (Soldering 60 s)	300°C
Molded DIP	260°C
Output Short Circuit Duration	5 s

NOTE:
Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for DIP, 7.1mW/°C for the Flatpak and 5.6mW/°C for the Mini DIP.

CONNECTION DIAGRAMS

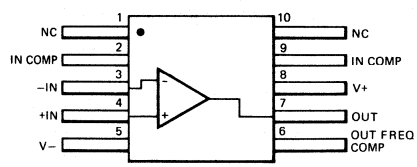
8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA709C	μA709TC

10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F

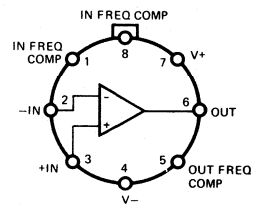


ORDER INFORMATION

TYPE	PART NO.
μA709A	μA709AFM
μA709	μA709FM

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

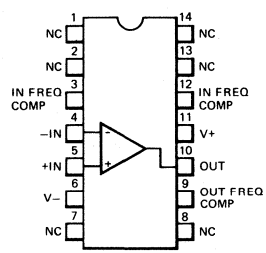


NOTE: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA709A	μA709AHM
μA709	μA709HM
μA709C	μA709HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA709A	μA709ADM
μA709	μA709DM
μA709C	μA709DC
μA709C	μA709PC

*Planar is a patented Fairchild process.

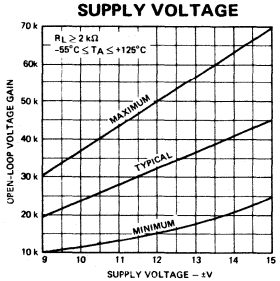
μA709A

ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

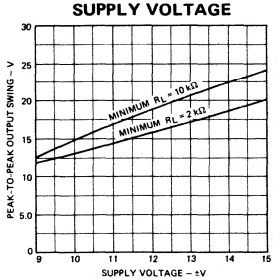
PARAMETER (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		0.6	2.0	mV
Input Offset Current				10	50	nA
Input Bias Current				100	200	nA
Input Resistance			350	700		kΩ
Output Resistance				150		Ω
Supply Current		V_S = ±15 V		2.5	3.6	mA
Power Consumption		V_S = ±15 V		75	108	mW
Transient Response	Rise time	V_S = ±15 V, V_{IN} = 20 mV, R_L = 2 kΩ, C1 = 5 nF, R1 = 1.5 kΩ, C2 = 200 pF, R2 = 50Ω $C_L \leq 100$ pF			1.5	μs
	Overshoot				30	%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:						
Input Offset Voltage		$R_S \leq 10$ kΩ			3.0	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50Ω, T_A = +25°C to +125°C		1.8	10	μV/°C
		R_S = 50Ω, T_A = +25°C to −55°C		1.8	10	μV/°C
		R_S = 10 kΩ, T_A = +25°C to +125°C		2.0	15	μV/°C
		R_S = 10 kΩ, T_A = +25°C to −55°C		4.8	25	μV/°C
Input Offset Current		T_A = +125°C		3.5	50	nA
		T_A = −55°C		40	250	nA
Average Temperature Coefficient of Input Offset Current		T_A = +25°C to +125°C		0.08	0.5	nA/°C
		T_A = +25°C to −55°C		0.45	2.8	nA/°C
Input Bias Current		T_A = −55°C		300	600	nA
Input Resistance		T_A = −55°C	85	170		kΩ
Input Voltage Range		V_S = ±15 V	±8.0			V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	80	110		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		40	100	μV/V
Large Signal Voltage Gain		V_S = ±15 V, $R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000		70,000	V/V
Output Voltage Swing		V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
		V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Supply Current		T_A = +125°C, V_S = ±15 V		2.1	3.0	mA
		T_A = −55°C, V_S = ±15 V		2.7	4.5	mA
Power Consumption		T_A = +125°C, V_S = ±15 V		63	90	mW
		T_A = −55°C, V_S = ±15 V		81	135	mW

PERFORMANCE CURVES FOR μA709A

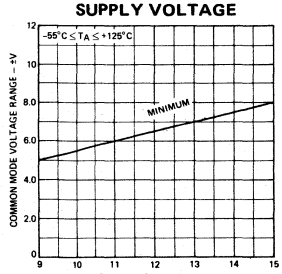
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



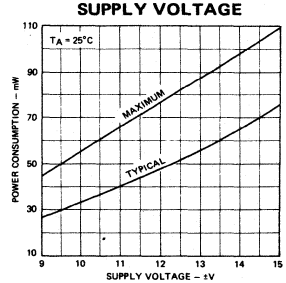
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



12

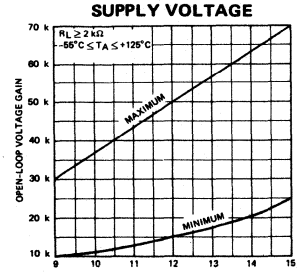
μA709

ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

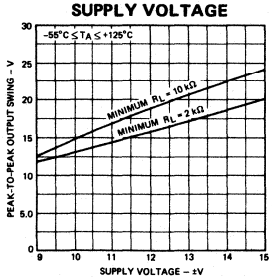
PARAMETER (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current				50	200	nA
Input Bias Current				200	500	nA
Input Resistance			150	400		kΩ
Output Resistance				150		Ω
Power Consumption		V_S = ±15 V		80	165	mW
Transient Response	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, C1 = 5000 pF, R1 = 1.5 kΩ, C2 = 200 pF, R2 = 50Ω		0.3	1.0	μs
	Overshoot	$C_L \leq 100$ pF		10	30	%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:						
Input Offset Voltage		$R_S \leq 10\ k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50Ω		3.0		μV/°C
		$R_S \leq 10\ k\Omega$		6.0		μV/°C
Large Signal Voltage Gain		V_S = ±15 V, $R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	25,000	45,000	70,000	V/V
Output Voltage Swing		V_S = ±15 V, $R_L \geq 10\ k\Omega$	±12	±14		V
		V_S = ±15 V, $R_L \geq 2\ k\Omega$	±10	±13		V
Input Voltage Range		V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10\ k\Omega$		25	150	μV/V
Input Offset Current		T_A = +125°C		20	200	nA
		T_A = −55°C		100	500	nA
Input Bias Current		T_A = −55°C		0.5	1.5	μA
Input Resistance			40	100		kΩ

PERFORMANCE CURVES FOR μA709

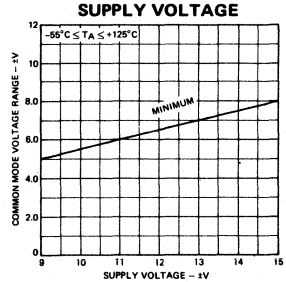
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



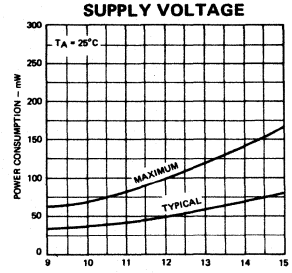
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



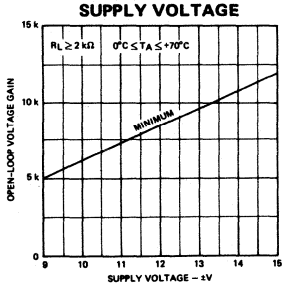
μA709C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

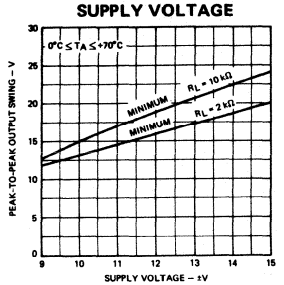
PARAMETER (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$, ±9 V ≤ V_S ≤ ±15 V		2.0	7.5	mV
Input Offset Current				100	500	nA
Input Bias Current				0.3	1.5	μA
Input Resistance			50	250		kΩ
Output Resistance				150		Ω
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	15,000	45,000		V/V
Output Voltage Swing		$R_L \geq 10\ k\Omega$	±12	±14		V
		$R_L \geq 2\ k\Omega$	±10	±13		V
Input Voltage Range			±8.0	±10		V
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	65	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10\ k\Omega$		25	200	μV/V
Power Consumption				80	200	mW
Transient Response	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, C1 = 5000 pF, R1 = 1.5 kΩ, C2 = 200 pF, R2 = 50Ω		0.3		μs
	Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:						
Input Offset Voltage		$R_S \leq 10\ k\Omega$, ±9 V ≤ V_S ≤ ±15 V			10	mV
Input Offset Current					750	nA
Input Bias Current					2.0	μA
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	12,000			V/V
Input Resistance			35			kΩ

PERFORMANCE CURVES FOR μA709C

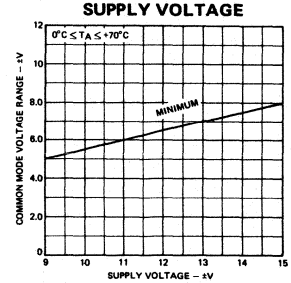
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

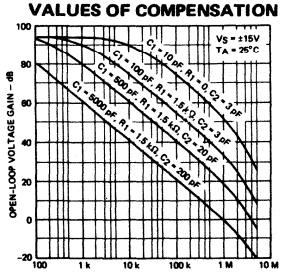


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

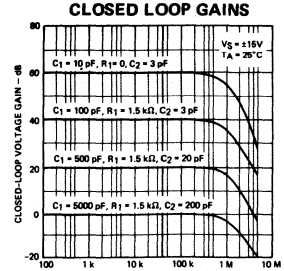


FREQUENCY COMPENSATION CURVES FOR ALL TYPES

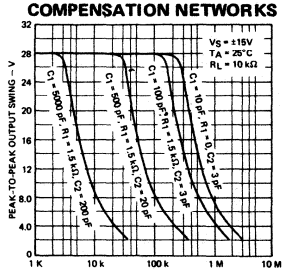
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

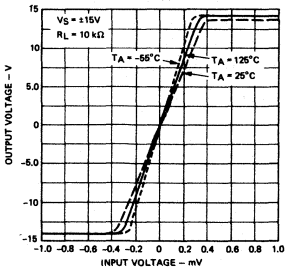


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

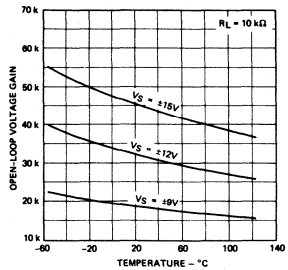


TYPICAL PERFORMANCE CURVES FOR μA709A

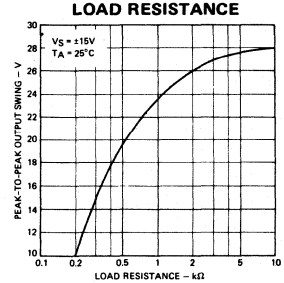
VOLTAGE TRANSFER CHARACTERISTIC



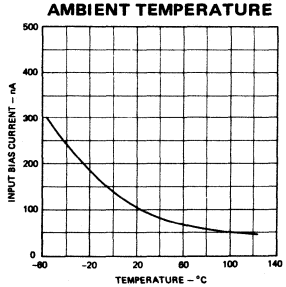
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



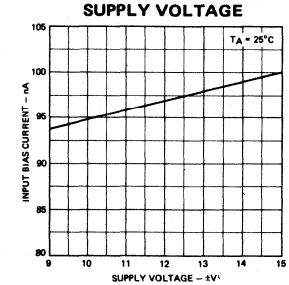
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



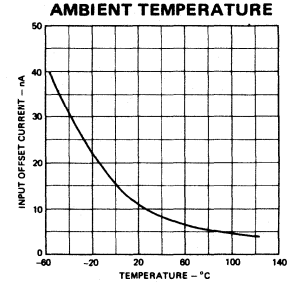
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



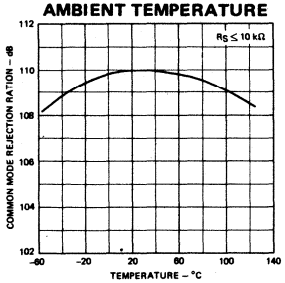
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



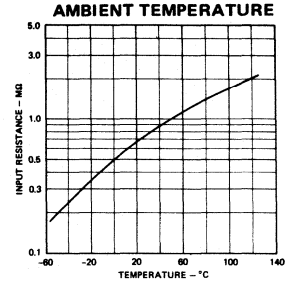
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



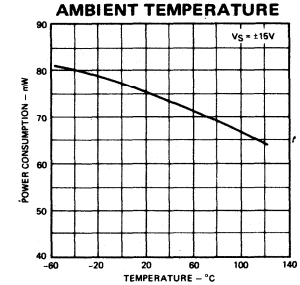
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



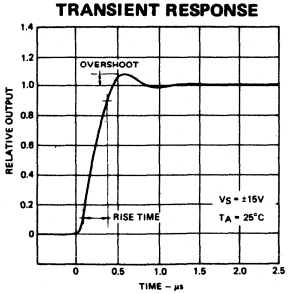
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



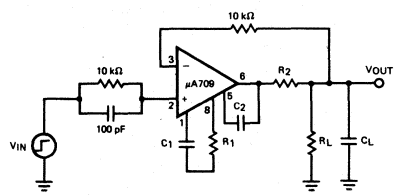
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSIENT RESPONSE

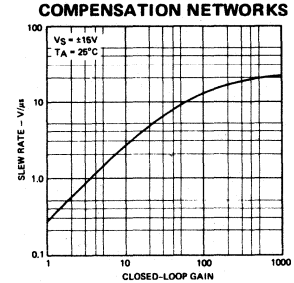


TRANSIENT RESPONSE TEST CIRCUIT



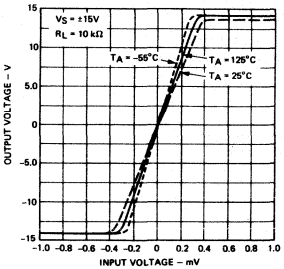
Pin numbers on this and all succeeding circuits apply to metal can or mini DIP package.

SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

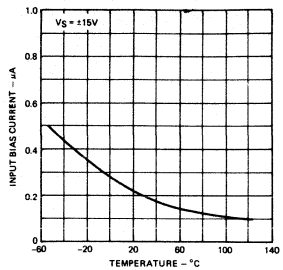


TYPICAL PERFORMANCE CURVES FOR μA709 AND μA709C

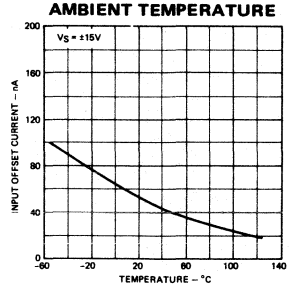
VOLTAGE TRANSFER CHARACTERISTIC



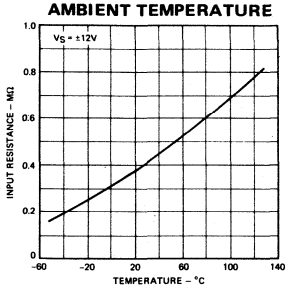
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



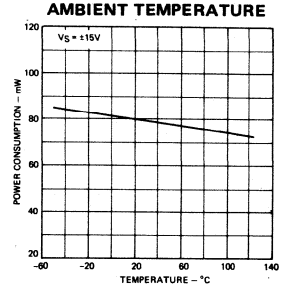
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



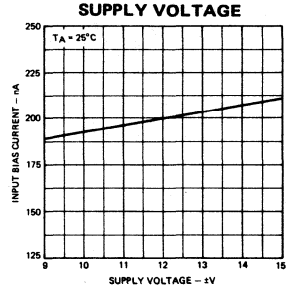
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



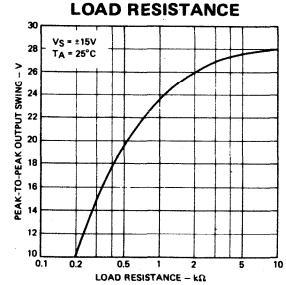
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



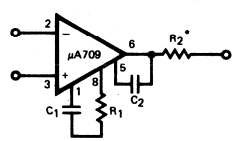
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

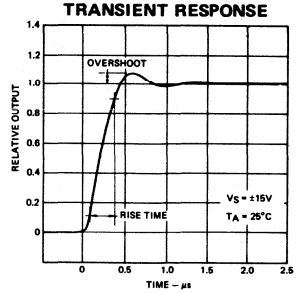


FREQUENCY COMPENSATION CIRCUIT

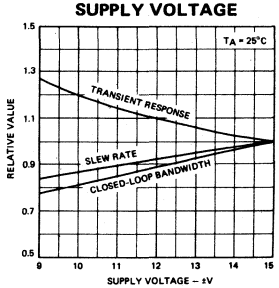


*Use R2 = 50 Ω when the amplifier is operated with capacitive loading.

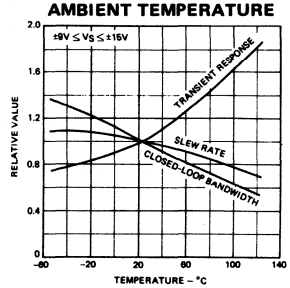
TRANSIENT RESPONSE



FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

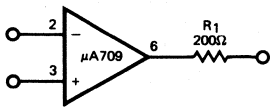


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

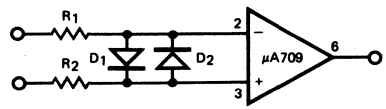


PROTECTION CIRCUITS

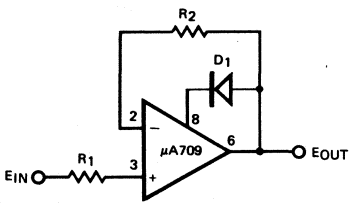
OUTPUT SHORT CIRCUIT PROTECTION



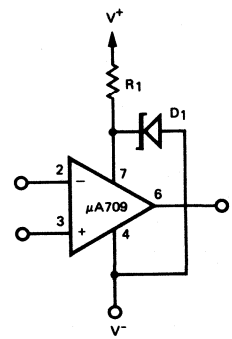
INPUT BREAKDOWN PROTECTION



LATCH-UP PROTECTION

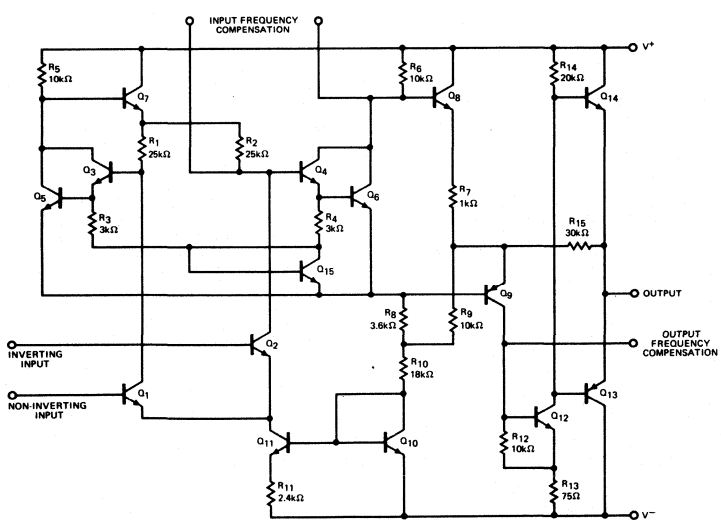


SUPPLY OVERVOLTAGE PROTECTION



Pin numbers apply to metal can or mini DIP package only.

EQUIVALENT CIRCUIT



μA715
HIGH SPEED OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

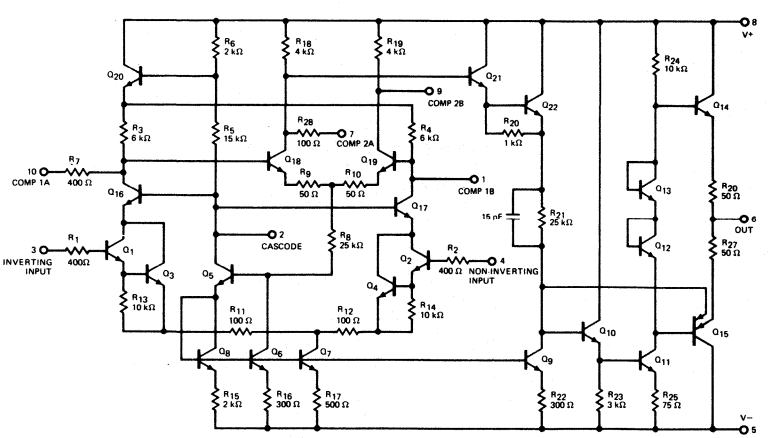
GENERAL DESCRIPTION – The μA715 is a High Speed, High Gain, monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715 features fast settling time, high slew rate, low offsets and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715 is ideally suited for use in A/D and D/A converters, active filters, deflection amplifiers, video amplifiers, phase locked-loops, multiplexed analog gates, precision comparators, sample and holds and general feedback applications requiring dc wide bandwidth operation.

- **HIGH SLEW RATE – 100 V/μs**
- **FAST SETTLING TIME – 800 ns**
- **WIDE BANDWIDTH – 65 MHz**
- **WIDE OPERATING SUPPLY RANGE**
- **WIDE INPUT VOLTAGE RANGES**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±15 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Operating Temperature Range	
Military (μA715)	−55°C to +125°C
Commercial (μA715C)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, DIP	300°C

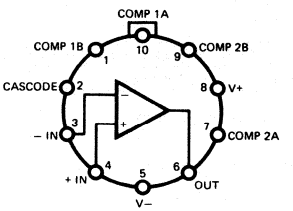
EQUIVALENT CIRCUIT



All pin numbers shown refer to 10-Lead TO-5 package.

CONNECTION DIAGRAMS

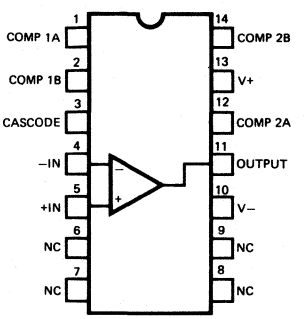
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5N
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA715	μA715HM
μA715C	μA715HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA715	μA715DM
μA715C	μA715DC

12

Notes on following pages.

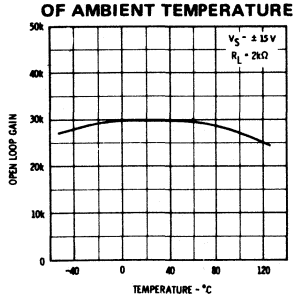
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS FOR μA715 (V_S = ± 15 V, T_A = 25°C unless otherwise specified)

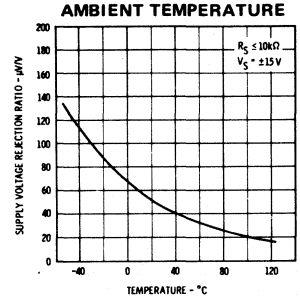
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		R_S ≤10 kΩ		2.0	5.0	mV
Input Offset Current				70	250	nA
Input Bias Current				400	750	nA
Input Resistance				1.0		MΩ
Input Voltage Range			±10	±12		V
Large Signal Voltage Gain		R_L ≥2 kΩ, V_{OUT} = ±10 V	15,000	30,000		
Output Resistance				75		Ω
Supply Current				5.5	7.0	mA
Power Consumption				165	210	mW
Settling Time (Unity Gain)		V_{OUT} = +5 V		800		ns
Transient Response (Unity Gain)	Rise Time	V_{IN} = 400 mV		30	60	ns
	Overshoot			25	40	%
Slew Rate		Av = 100		70		V/μs
		Av = 10		38		V/μs
		Av = 1 (non-inverting)	15	18		V/μs
		Av = 1 (inverting)		100		V/μs
The following apply for −55°C ≤ T_A ≤ +125°C:						
Input Offset Voltage		R_S ≤10 kΩ			7.5	mV
Input Offset Current		T_A = +125°C			250	nA
		T_A = −55°C			800	nA
Input Bias Current		T_A = +125°C			750	nA
		T_A = −55°C			4.0	μA
Common Mode Rejection Ratio		R_S ≤10 kΩ	74	92		dB
Supply Voltage Rejection Ratio		R_S ≤10 kΩ		45	300	μV/V
Large Signal Voltage Gain		R_L ≥2 kΩ, V_{OUT} = ±10 V	10,000			
Output Voltage Swing		R_L ≥2 kΩ	±10	±13		

TYPICAL PERFORMANCE CURVES FOR μA715

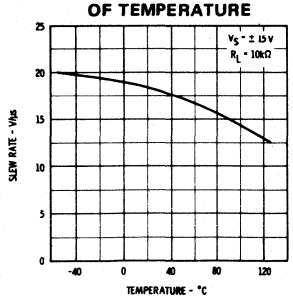
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



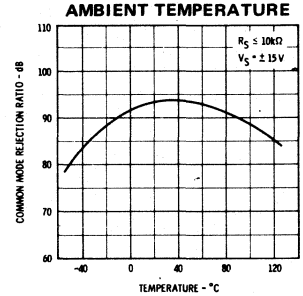
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

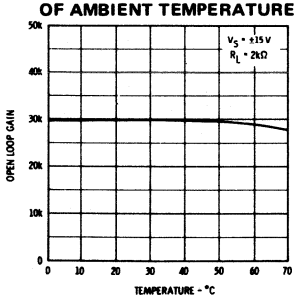


ELECTRICAL CHARACTERISTICS FOR μA715C (V_S = ±15 V, T_A = 25°C, unless otherwise specified)

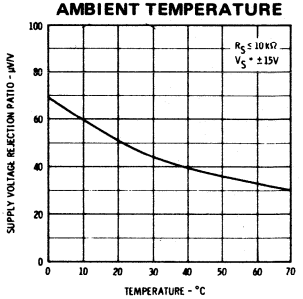
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	7.5	mV
Input Offset Current				70	250	nA
Input Bias Current				0.4	1.5	μA
Input Resistance				1.0		MΩ
Input Voltage Range			±10	±12		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	74	92		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		45	400	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	10,000	30,000		
Output Resistance				75		Ω
Supply Current				5.5	10	mA
Power Consumption				165	300	mW
Settling Time (Unity Gain)		V_{OUT} = +5 V		800		ns
Transient Response (Unity Gain)	Rise Time	V_{IN} = 400 mV		30	75	ns
	Overshoot			25	50	%
Slew Rate		A_V = 100		70		V/μs
		A_V = 10		38		V/μs
		A_V = 1 (non-inverting)	10	18		V/μs
		A_V = 1 (inverting)		100		V/μs
The following apply for 0°C ≤ T_A ≤ +70°C:						
Input Offset Voltage		$R_S \leq 10$ kΩ			10	mV
Input Offset Current		T_A = +70°C			250	nA
		T_A = 0°C			750	nA
Input Bias Current		T_A = +70°C			1.5	μA
		T_A = 0°C			7.5	μA
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	8,000			
Output Voltage Swing		$R_L \geq 2$ kΩ	±10	±13		V

TYPICAL PERFORMANCE CURVES FOR μA715C

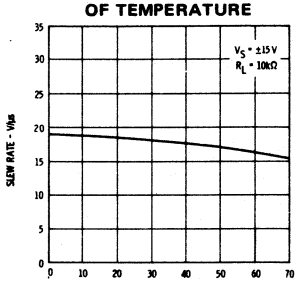
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



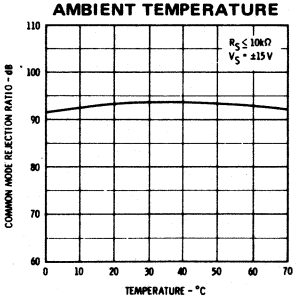
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE

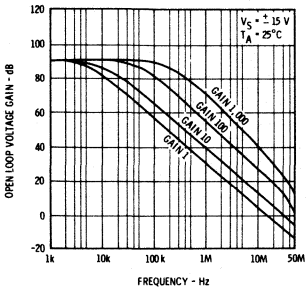


COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

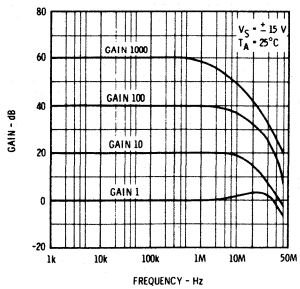


TYPICAL PERFORMANCE CURVES FOR μA715 AND μA715C

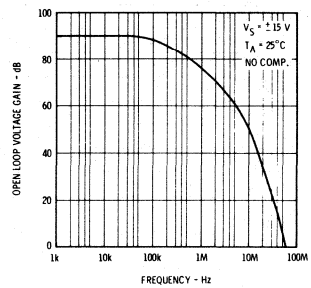
OPEN LOOP RESPONSE WITH COMPENSATION NECESSARY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



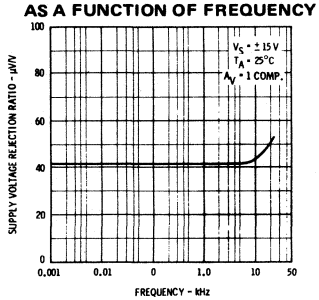
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



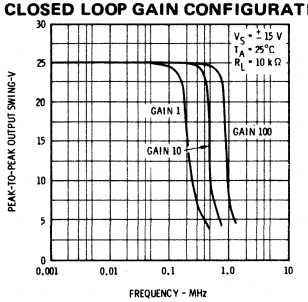
OPEN LOOP GAIN AS A FUNCTION OF FREQUENCY



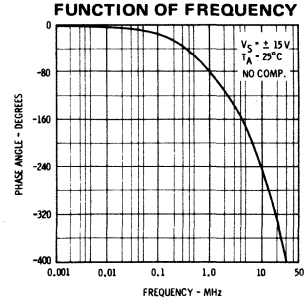
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF FREQUENCY



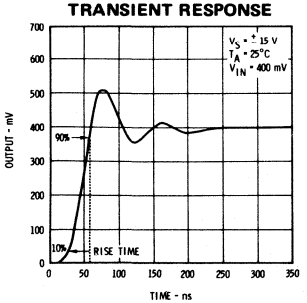
OUTPUT SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



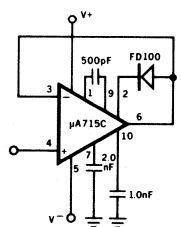
OPEN LOOP PHASE AS A FUNCTION OF FREQUENCY



VOLTAGE FOLLOWER TRANSIENT RESPONSE

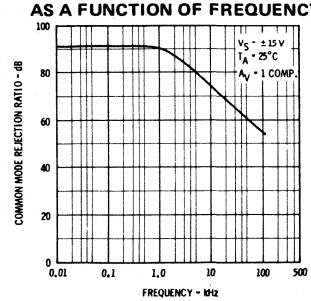


VOLTAGE FOLLOWER



Pin numbers apply to metal can.

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



NOTES
1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and 8.3 mW/°C for the DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

LAYOUT INSTRUCTIONS

LAYOUT — The layout should be such that stray capacitance is minimal.

SUPPLIES — The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

RINGING — Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.

LATCH-UP — This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode towards pin 2 is the recommended preventive measure.

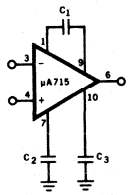
TYPICAL PERFORMANCE CURVES FOR μA715 AND μA715C

NON-INVERTING COMPENSATION COMPONENTS VALUES

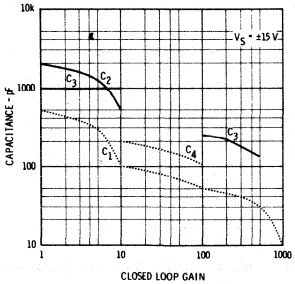
CLOSED LOOP GAIN	C1	C2	C3
1000	10 pF		
100	50 pF		250 pF
10 *	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

*For Gain 10, compensation may be simplified by removing C2, C3 and adding a 200 pF capacitor (C4) between Pin 7 and 10.

FREQUENCY COMPENSATION CIRCUIT

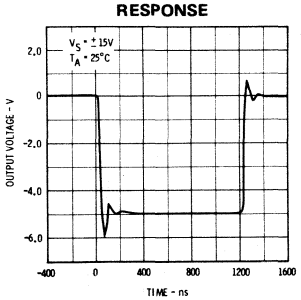


SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP GAIN

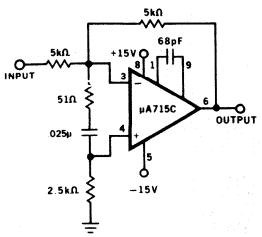


INVERTING UNITY GAIN

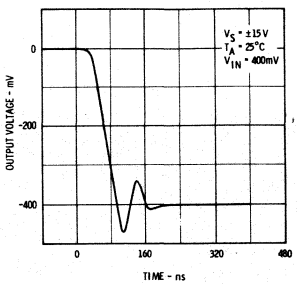
LARGE SIGNAL PULSE RESPONSE



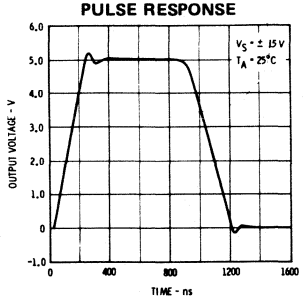
HIGH SLEW RATE CIRCUIT



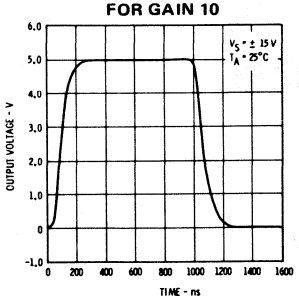
SMALL SIGNAL PULSE RESPONSE INVERTING UNITY GAIN



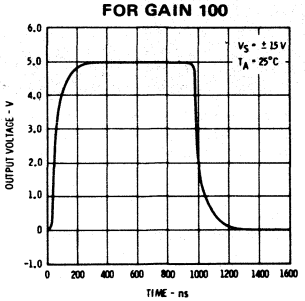
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



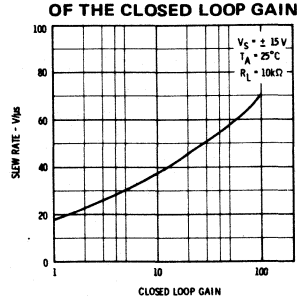
LARGE SIGNAL PULSE RESPONSE FOR GAIN 10



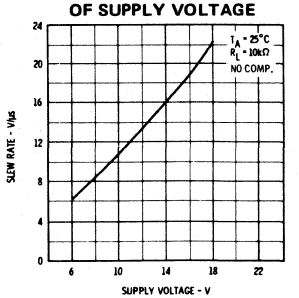
LARGE SIGNAL PULSE RESPONSE FOR GAIN 100



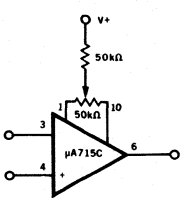
SLEW RATE AS A FUNCTION OF THE CLOSED LOOP GAIN



SLEW RATE AS A FUNCTION OF SUPPLY VOLTAGE



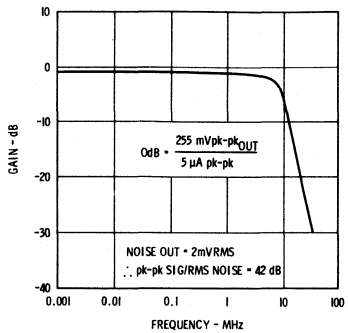
VOLTAGE OFFSET NULL CIRCUIT

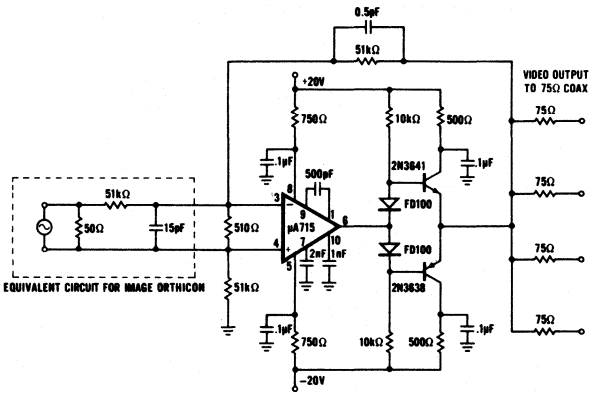


Pin numbers apply to metal can.

TYPICAL APPLICATIONS

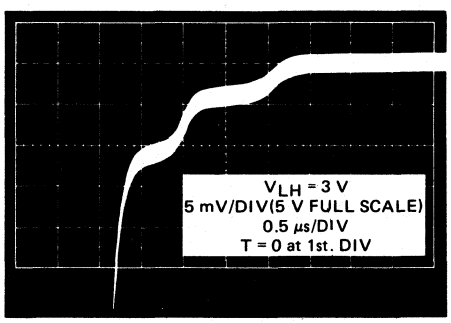
WIDE BAND VIDEO AMPLIFIER WITH 75 Ω COAX CABLE DRIVE CAPABILITY



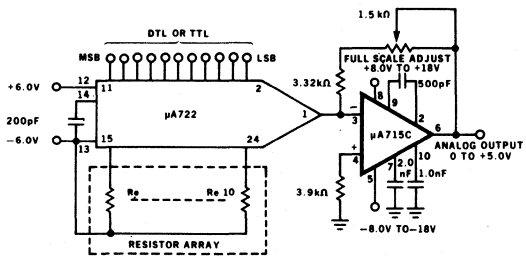


HIGH SPEED 10-BIT DIGITAL TO ANALOG CONVERTER

ANALOG OUTPUT 0 TO +5.0 V



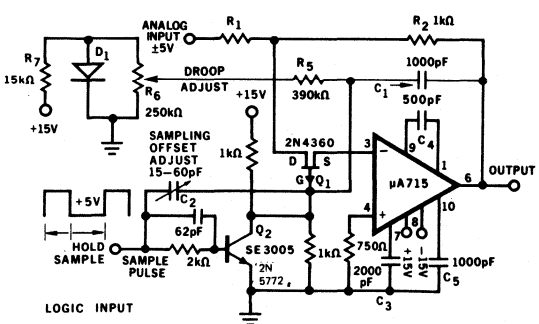
μA722/μA715 op amp switching ON, as it should with typical logic voltage on least significant bits. Note complete absence of ringing.



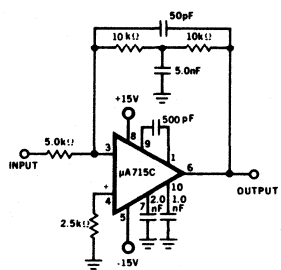
Conversion Rate
6 bits - 300 ns
8 bits - 600 ns
10 bits - 1000 ns

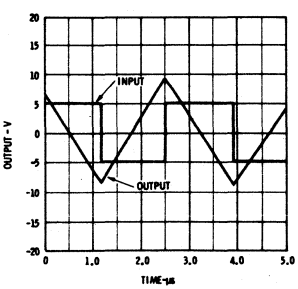
NOTE:
Contact Fairchild for additional information including how to increase conversion speed by clamping LSB's and how to obtain bipolar outputs.

HIGH SPEED SAMPLE AND HOLD



HIGH SPEED INTEGRATOR





μA725

INSTRUMENTATION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA725 is a monolithic Instrumentation Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725 is pin compatible with the popular μA741 operational amplifier.

- **LOW INPUT NOISE CURRENT – 0.15 pA/$\sqrt{\text{Hz}}$**
- **HIGH OPEN LOOP GAIN – 3,000,000**
- **LOW INPUT OFFSET CURRENT – 2 nA**
- **LOW INPUT VOLTAGE DRIFT – 0.6 μV/°C**
- **HIGH COMMON MODE REJECTION – 120 dB**
- **HIGH INPUT VOLTAGE RANGE – ±14 V**
- **WIDE POWER SUPPLY RANGE – ±3 V TO ±22 V**
- **OFFSET NULL CAPABILITY**

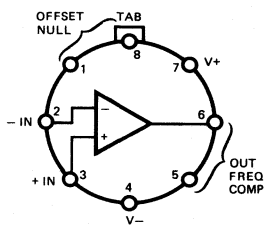
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±22 V
Voltage Between Offset Null and V^+	±0.5 V
Storage Temperature Range	
Metal Can	−65°C to +150°C
Operating Temperature Range	
Military (μA725A, μA725)	−55°C to +125°C
Commercial (μA725E, μA725C)	0°C to +70°C
Lead Temperature	
Metal Can (Soldering, 60 Seconds)	300°C

CONNECTION DIAGRAM

8-LEAD METAL CAN
(TOP VIEW)

PACKAGE OUTLINE 5S
PACKAGE CODE H

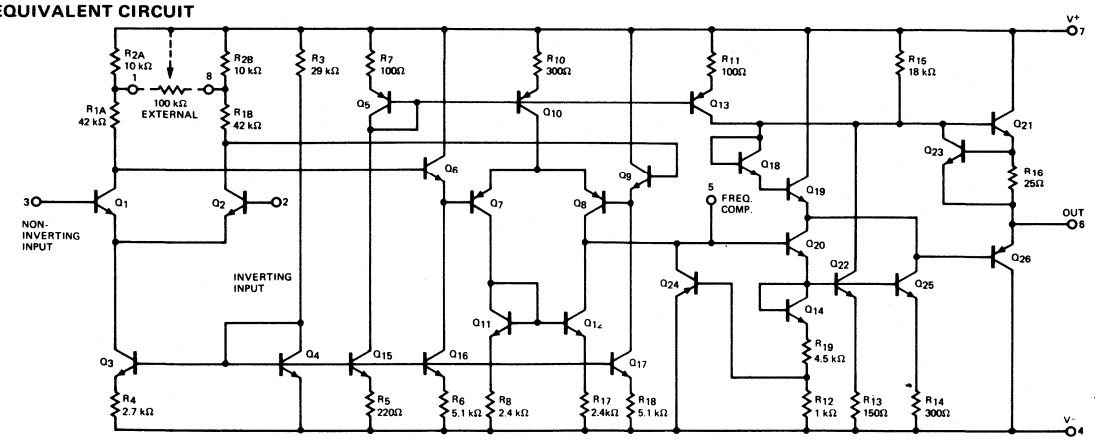


ORDER INFORMATION

TYPE	PART NO.
μA725A	μA725AHM
μA725	μA725HM
μA725C	μA725HC
μA725E	μA725EHC

12

EQUIVALENT CIRCUIT



Notes on following pages

*Planar is a patented Fairchild process.

μA725A

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

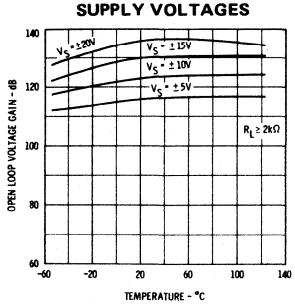
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.5	mV
Input Offset Current				5.0	nA
Input Bias Current				75	nA
Input Noise Voltage	f_o = 10 Hz			15	nV/√Hz
	f_o = 100 Hz			12	nV/√Hz
	f_o = 1 kHz			12	nV/√Hz
Input Noise Current	f_o = 10 Hz			1.2	pA/√Hz
	f_o = 100 Hz			0.6	pA/√Hz
	f_o = 1 kHz			0.25	pA/√Hz
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	1,000,000	3,000,000		V/V
	$R_L \geq 500$ Ω, V_{OUT} = ±0.5 V, V_S = ±3 V	100,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	120	130		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	5.0	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12.5			V
	$R_L \geq 2$ kΩ	±10			V
Output Resistance			150		Ω
Power Consumption			80	120	mW
	V_S = ±3 V			6.0	mW

The following specifications apply for $-55°C \leq T_A \leq +125°C$ unless otherwise specified:

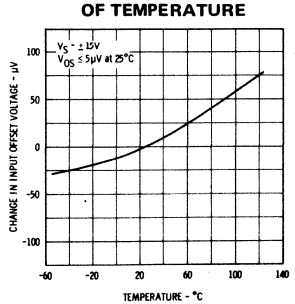
Input Offset Voltage (Without External trim)	$R_S \leq 10$ kΩ			0.75	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50 Ω			2.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50 Ω		0.6	1.0	μV/°C
Input Offset Current	T_A = +125°C			4.0	nA
	T_A = −55°C		5.0	18	nA
Average Input Offset Current Drift				90	pA/°C
Input Bias Current	T_A = +125°C			70	nA
	T_A = −55°C			180	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, T_A = +125°C	1,000,000			V/V
	$R_L \geq 2$ kΩ, T_A = −55°C	500,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	110			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			8.0	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES FOR μA725A AND μA725

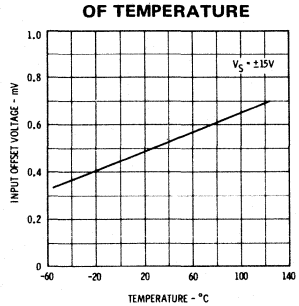
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



μA725

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	1.0	mV
Input Offset Current			2.0	20	nA
Input Bias Current			42	100	nA
Input Noise Voltage	f_o = 10 Hz		15		nV/$\sqrt{Hz}$
	f_o = 100 Hz		9.0		nV/$\sqrt{Hz}$
	f_o = 1 kHz		8.0		nV/$\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz		1.0		pA/$\sqrt{Hz}$
	f_o = 100 Hz		0.3		pA/$\sqrt{Hz}$
	f_o = 1 kHz		0.15		pA/$\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq$ 2 kΩ, V_{OUT} = ±10 V	1,000,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	110	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq$ 2 kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	105	mW
The following specifications apply for $-55°C \leq T_A \leq +125°C$ unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			1.5	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50Ω		2.0	5.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50Ω		0.6		μV/°C
Input Offset Current	T_A = +125°C		1.2	20	nA
	T_A = −55°C		7.5	40	nA
Average Input Offset Current Drift			35	150	pA/°C
Input Bias Current	T_A = +125°C		20	100	nA
	T_A = −55°C		80	200	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, T_A = +125°C	1,000,000			V/V
	$R_L \geq 2$ kΩ, T_A = −55°C	250,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	100			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			20	μV/V
Output Voltage Swing	$R_L \geq$ 2 kΩ	±10			V

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C.
2. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

12

μA725E

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

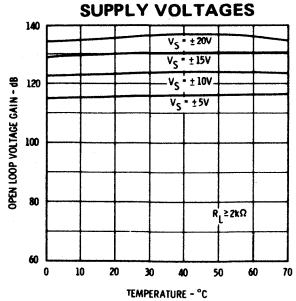
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.5	mV
Input Offset Current				5.0	nA
Input Bias Current				75	nA
Input Noise Voltage	f_o = 10 Hz			15	nV/√Hz
	f_o = 100 Hz			12	nV/√Hz
	f_o = 1 kHz			12	nV/√Hz
Input Noise Current	f_o = 10 Hz			1.2	pA/√Hz
	f_o = 100 Hz			0.6	pA/√Hz
	f_o = 1 kHz			0.25	pA/√Hz
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	1,000,000	3,000,000		V/V
	$R_L \geq 500$ Ω, V_{OUT} = ±0.5 V, V_S = ±3 V	100,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	120			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	5.0	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12.5			V
	$R_L \geq 2$ kΩ	±10			V
Output Resistance			150		Ω
Power Consumption			80	150	mW
	V_S = ±3 V			6.0	mW

The following specifications apply for 0°C ≤ T_A ≤ +70°C unless otherwise specified:

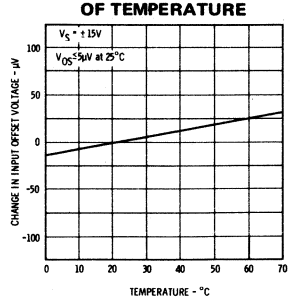
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.75	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50 Ω			2.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50 Ω			1.0	μV/°C
Input Offset Current	T_A = +70°C		1.2	4.0	nA
	T_A = 0°C		4.0	18	nA
Average Input Offset Current Drift			10	90	pA/°C
Input Bias Current	T_A = +70°C			70	nA
	T_A = 0°C			180	nA
Large Signal Voltage	$R_L \geq 2$ kΩ, T_A = +70°C	1,000,000			V/V
	$R_L \geq 2$ kΩ, T_A = 0°C	500,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	110			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			8.0	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES FOR μA725E AND μA725C

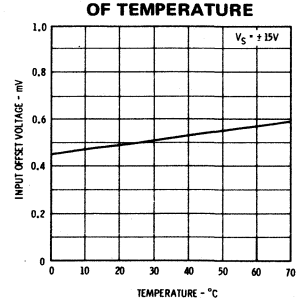
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



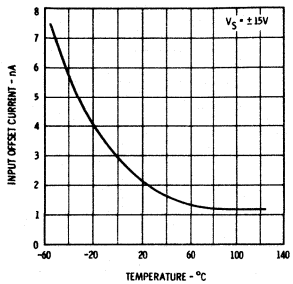
μA725C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

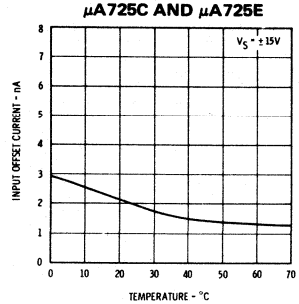
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	2.5	mV
Input Offset Current			2.0	35	nA
Input Bias Current			42	125	nA
Input Noise Voltage	f_o = 10 Hz		15		nV/$\sqrt{Hz}$
	f_o = 100 Hz		9.0		nV/$\sqrt{Hz}$
	f_o = 1 kHz		8.0		nV/$\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz		1.0		pA/$\sqrt{Hz}$
	f_o = 100 Hz		0.3		pA/$\sqrt{Hz}$
	f_o = 1 kHz		0.15		pA/$\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	250,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	94	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	35	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	150	mW
The following specifications apply for 0°C ≤ T_A ≤ +70°C unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			3.5	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50Ω		2.0		μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50Ω		0.6		μV/°C
Input Offset Current	T_A = +70°C		1.2	35	nA
	T_A = 0°C		4.0	50	nA
Average Input Offset Current Drift			10		pA/°C
Input Bias Current	T_A = +70°C			125	nA
	T_A = 0°C			250	nA
Large Signal Voltage	$R_L \geq 2$ kΩ, T_A = +70°	125,000			V/V
	$R_L \geq 2$ kΩ, T_A = 0°C	125,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ		115		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		20		μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES FOR ALL TYPES (Unless Otherwise Specified)

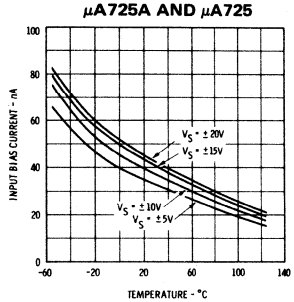
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE μA725A AND μA725



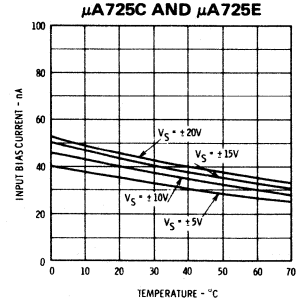
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE μA725C AND μA725E



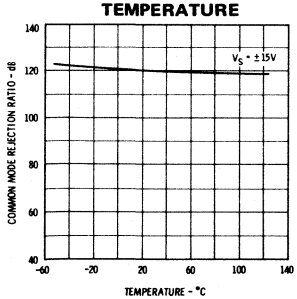
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE μA725A AND μA725



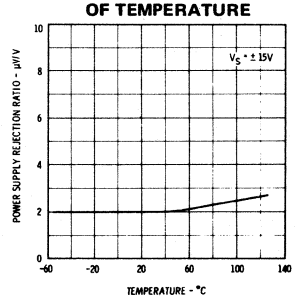
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE μA725C AND μA725E



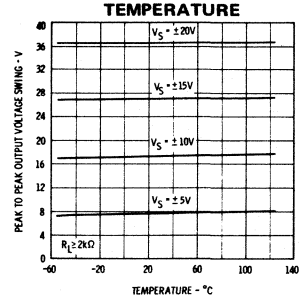
COMMON MODE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



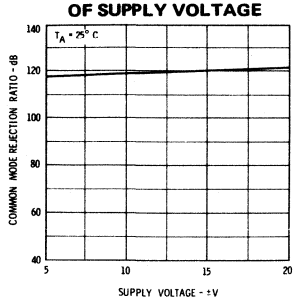
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



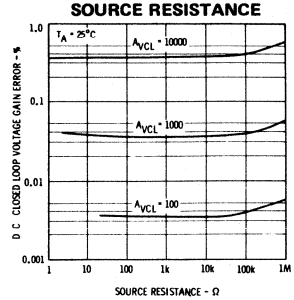
OUTPUT VOLTAGE SWING AS A FUNCTION OF TEMPERATURE



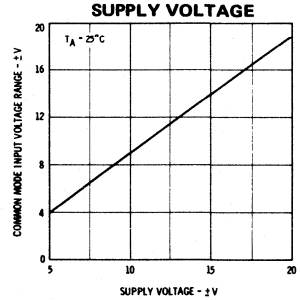
COMMON MODE REJECTION RATIO AS A FUNCTION OF SUPPLY VOLTAGE



DC CLOSED LOOP VOLTAGE GAIN ERROR AS A FUNCTION OF SOURCE RESISTANCE

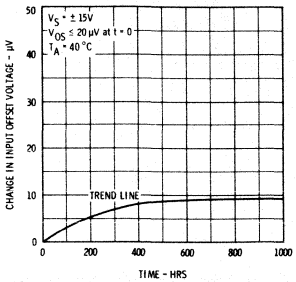


COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

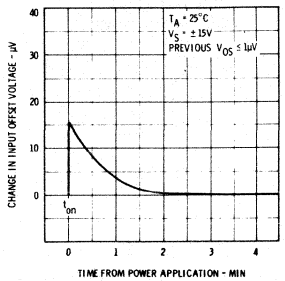


TYPICAL PERFORMANCE CURVES FOR ALL TYPES (Unless Otherwise Specified)

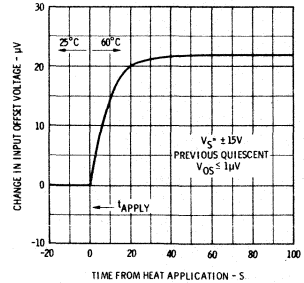
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



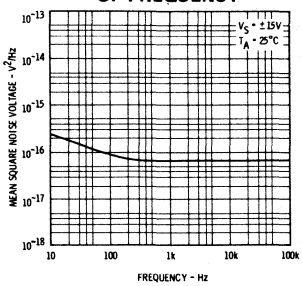
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN ON



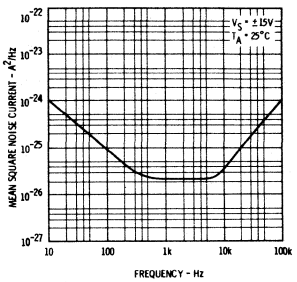
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK AS A FUNCTION OF TIME



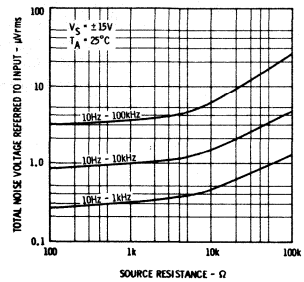
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



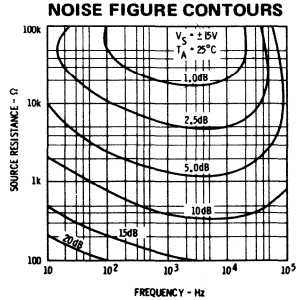
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



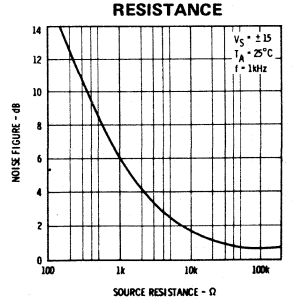
BROAD BAND NOISE FOR VARIOUS BANDWIDTHS



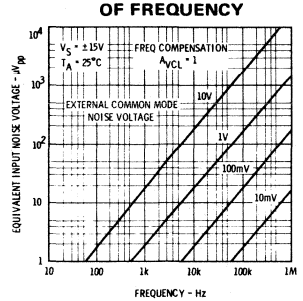
NARROW BAND SPOT NOISE FIGURE CONTOURS



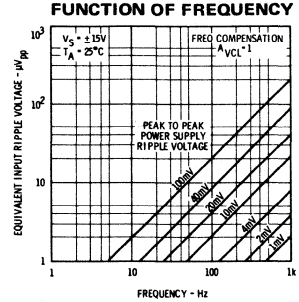
NOISE FIGURE AS A FUNCTION OF SOURCE RESISTANCE



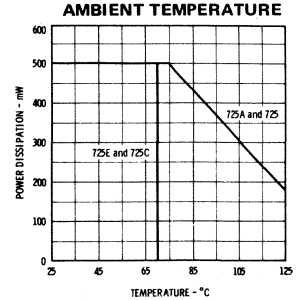
EQUIVALENT INPUT NOISE VOLTAGE DUE TO EXTERNAL COMMON MODE NOISE AS A FUNCTION OF FREQUENCY



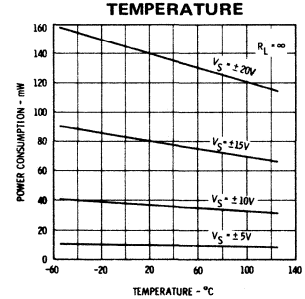
EQUIVALENT INPUT RIPPLE VOLTAGE DUE TO POWER SUPPLY RIPPLE AS A FUNCTION OF FREQUENCY



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



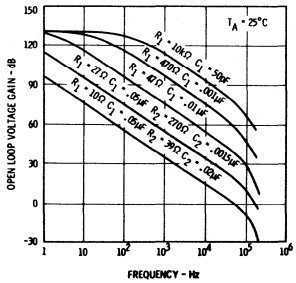
POWER CONSUMPTION AS A FUNCTION OF TEMPERATURE



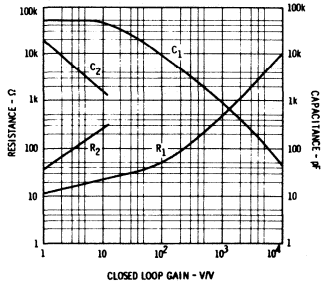
12

TYPICAL PERFORMANCE CURVES FOR ALL TYPES

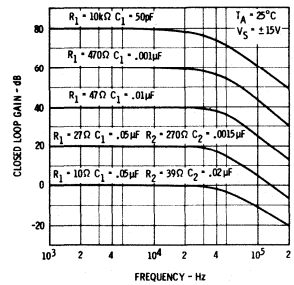
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY USING RECOMMENDED COMPENSATION NETWORKS



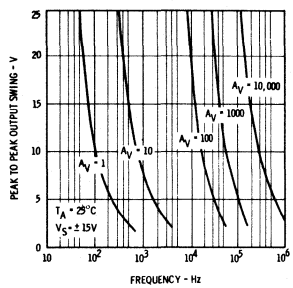
VALUES FOR SUGGESTED COMPENSATION NETWORKS FOR VARIOUS CLOSED LOOP VOLTAGE GAINS



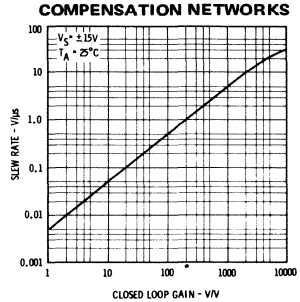
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS USING RECOMMENDED COMPENSATION NETWORKS



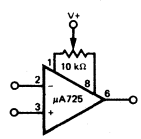
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR RECOMMENDED COMPENSATION NETWORKS



SLEW RATE AS A FUNCTION OF CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



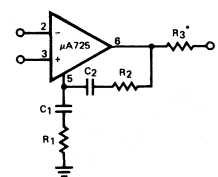
VOLTAGE OFFSET NULL CIRCUIT



COMPENSATION COMPONENT VALUES

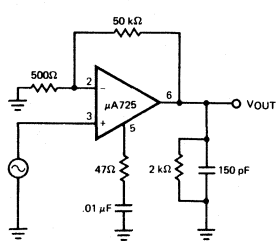
A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

FREQUENCY COMPENSATION CIRCUIT



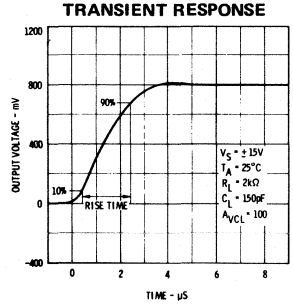
*Use $R_3 = 51\Omega$ when the amplifier is operated with capacitive load.

TRANSIENT RESPONSE TEST CIRCUIT



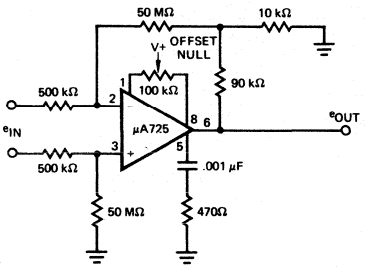
Pin numbers are shown for metal can only.

TRANSIENT RESPONSE



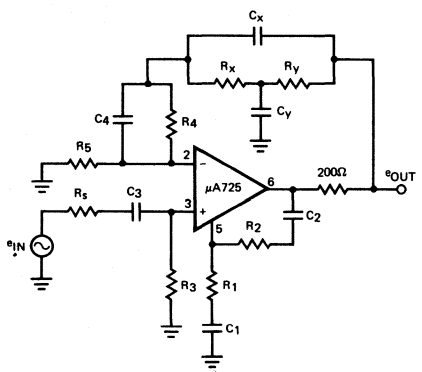
TYPICAL APPLICATIONS

PRECISION AMPLIFIER – A_{VCL} = 1000

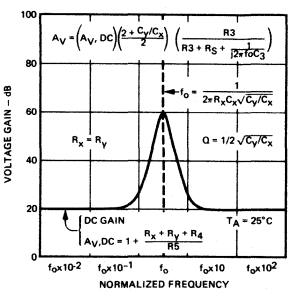


CHARACTERISTICS:
- A_V = 1000 = 60 dB
- DC Gain Error = 0.05%
- Bandwidth = 1 kHz for −0.05% error
- Diff. Input Res. = 1 MΩ
- Typical amplifying capability
  - e_{IN} = 10 μV on V_{CMI} = 1.0 V
- Caution: Minimize Stray Capacitance

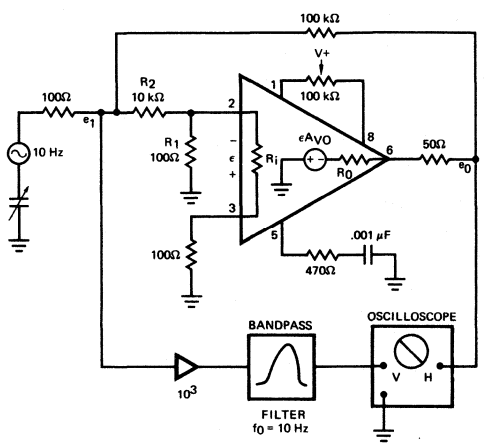
ACTIVE FILTER – BAND PASS WITH 60 dB GAIN



ACTIVE FILTER FREQUENCY RESPONSE



OPEN LOOP VOLTAGE GAIN TEST CIRCUIT

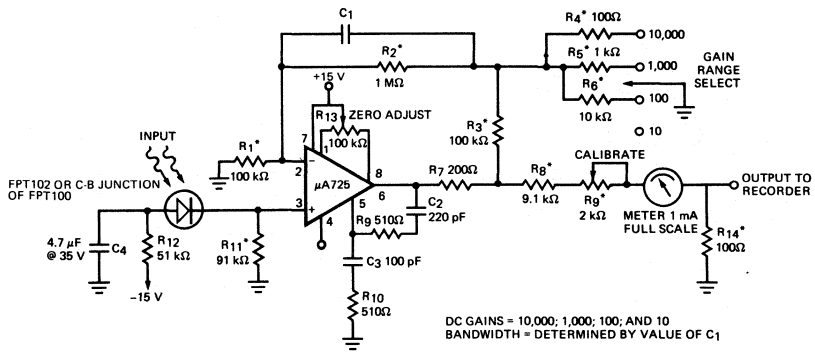


$$A_{VO} \triangleq \frac{e0}{e_1}\left(\frac{R2\,Ri + R1\,R_i + R1\,R2}{R1\,R_i}\right) = \frac{e_0}{e_1}\,101$$

12

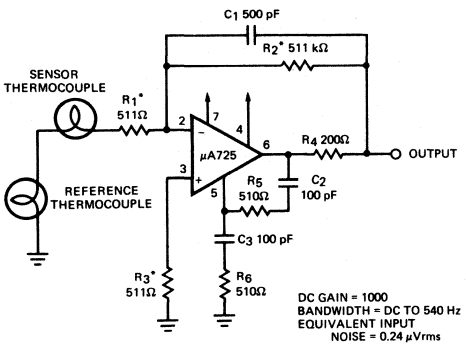
TYPICAL APPLICATIONS (Cont'd)

PHOTODIODE AMPLIFIER



NOTE: *Indicates ±1% metal film resistors recommended for temperature stability.

THERMOCOUPLE AMPLIFIER



NOTE: *Indicates ±1 % metal film resistors recommended for temperature stability.

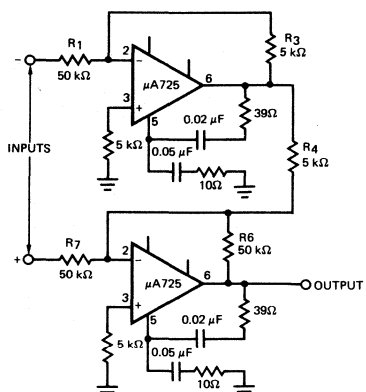
$$\frac{R1}{R6} = \frac{R3}{R4} \text{ for best CMRR}$$

$$R3 = R4$$

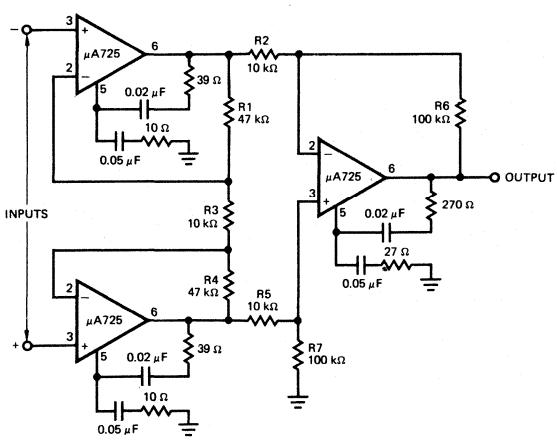
$$R1 = R6 = 10\ R3$$

$$\text{Gain} = \frac{R6}{R7}$$

±100 V COMMON MODE RANGE DIFFERENTIAL AMPLIFIER



INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$$\frac{R2}{R5} = \frac{R6}{R7} \text{ for best CMR}$$

$$R1 = R4$$

$$R2 = R5$$

$$\text{Gain} = \frac{R6}{R2}\left(1 + \frac{2\,R1}{R3}\right)$$

μA727

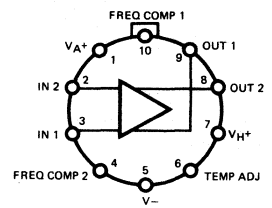
TEMPERATURE CONTROLLED DIFFERENTIAL PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA727 is a monolithic, fixed gain, Differential Input/Output Preamplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low drift dc amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gauge transducers, and A/D converters.

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE – 300 MΩ**
- **WIDE COMMON MODE RANGE – C_{MRR} = 100 dB**

CONNECTION DIAGRAM
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5I
PACKAGE CODE H



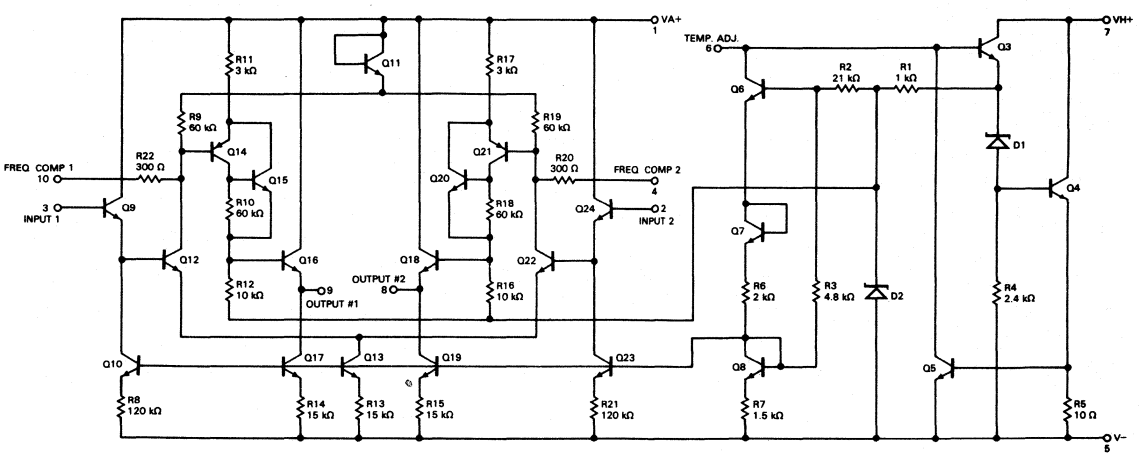
ORDER INFORMATION

TYPE	PART NO.
μA727	μA727HM
μA727C	μA727HC

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
Military (μA727)	–55°C to +125°C
Commercial (μA727C)	–20°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 s time limit)	300°C
Internal Power Dissipation	500 mW
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA727

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_{H^+} = V_{A^+} = +15$ V, $V_{-} = -15$ V, $R_{ADJ} = 330$ kΩ, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		±5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

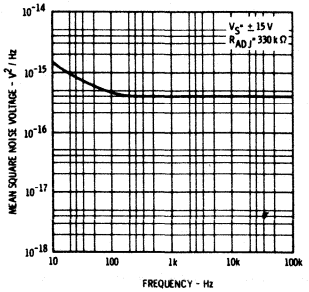
μA727C

ELECTRICAL CHARACTERISTICS ($-20°C \leq T_A \leq +85°C$, $V_{H^+} = V_{A^+} = +15$ V, $V_{-} = -15$ V, $R_{ADJ} = 1$ MΩ, unless otherwise specified)

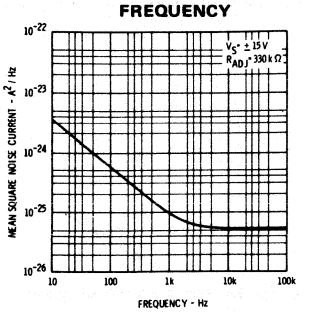
PARAMETER	CONDITONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\Omega$		0.6	3.0	μV/°C
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ	70	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−7.0	−5.0	−4.0	V
Differential Output Voltage Swing		±3.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15	μV/μA
Differential Voltage Gain		50	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL PERFORMANCE CURVES FOR μA727 AND μA727C

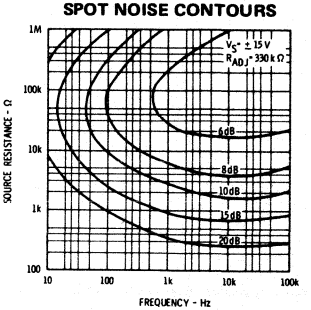
NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



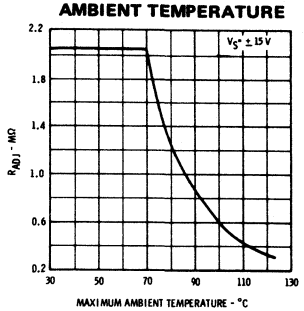
NOISE CURRENT AS A FUNCTION OF FREQUENCY



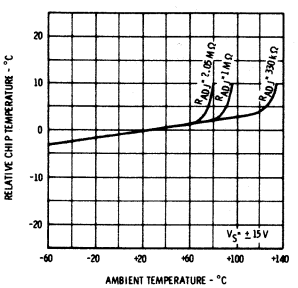
SPOT NOISE CONTOURS



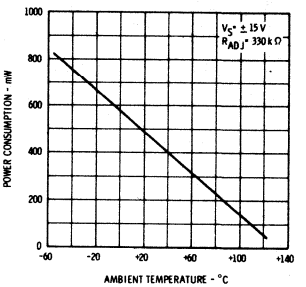
RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE



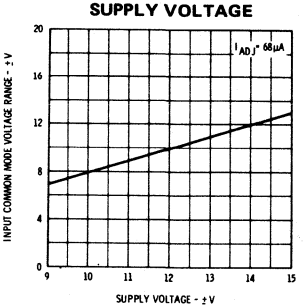
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE



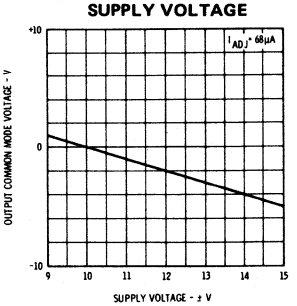
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



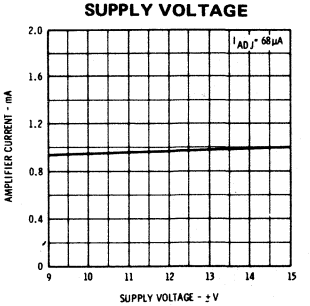
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



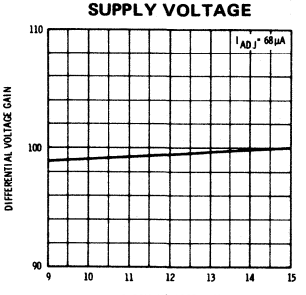
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



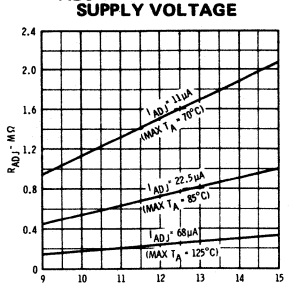
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



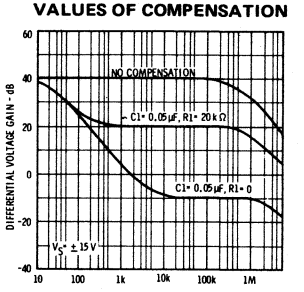
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE

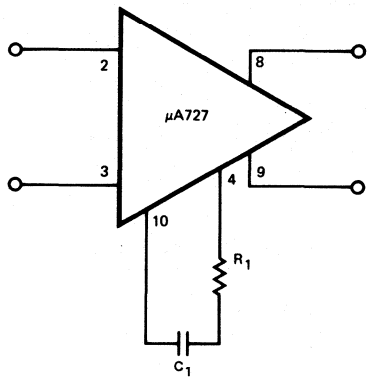


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION

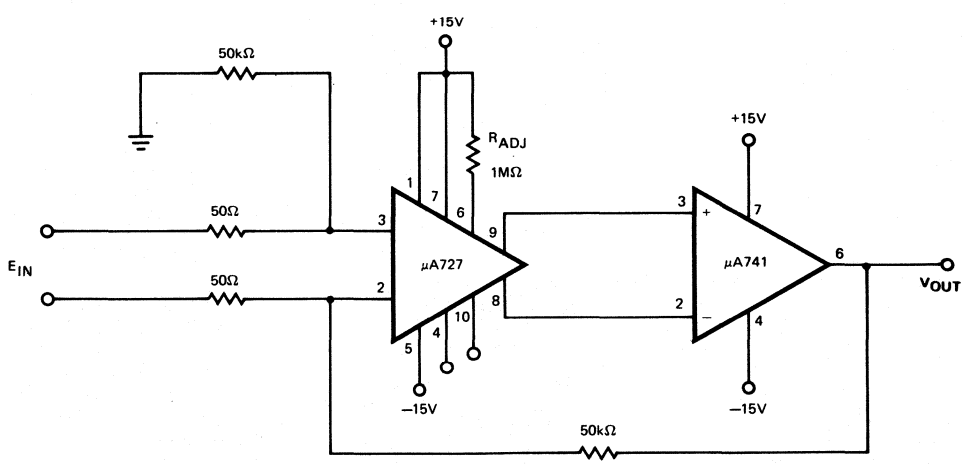


12

FREQUENCY COMPENSATION CIRCUIT



TYPICAL X1000 CIRCUIT



μA730
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

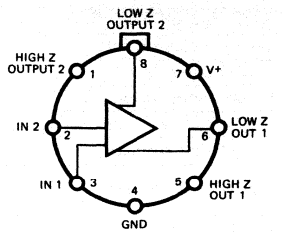
GENERAL DESCRIPTION – The μA730 is a Differential Amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Military (μA730)	−55°C to +125°C
Commercial (μA730C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 s)	300°C

NOTE:
1. Rating applies for ambient temperature to +70°C; derate linearly at 6.3 mW/°C for ambient temperatures above +70°C.

CONNECTION DIAGRAM
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



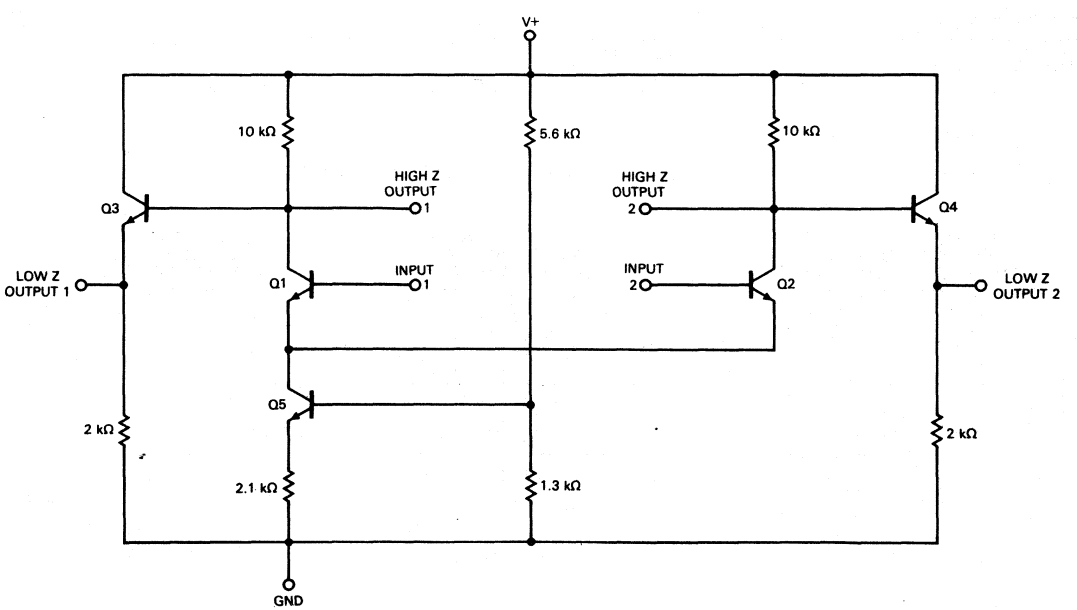
NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA730	μA730HM
μA730C	μA730HC

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



12

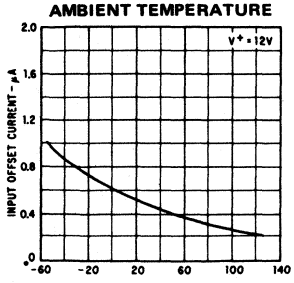
μA730

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12.0 V, and V_{CM} = 3.5 V unless otherwise specified)

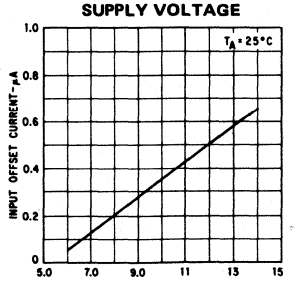
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	145	160	
Differential Distortion	$R_L \geq 100$ kΩ		80	300	mV_{pk-pk}
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		V_{pk-pk}
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	$T_A = +125°C$		0.2	1.5	μA
	$T_A = -55°C$		1.0	3.0	μA
Input Bias Current	$T_A = -55°C$		6.5	15	μA
Input Resistance		0.9			kΩ
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5V \leq V_{CM} \leq +5.2V$	70	85		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		V_{pk-pk}
Supply Current	$T_A = -55°C$		10	15	mA
	$T_A = 125°C$		8.0	11	mA
Power Consumption	$T_A = -55°C$		120	180	mW
	$T_A = 125°C$		96	121	mW

TYPICAL PERFORMANCE CURVES FOR μA730

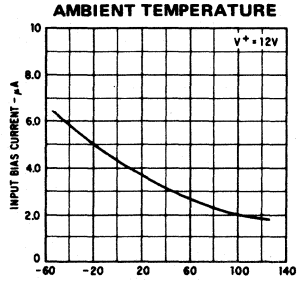
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



μA730C

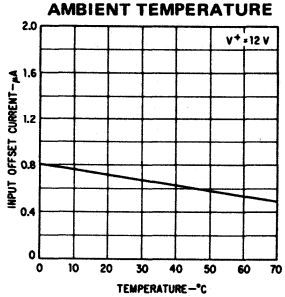
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12.0 V, and V_{CM} = 3.5 V unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	135	160	
Differential Distortion	$R_L \geq 100$ kΩ		85	300	mVp-p
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		V_{pk-pk}
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	$T_A = +70°C$		0.5	3.0	μA
	$T_A = 0°C$		0.8	5.0	μA
Input Bias Current	$T_A = 0°C$		5.0	20	μA
Input Resistance		1.8			kΩ
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5V \leq V_{CM} \leq +5.2V$	60	80		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		V_{pk-pk}
Supply Current	$T_A = 0°C$		10	15	mA
	$T_A = +70°C$		8.8	13	mA
Power Consumption	$T_A = 0°C$		120	180	mW
	$T_A = +70°C$		106	156	mW

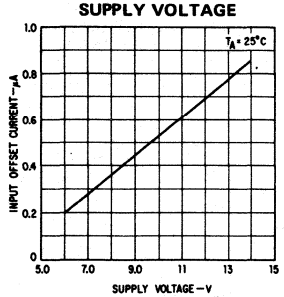
12

TYPICAL PERFORMANCE CURVES FOR μA730C

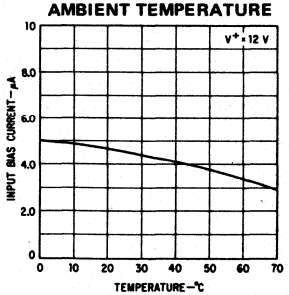
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

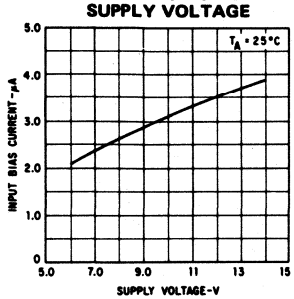


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

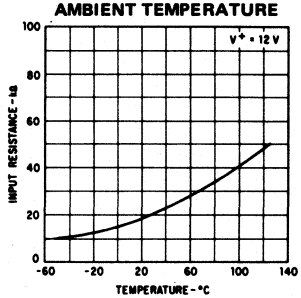


TYPICAL PERFORMANCE CURVES FOR μA730

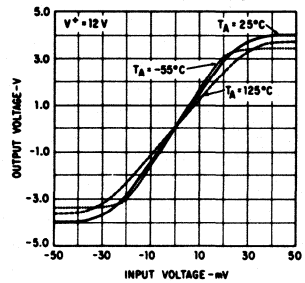
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



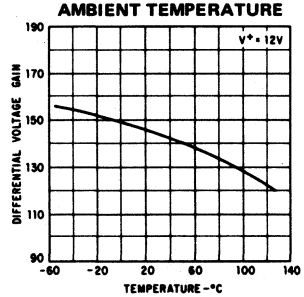
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



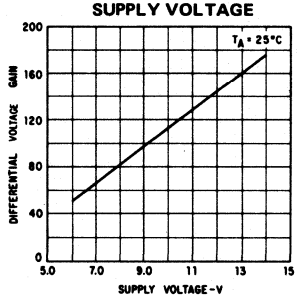
VOLTAGE TRANSFER CHARACTERISTICS



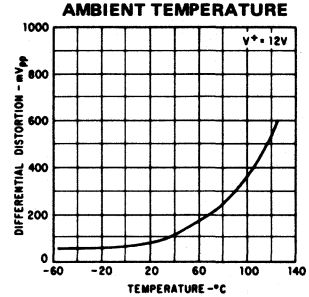
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



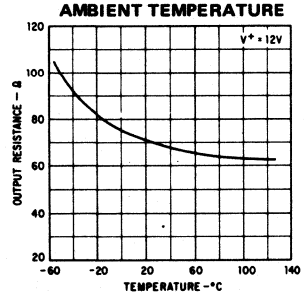
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



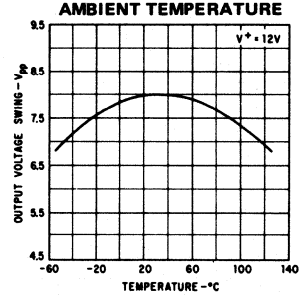
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



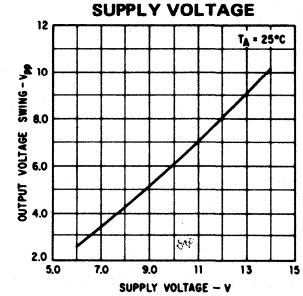
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



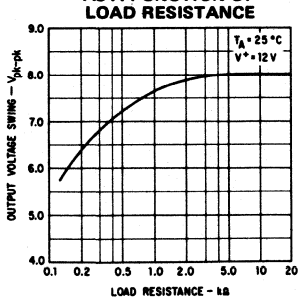
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



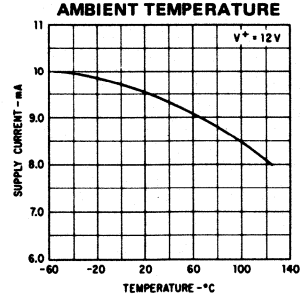
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



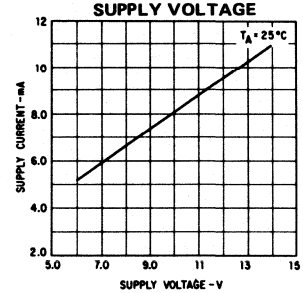
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

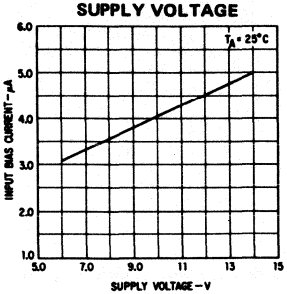


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

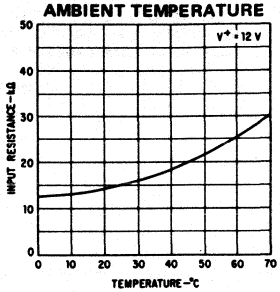


TYPICAL PERFORMANCE CURVES FOR μA730C

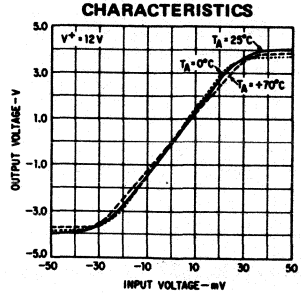
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



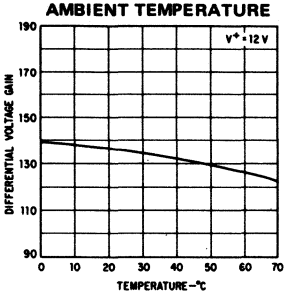
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



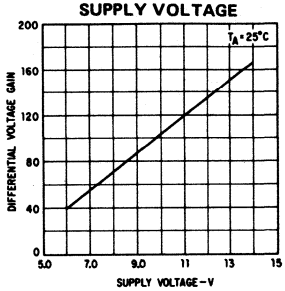
VOLTAGE TRANSFER CHARACTERISTICS



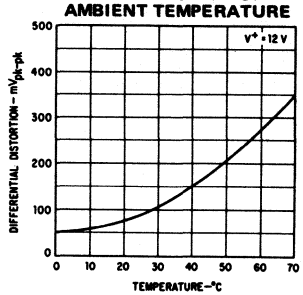
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



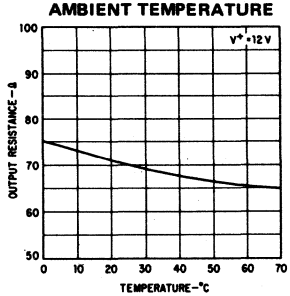
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



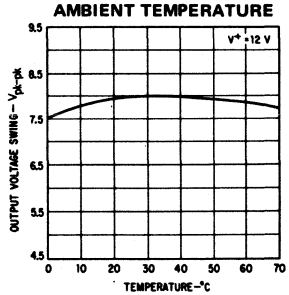
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



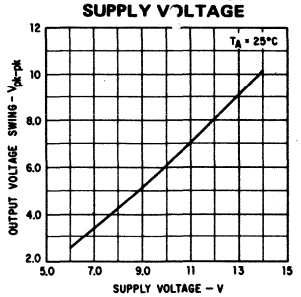
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



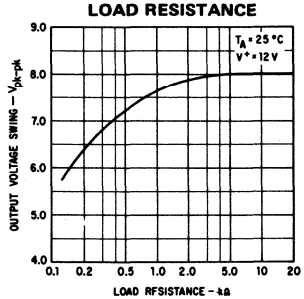
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



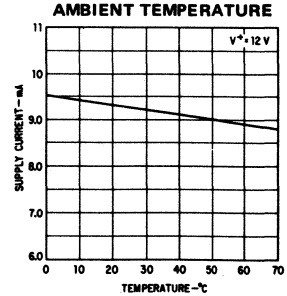
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



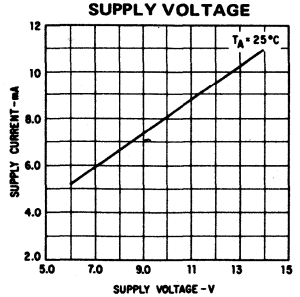
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



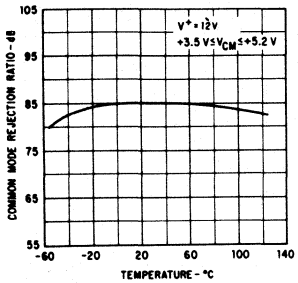
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



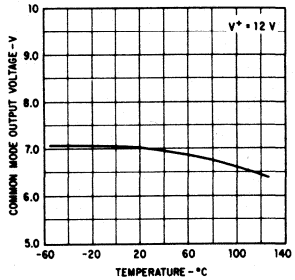
12

TYPICAL PERFORMANCE CURVES FOR μA730 AND μA730C

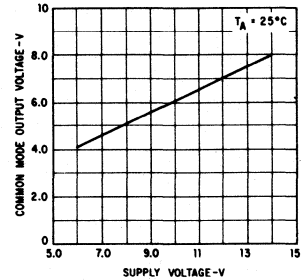
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



μA739

DUAL LOW NOISE AUDIO PREAMPLIFIER/OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

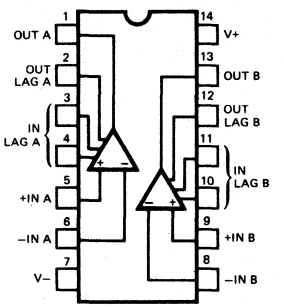
GENERAL DESCRIPTION – The μA739 consists of two identical monolithic Operational Amplifiers using the Fairchild Planar* epitaxial process. These low noise, high gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltages and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	670 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Hermetic	−65°C to +150°C
Molded	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P

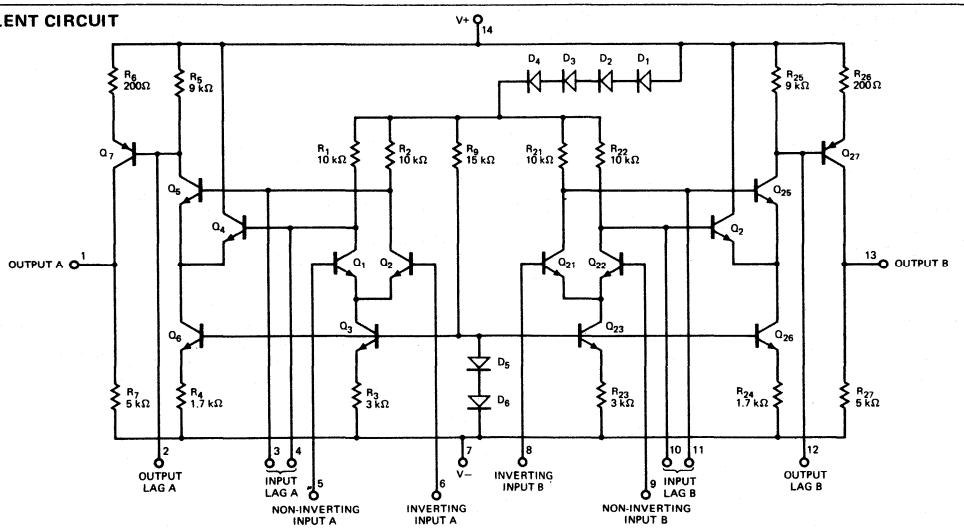


ORDER INFORMATION

TYPE	PART NO.
μA739C	μA739DC
μA739C	μA739PC

12

EQUIVALENT CIRCUIT



Notes on following page

*Planar is a patented Fairchild process.

μA739C

ELECTRICAL CHARACTERISTICS (V_S = ±15V, R_L = 50kΩ to Pin 7, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±5.0V	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0kHz		5.0		kΩ
Input Voltage Range		±10	±11		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		50		μV/V
Power Consumption	V_{OUT} = 0		270	420	mW
Supply Current	V_{OUT} = 0		9.0	14	mA
Broadband Noise Figure	R_S = 5.0kΩ, BW = 10Hz to 10kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, V_{IN} = ±20mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, V_{IN} = ±20mV		0.3		μs
Slew Rate (unity gain) [See Figure 2]	C_1 = 0.1μF, R_1 = 4.7Ω		1.0		V/μs
Channel Separation (See Figure 3)	$R_S \leq 10k\Omega$, f = 10kHz		140		dB
The following specifications apply for V_S = ±4.0V, T_A = 25°C					
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	V_{OUT} = 0		2.5		mA
Power Consumption	V_{OUT} = 0		20		mW
Large Signal Voltage Gain	V_{OUT} = ±1.0V	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES:

1. Rating applies at ambient temperature below 70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

PULSE RESPONSE WAVEFORMS

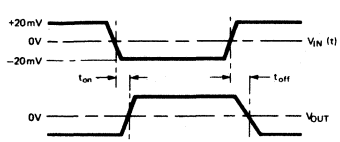


Fig. 1

FREQUENCY RESPONSE TEST CIRCUIT

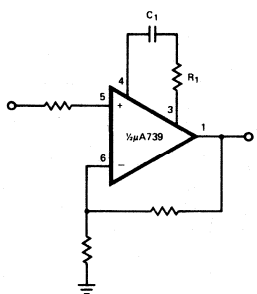


Fig. 2

CHANNEL SEPARATION TEST CIRCUIT

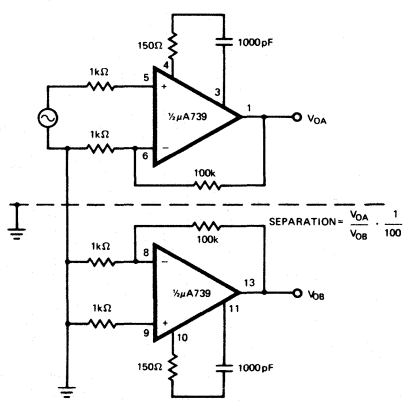
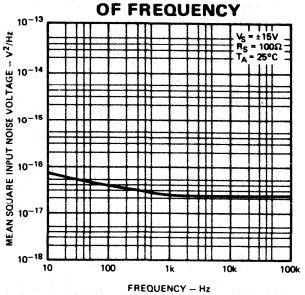


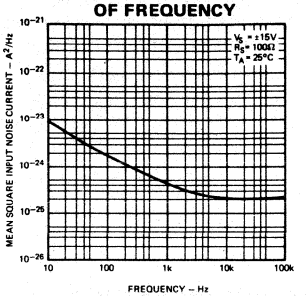
Fig. 3

TYPICAL PERFORMANCE CURVES FOR μA739C

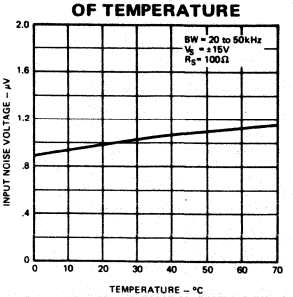
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



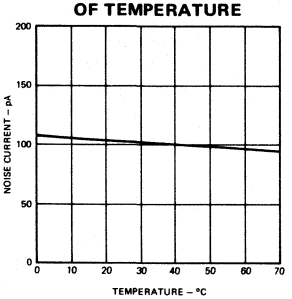
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



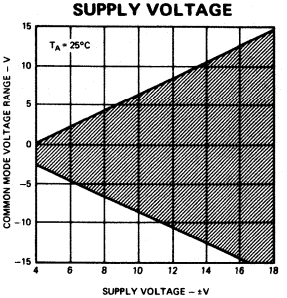
WIDE BAND INPUT NOISE VOLTAGE AS A FUNCTION OF TEMPERATURE



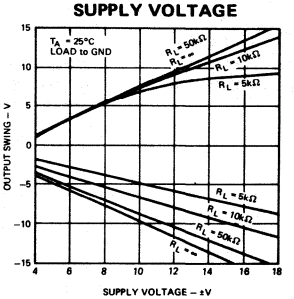
WIDE BAND INPUT NOISE CURRENT AS A FUNCTION OF TEMPERATURE



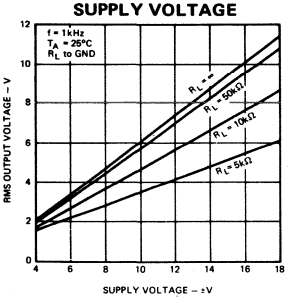
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



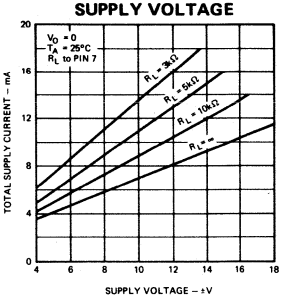
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



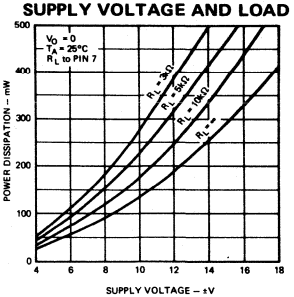
OUTPUT CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE



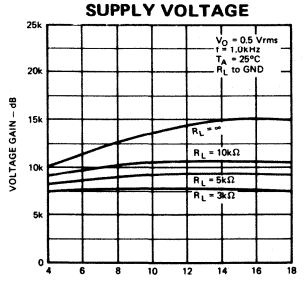
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



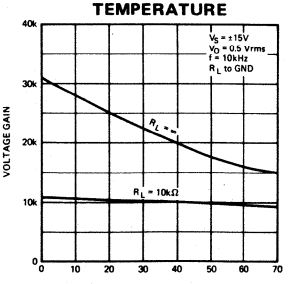
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



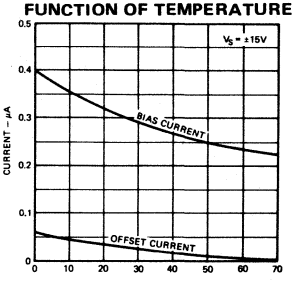
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



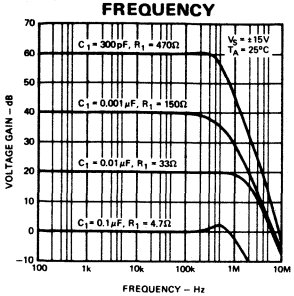
INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTION OF TEMPERATURE



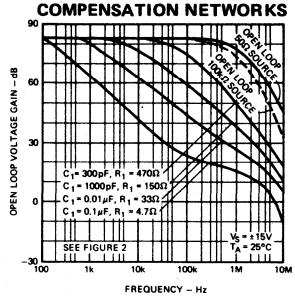
12

TYPICAL PERFORMANCE CURVES FOR μA739C

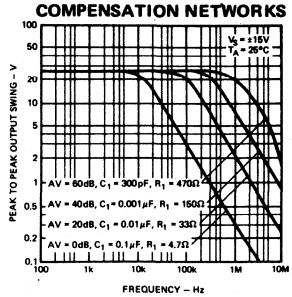
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



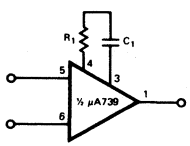
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



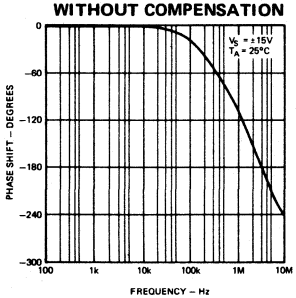
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



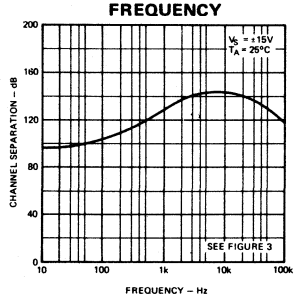
FREQUENCY COMPENSATION NETWORK



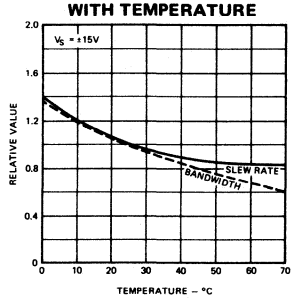
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

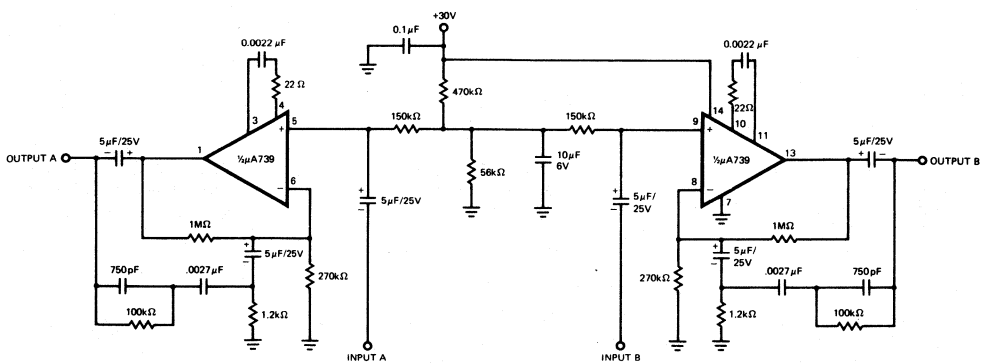


CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE



TYPICAL APPLICATION

STEREO PHONO PREAMPLIFIER – RIAA EQUALIZED



TYPICAL PERFORMANCE

Gain 40dB at 1kHz, RIAA equalized
Input overload point, 80mV rms
Noise level, 2 μV referred to input
Signal to noise ratio, 74dB below 10mV
Channel separation @ 1kHz, 80dB

μA740

FET INPUT OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA740 is a high performance monolithic FET Input Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of latch-up make the μA740 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample-and-hold circuits, transducer amplifiers, and other general feedback applications. The μA740 is short circuit protected and has the same pin configuration as the popular μA741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications.

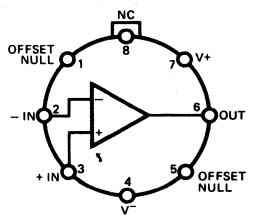
- **HIGH INPUT IMPEDANCE . . . 1,000,000 MΩ**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V+	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA740)	−55°C to +125°C
Commercial (μA740C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

CONNECTION DIAGRAM

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



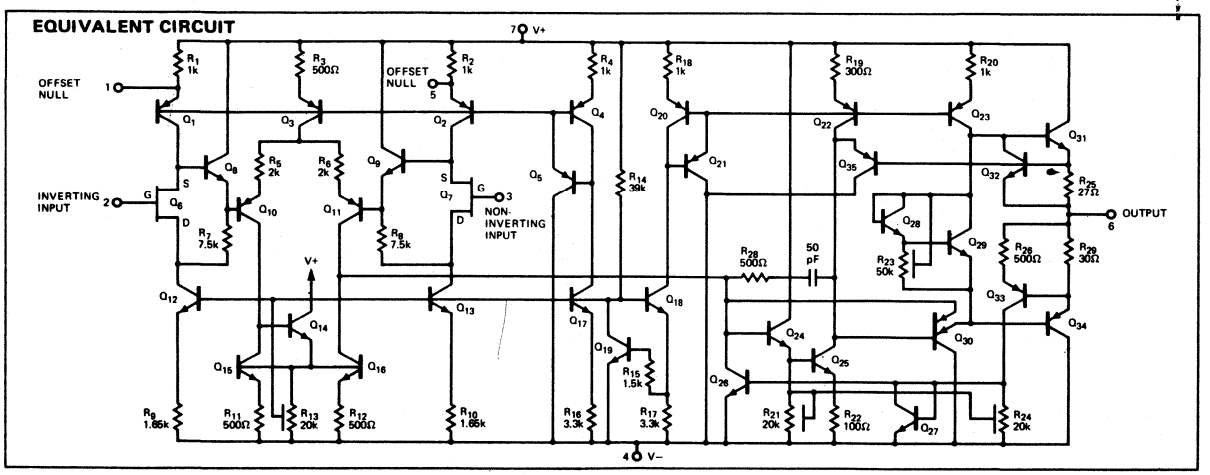
NOTE: Pin 4 Connected to Case.

ORDER INFORMATION

TYPE	PART NO.
μA740	μA740HM
μA740C	μA740HC

12

EQUIVALENT CIRCUIT



Notes on following pages.

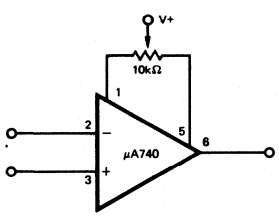
*Planar is a patented Fairchild process.

μA740

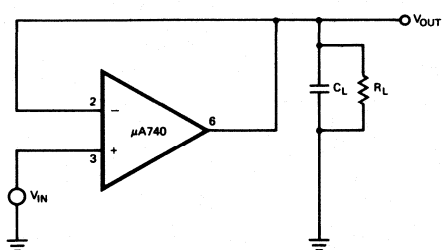
ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_C = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 100\,k\Omega$		10	20	mV
Input Offset Current [Note 4]				40	150	pA
Input Current (either input) [Note 4]				100	200	pA
Input Resistance				1,000,000		MΩ
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50,000	1,000,000		V/V
Output Resistance				75		Ω
Output Short Circuit Current				20		mA
Common Mode Rejection Ratio			64	80		dB
Supply Voltage Rejection Ratio				70	300	μV/V
Supply Current				4.2	5.2	mA
Power Consumption				126	156	mW
Slew Rate				6.0		V/μs
Unity Gain Bandwidth				3.0		MHz
Transient Response (Unity Gain)	Rise Time	$C_L \leq 100pF$, R_L = 2kΩ, V_{IN} = 100mV		110		ns
	Overshoot			10	20	%
The following specifications apply for T_C = −55°C to +85°C:						
Input Voltage Range			±10		±12	V
Large Signal Voltage Gain		$R_L \geq 2\,k\Omega$, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing		$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		V
Input Offset Voltage		$R_S \leq 100k\Omega$		15	30	mV
Input Offset Current		T_A = −55°C		30		pA
		T_A = +85°C		185		pA
Input Current (either input)		T_A = − 55°C			200	pA
		T_A = +85°C		2.5	4.0	nA

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



μA740C

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_C = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 100k\Omega$		30	110	mV
Input Offset Current (Note 4)				60	300	pA
Input Current (either input) [Note 4]				0.1	2.0	nA
Input Resistance				1,000,000		MΩ
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	20,000	1,000,000		V/V
Output Resistance				75		Ω
Output Short Circuit Current				20		mA
Supply Current				4.2	8.0	mA
Power Consumption				126	240	mW
Slew Rate				6.0		V/μs
Unity Gain Bandwidth				1.0		MHz
Transient Response (Unity Gain)	Rise Time	$C_L \leq 100pF$, R_L = 2kΩ, V_{IN} = 100mV		300		ns
	Overshoot			10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$:						
Input Voltage Range			±10	±12		V
Common Mode Rejection Ratio			55	80		dB
Supply Voltage Rejection Ratio				70	500	μV/V
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V		500,000		V/V
Output Voltage Swing		$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		V
Input Offset Voltage				30		mV
Input Offset Current				60		pA
Input Current (either input)				1.1	10	nA

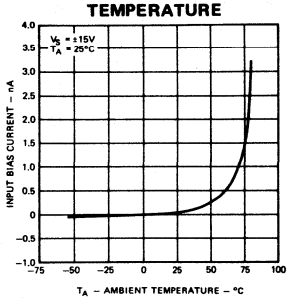
NOTES:

1. Rating applies for ambient temperature to +70°C; derate linearly at 6.3mW/°C for ambient temperatures above +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
4. Typically doubles for every 10°C increase in ambient temperature.

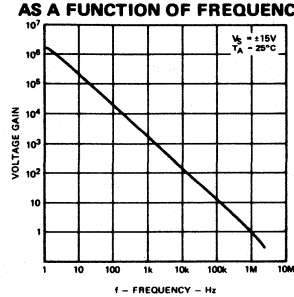
12

TYPICAL PERFORMANCE CURVES FOR μA740 AND μA740C

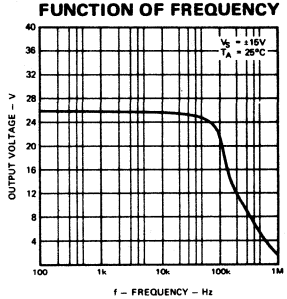
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



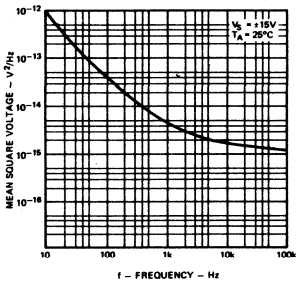
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



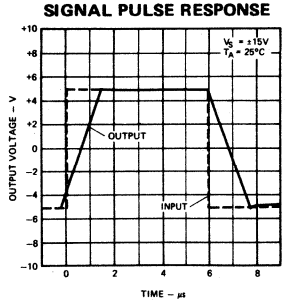
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



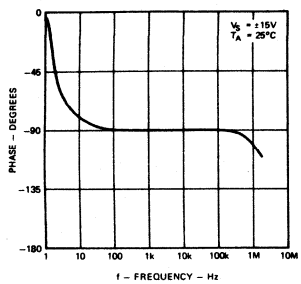
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

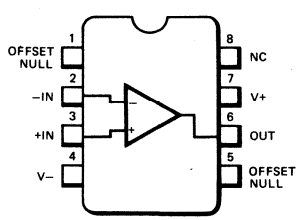
GENERAL DESCRIPTION — The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. Electrical characteristics of the μA741A and E are identical to MIL-M-38510/10101.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA741A, μA741, μA741E	±22 V
μA741C	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Molded and Hermetic DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Hermetic DIP, and Flatpak	−65°C to +150°C
Mini DIP, Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA741A, μA741)	−55°C to +125°C
Commercial (μA741E, μA741C)	0°C to +70°C
Lead Temperature (Soldering)	
Metal Can, Hermetic DIPs, and Flatpak (60 s)	300°C
Molded DIPs (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

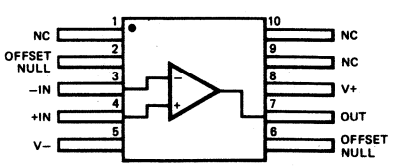
8-LEAD MINIDIP
(TOP VIEW)
PACKAGE OUTLINES 6T 9T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
μA741C	μA741TC
μA741C	μA741RC

10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F

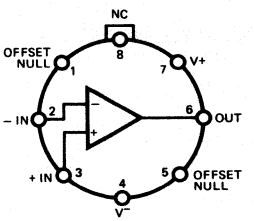


ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AFM
μA741	μA741FM

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B

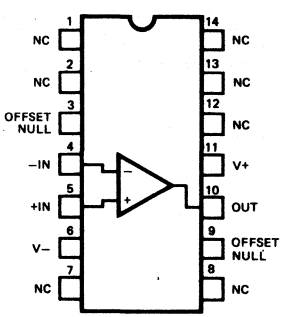


Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741AHM
μA741	μA741HM
μA741E	μA741EHC
μA741C	μA741HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
μA741A	μA741ADM
μA741	μA741DM
μA741E	μA741EDC
μA741C	μA741DC
μA741C	μA741PC

12

Notes on following pages.

*Planar is a patented Fairchild process.

μA741A

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\Omega$			0.8	3.0	mV
Average Input Offset Voltage Drift						15	μV/°C
Input Offset Current					3.0	30	nA
Average Input Offset Current Drift						0.5	nA/°C
Input Bias Current					30	80	nA
Power Supply Rejection Ratio		V_S = +10, –20; V_S = +20, –10V, R_S = 50Ω			15	50	μV/V
Output Short Circuit Current				10	25	35	mA
Power Dissipation		V_S = ±20V			80	150	mW
Input Impedance		V_S = ±20V		1.0	6.0		MΩ
Large Signal Voltage Gain		V_S = ±20V, R_L = 2kΩ, V_{OUT} = ±15V		50			V/mV
Transient Response	Rise Time				0.25	0.8	μs
(Unity Gain)	Overshoot				6.0	20	%
Bandwidth (Note 4)				.437	1.5		MHz
Slew Rate (Unity Gain)		V_{IN} = ±10V		0.3	0.7		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$							
Input Offset Voltage						4.0	mV
Input Offset Current						70	nA
Input Bias Current						210	nA
Common Mode Rejection Ratio		V_S = ±20V, V_{IN} = ±15V, R_S = 50Ω		80	95		dB
Adjustment For Input Offset Voltage		V_S = ±20V		10			mV
Output Short Circuit Current				10		40	mA
Power Dissipation		V_S = ±20V	–55°C			165	mW
			+125°C			135	mW
Input Impedance		V_S = ±20V		0.5			MΩ
Output Voltage Swing		V_S = ±20V,	R_L = 10kΩ	±16			V
			R_L = 2kΩ	±15			V
Large Signal Voltage Gain		V_S = ±20V, R_L = 2kΩ, V_{OUT} = ±15V		32			V/mV
		V_S = ±5V, R_L = 2kΩ, V_{OUT} = ±2 V		10			V/mV

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. Calculated value from: $BW(MHz) = \frac{0.35}{\text{Rise Time } (\mu s)}$

μA741

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	50,000	200,000		
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2\ k\Omega$		0.5		V/μs

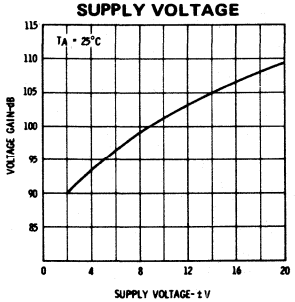
The following specifications apply for $-55°C \leq T_A \leq +125°C$:

Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current	T_A = +125°C		7.0	200	nA
	T_A = −55°C		85	500	nA
Input Bias Current	T_A = +125°C		0.03	0.5	μA
	T_A = −55°C		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	25,000			
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		V
Supply Current	T_A = +125°C		1.5	2.5	mA
	T_A = −55°C		2.0	3.3	mA
Power Consumption	T_A = +125°C		45	75	mW
	T_A = −55°C		60	100	mW

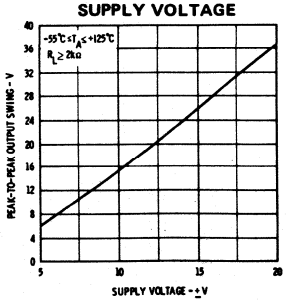
12

TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

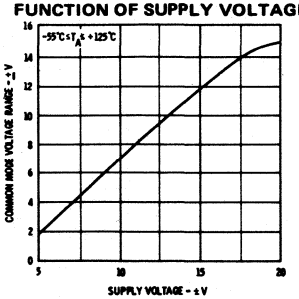
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

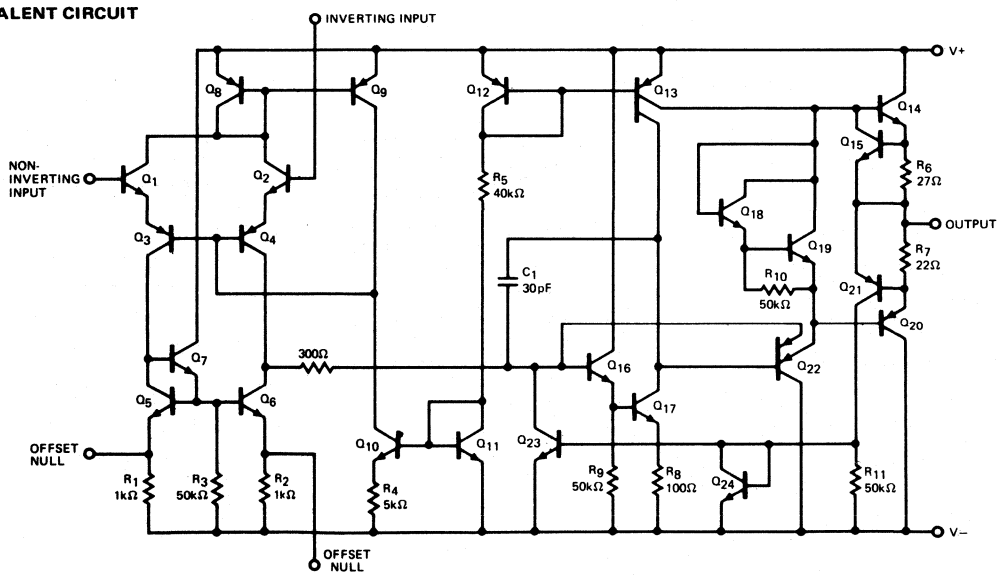


μA741E

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\Omega$			0.8	3.0	mV
Average Input Offset Voltage Drift						15	μV/°C
Input Offset Current					3.0	30	nA
Average Input Offset Current Drift						0.5	nA/°C
Input Bias Current					30	80	nA
Power Supply Rejection Ratio		V_S = +10, –20; V_S = +20, –10V, R_S = 50Ω			15	50	μV/V
Output Short Circuit Current				10	25	35	mA
Power Dissipation		V_S = ±20V			80	150	mW
Input Impedance		V_S = ±20V		1.0	6.0		MΩ
Large Signal Voltage Gain		V_S = ±20V, R_L = 2kΩ, V_{OUT} = ±15V		50			V/mV
Transient Response	Rise Time				0.25	0.8	μs
(Unity Gain)	Overshoot				6.0	20	%
Bandwidth (Note 4)				.437	1.5		MHz
Slew Rate (Unity Gain)		V_{IN} = ±10V		0.3	0.7		V/μs
The following specifications apply for 0°C ≤ T_A ≤ 70°C							
Input Offset Voltage						4.0	mV
Input Offset Current						70	nA
Input Bias Current						210	nA
Common Mode Rejection Ratio		V_S = ±20V, V_{IN} = ±15V, R_S = 50Ω		80	95		dB
Adjustment For Input Offset Voltage		V_S = ±20V		10			mV
Output Short Circuit Current				10		40	mA
Power Dissipation		V_S = ±20V				150	mW
Input Impedance		V_S = ±20V		0.5			MΩ
Output Voltage Swing		V_S = ±20V,	R_L = 10kΩ	±16			V
			R_L = 2kΩ	±15			V
Large Signal Voltage Gain		V_S = ±20V, R_L = 2kΩ, V_{OUT} = ±15V		32			V/mV
		V_S = ±5V, R_L = 2kΩ, V_{OUT} = ±2 V		10			V/mV

EQUIVALENT CIRCUIT



μA741C

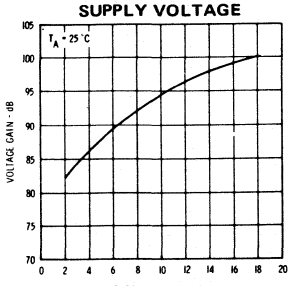
ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10\ k\Omega$		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	20,000	200,000		
Output Voltage Swing		$R_L \geq 10\ k\Omega$	±12	±14		V
		$R_L \geq 2\ k\Omega$	±10	±13		V
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2\ k\Omega$		0.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C:						
Input Offset Voltage					7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	15,000			
Output Voltage Swing		$R_L \geq 2\ k\Omega$	±10	±13		V

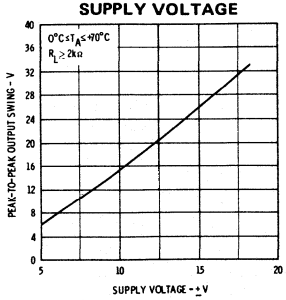
12

TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

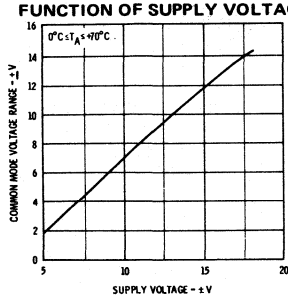
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

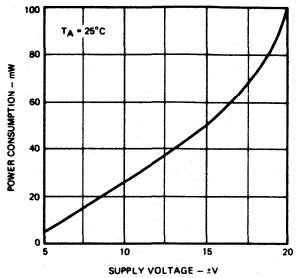


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

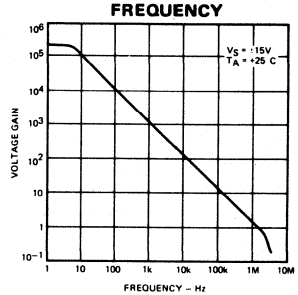


TYPICAL PERFORMANCE CURVES FOR μA741A, μA741, μA741E AND μA741C

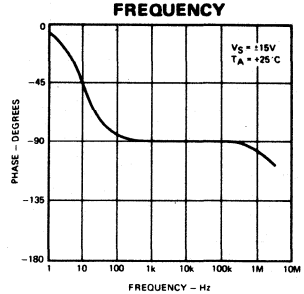
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



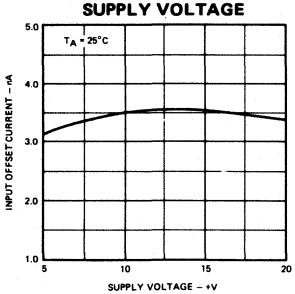
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



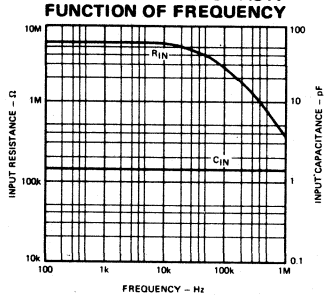
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



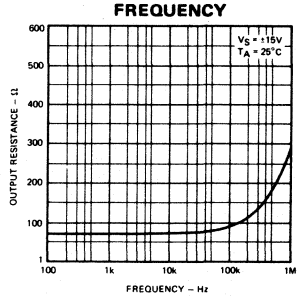
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



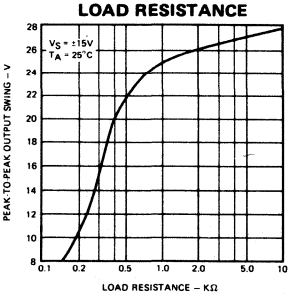
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



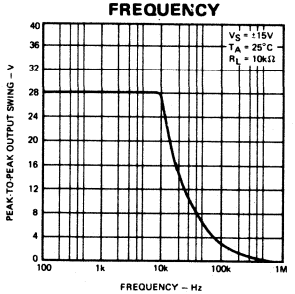
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



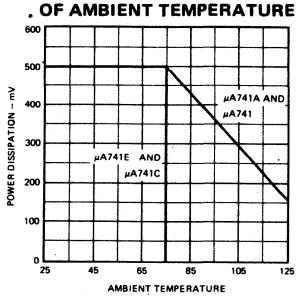
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



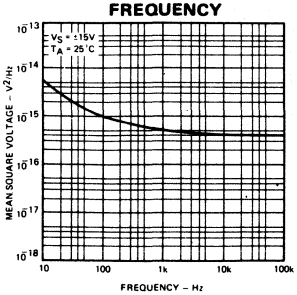
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



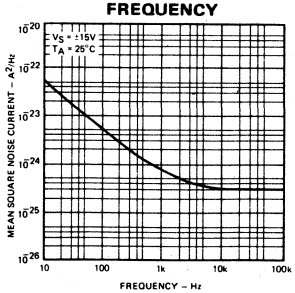
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



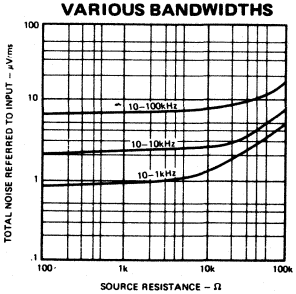
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

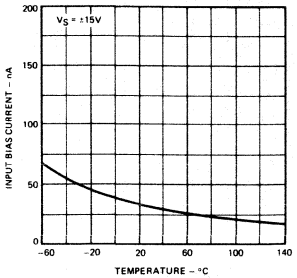


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

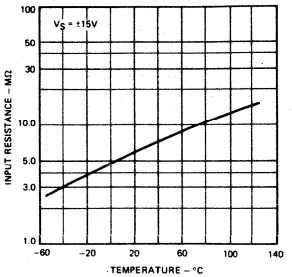


TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

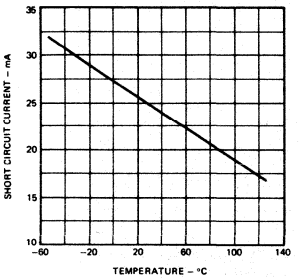
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



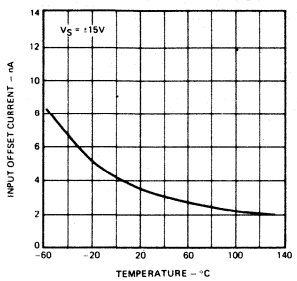
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



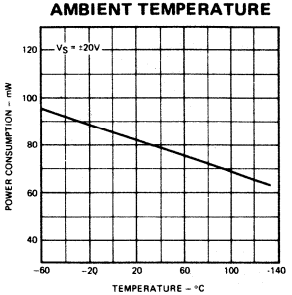
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



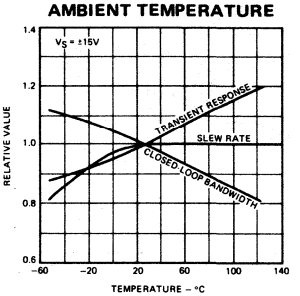
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

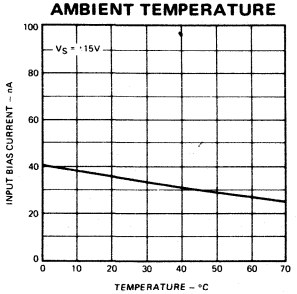


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

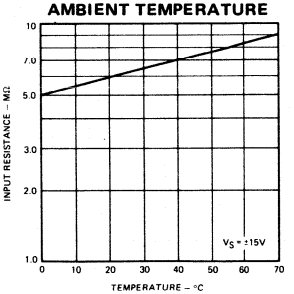


TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

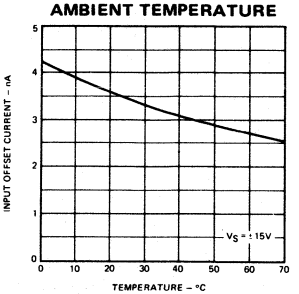
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



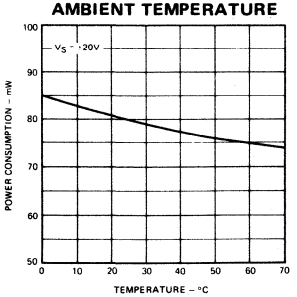
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



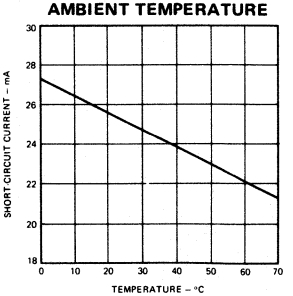
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



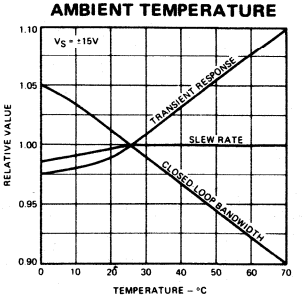
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

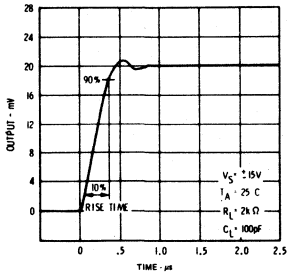


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

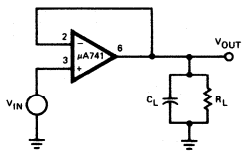


12

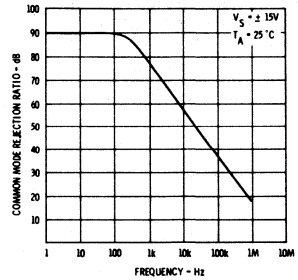
TRANSIENT RESPONSE



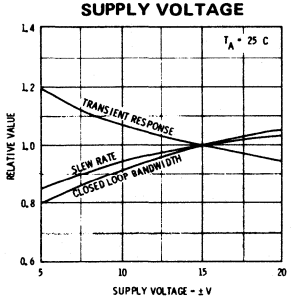
TRANSIENT RESPONSE TEST CIRCUIT



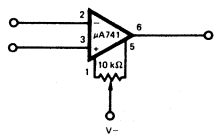
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



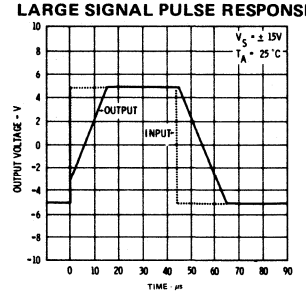
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

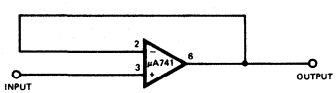


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



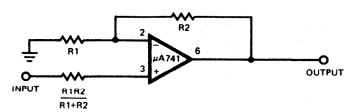
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



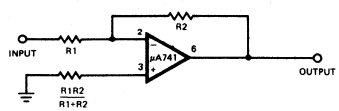
R_{IN} = 400 MΩ
C_{IN} = 1 pF
R_{OUT} << 1 Ω
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



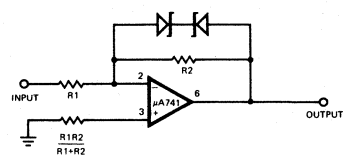
GAIN	R1	R2	B W	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R1	R2	B W	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER

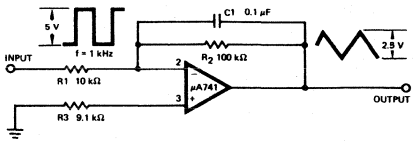


$$\frac{E_{OUT}}{E_{IN}} = \frac{R2}{R1} \text{ if } |E_{OUT}| \leq V_Z + 0.7\ V$$

where V_Z = Zener breakdown voltage

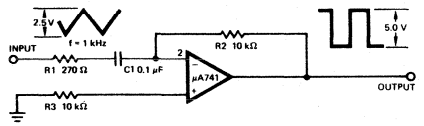
TYPICAL APPLICATIONS (Cont'd)

SIMPLE INTEGRATOR



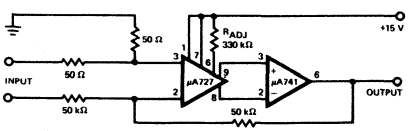
$$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}dt$$

SIMPLE DIFFERENTIATOR



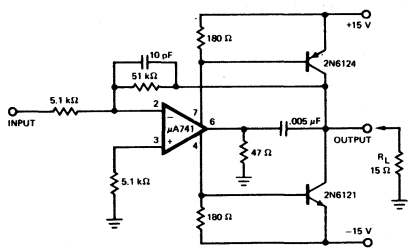
$$E_{OUT} = -R2C1\frac{dE_{IN}}{dt}$$

LOW DRIFT LOW NOISE AMPLIFIER

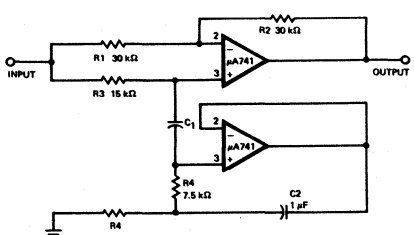


Voltage Gain = 10^3
Input Offset Voltage Drift = 0.6 μV/°C
Input Offset Current Drift = 2.0 pA/°C

HIGH SLEW RATE POWER AMPLIFIER



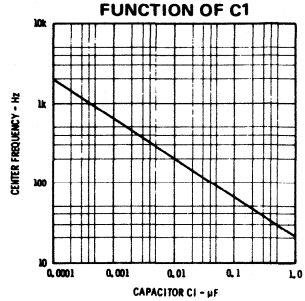
NOTCH FILTER USING THE μA741 AS A GYRATOR



Trim R3 such that

$$\frac{R1}{R2} = \frac{R3}{2\ R4}$$

NOTCH FREQUENCY AS A FUNCTION OF C1



12

μA747

DUAL FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

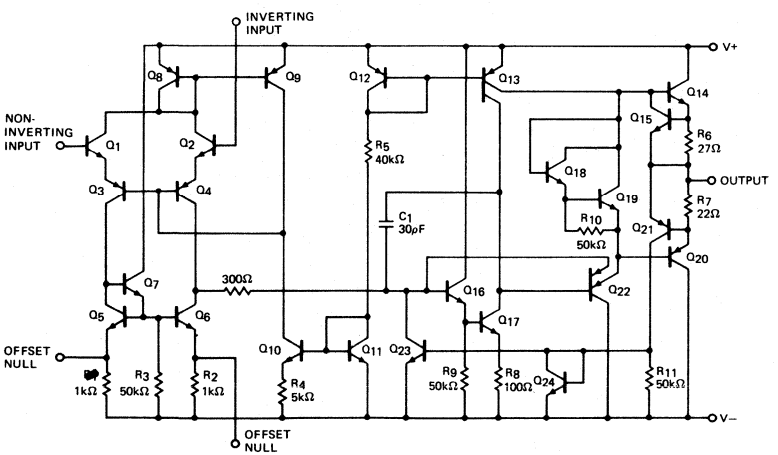
GENERAL DESCRIPTION — The μA747 is a pair of high performance monolithic Operational Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch-up make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet. Electrical characteristics are identical to MIL-M-38510/10102.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

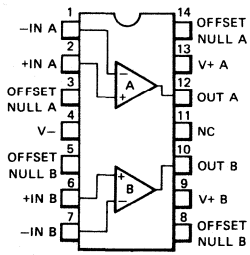
Supply Voltage	
Military (μA747A, μA747, μA747E)	±22 V
Commercial (μA747C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage betweeen Offset Null and V−	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA747A, μA747)	−55° C to +125°C
Commercial (μA747E, μA747C)	0°C to 70°C
Lead Temperature (Soldering 60s)	300°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT (1/2 μA747)



Notes on following pages.

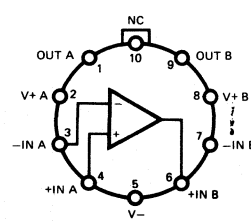
CONNECTION DIAGRAMS
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 7A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA747A	μA747ADM
μA747	μA747DM
μA747E	μA747EDC
μA747C	μA747DC
μA747C	μA747PC
μA747−I	μA747−IDM
μA747−IC	μA747−IDC

10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F



ORDER INFORMATION

TYPE	PART NO.
μA747A	μA747AHM
μA747	μA747HM
μA747E	μA747EHC
μA747C	μA747HC
μA747−I	μA747−IHM
μA747−IC	μA747−IHC

NOTE:
V+A is internally connected to V+B for μA747A, μA747, μA747E, and μA747C. They are not internally connected for μA747-I and μA747-IC.

*Planar is a patented Fairchild process.

μA747A

ELECTRICAL CHARACTERISTICS $\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$ unless otherwise specified)

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift					15	μV/°C
Input Offset Current				3.0	30	nA
Average Input Offset Current Drift		$T_A = 25°C$ to $+125°C$ $T_A = -55°C$ to $+25°C$			0.2 0.5	nA/°C nA/°C
Input Bias Current				30	80	nA
Power Supply Rejection Ratio		$V_S = +10, -20$; $V_S = +20\ V, -10\ V$ 0.2 $R_S = 50\ \Omega$		15	50	μV/V
Common Mode Rejection Ratio		$V_S = \pm 20\ V$, $V_{IN} = \pm 15\ V$ $R_S = 50\ \Omega$	80	95		dB
Adjustment for Input Offset Voltage		$V_S = \pm 20\ V$	10			mV
Output Short Circuit Current			10	25	35	mA
Power Dissipation		$V_S = \pm 20\ V$ per Channel		80	150	mW
Input Impedance		$V_S = \pm 20\ V$	1.0	6		MΩ
Large Signal Voltage Gain		$V_S = \pm 20\ V$, $R_L = 2\ k\Omega$ $V_{OUT} = \pm 15\ V$	50			V/mV
Transient Response (Unity Gain)	Rise Time			0.25	0.8	μs
	Overshoot			6.0	20	%
Bandwidth (Note 4)			0.437	1.5		MHz
Slew Rate (Unity Gain)		$V_{IN} = \pm 10\ V$	0.3	0.7		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$						
Input Offset Voltage					4.0	mV
Input Offset Current					70	nA
Input Bias Current					210	nA
Output Short Circuit Current			10		40	mA
Power Dissipation		$V_S = \pm 20\ V$ $-55°C$			165	mW
		$V_S = \pm 20\ V$ $+125°C$			135	mW
Input Impedance		$V_S = \pm 20\ V$	0.5			MΩ
Output Voltage Swing		$V_S = \pm 20\ V$, $R_L = 10\ k\Omega$	±16			V
		$R_L = 2\ k\Omega$	±15			V
Large Signal Voltage Gain		$V_S = \pm 20\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 15\ V$	32			V/mV
		$V_S = \pm 5\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 2\ V$	10			V/mV
Channel Separation		$V_S = \pm 20\ V$	100			dB

NOTES:
1. Rating applies to ambient temperatures uo to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. Calculated value from: $BW\ (MHz) = \frac{0.35}{\text{RISE TIME } (\mu s)}$

12

μA747

ELECTRICAL CHARACTERISTICS – Each Amplifier (V_S = ±15 V, T_A = 25°C unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	50,000	200,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2$ kΩ		0.5		V/μs
Channel Separation				120		dB

The following specifications apply for −55°C ≤ T_A ≤ +125°C.

Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	T_A = +125°C		7.0	200	nA
	T_A = −55°C		85	500	nA
Input Bias Current	T_A = +125°C		0.03	0.5	μA
	T_A = −55°C		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	T_A = +125°C		1.5	2.5	mA
	T_A = −55°C		2.0	3.3	mA
Power Consumption	T_A = +125°C		45	75	mW
	T_A = −55°C		60	100	mW

μA747C

ELECTRICAL CHARACTERISTICS — Each Amplifier (V_S = ±15 V, T_A = 25°C unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000	200,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2$ kΩ		0.5		V/μs
Channel Separation				120		dB

The following specifications apply for 0°C ≤ T_A ≤ +70°C.

Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			0.03	0.8	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current			2.0	3.3	mA
Power Consumption			60	100	mW

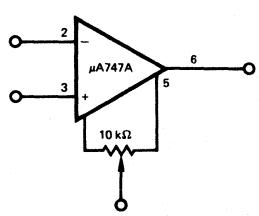
12

μA747E

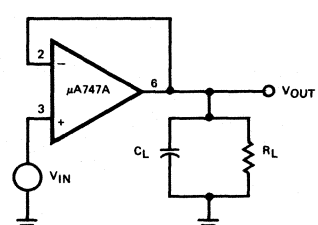
ELECTRICAL CHARACTERISTICS ($\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$ unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift					15	μV/°C
Input Offset Current				3	30	nA
Average Input Offset Current Drift		$T_A = 25°C$ to 70°C $T_A = 0°C$ to 25°C			0.2 0.5	nA/°C nA/°C
Input Bias Current				30	80	nA
Power Supply Rejection Ratio		$V_S = +10, -20$; $V_S = +20, -10$ V $R_S = 50\ \Omega$		15	50	μV/V
Common Mode Rejection Ratio		$V_S = \pm 20$ V, $V_{IN} = \pm 15$ V $R_S = 50\ \Omega$	80	95		dB
Adjustment for Input Offset Voltage		$V_S = \pm 20$ V	10			mV
Output Short Circuit Current			10	25	35	mA
Power Dissipation		$V_S = \pm 20$ V		80	150	mW
Input Impedance		$V_S = \pm 20$ V	1.0	6		MΩ
Large Signal Voltage Gain		$V_S = \pm 20$ V, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 15$ V	50			V/mV
Transient Response (Unity Gain)	Rise Time			0.25	0.8	μs
	Overshoot			6	20	%
Bandwidth (Note 4)			0.437	1.5		MHz
Slew Rate (Unity Gain)		$V_{IN} = \pm 10$ V	0.3	0.7		V/μs
The following specifications apply for $0°C \leq T_A \leq 70°C$						
Input Offset Voltage					4.0	mV
Input Offset Current					70	nA
Input Bias Current					210	nA
Output Short Circuit Current			10		40	mA
Power Dissipation		$V_S = \pm 20$ V			165	mW
Input Impedance		$V_S = \pm 20$ V	0.5			MΩ
Output Voltage Swing		$V_S = \pm 20$ V, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±16 ±15			V V
Large Signal Voltage Gain		$V_S = \pm 20$ V, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 15$ V	32			V/mV
		$V_S = \pm 5$ V, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 2$ V	10			V/mV
Channel Separation		$V_S = \pm 20$ V	100			dB

VOLTAGE OFFSET NULL CIRCUIT

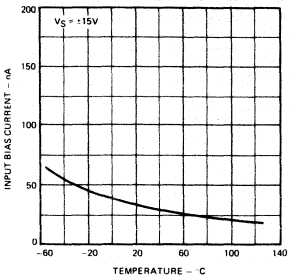


TRANSIENT RESPONSE TEST CIRCUIT

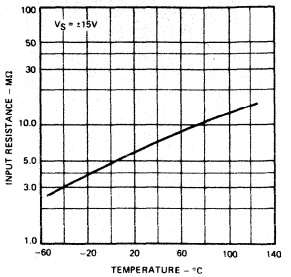


TYPICAL PERFORMANCE CURVES FOR μA747A AND μA747

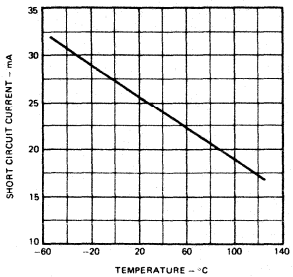
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



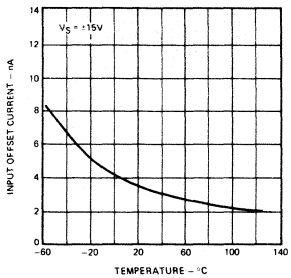
INPUT RESIGTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



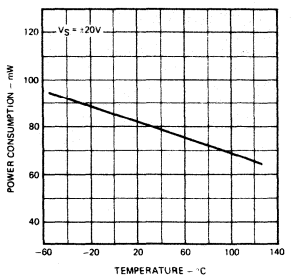
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



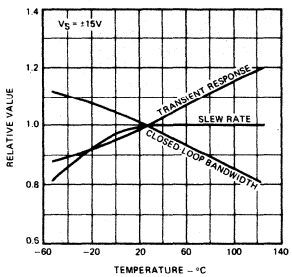
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

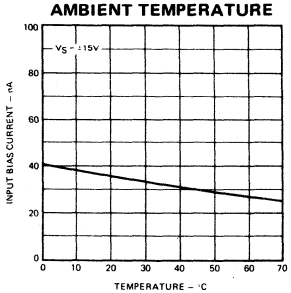


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

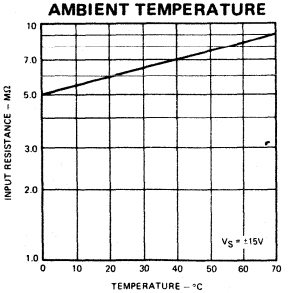


TYPICAL PERFORMANCE CURVES FOR μA747E AND μA747C

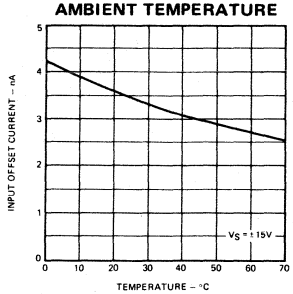
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



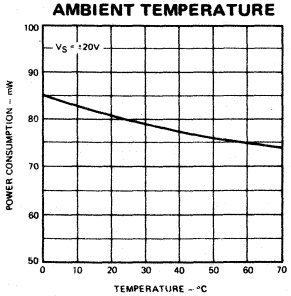
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



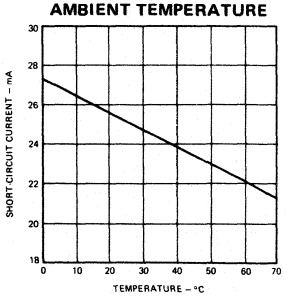
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



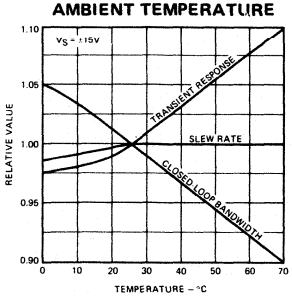
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



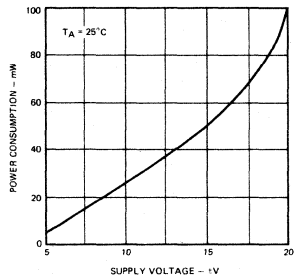
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



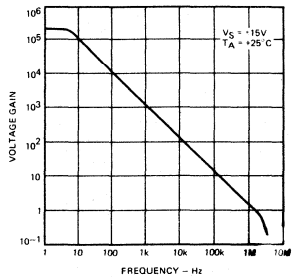
12

TYPICAL PERFORMANCE CURVES FOR μA747A, μA747C, μA747 AND μA747E

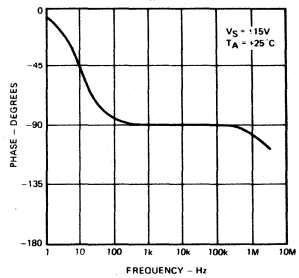
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



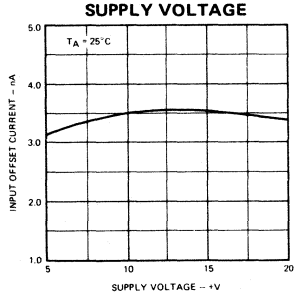
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



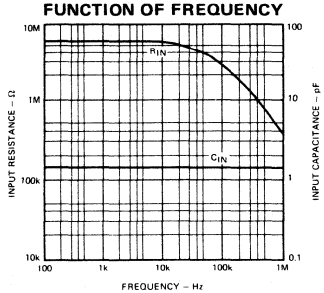
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



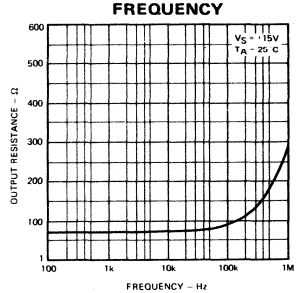
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



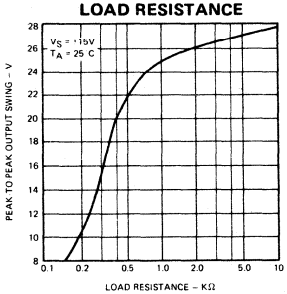
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



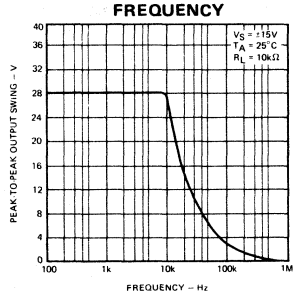
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



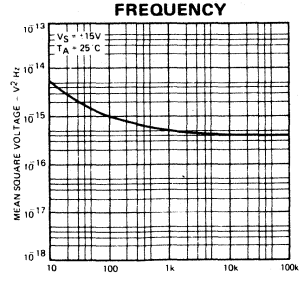
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



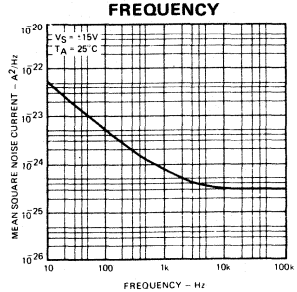
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



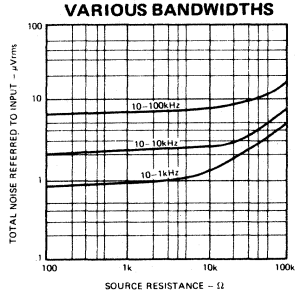
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

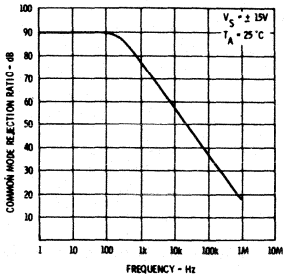


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

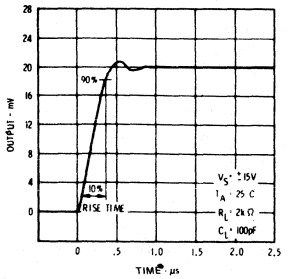


TYPICAL PERFORMANCE CURVES (Each Anplifier) FOR μA747 AND μA747C

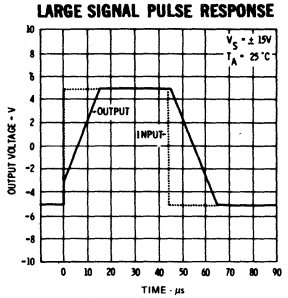
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



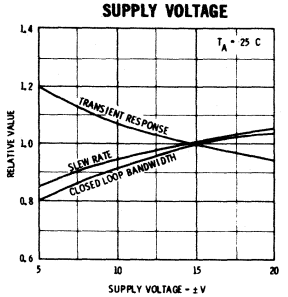
TRANSIENT RESPONSE



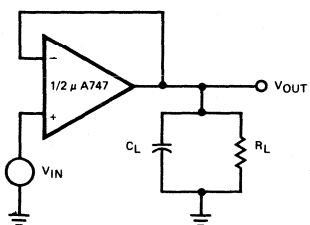
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



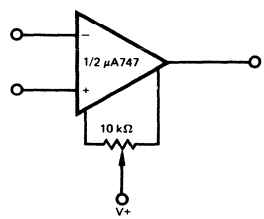
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



TRANSIENT RESPONSE TEST CIRCUIT



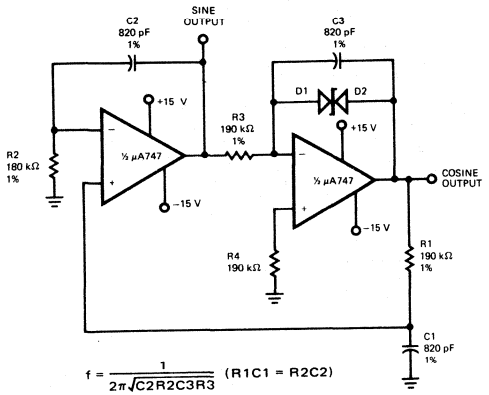
VOLTAGE OFFSET NULL CIRCUIT



12

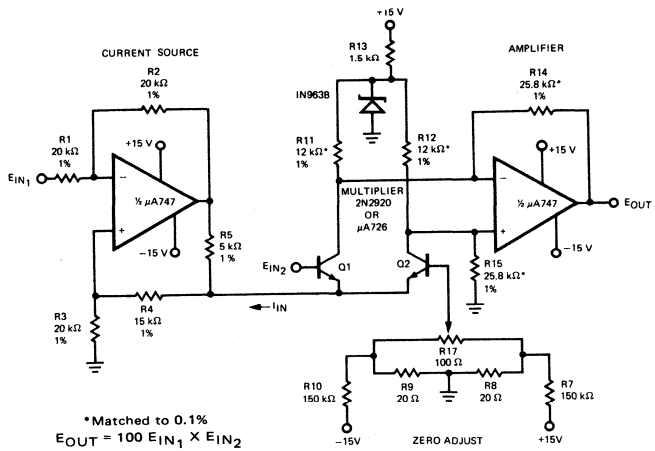
TYPICAL APPLICATIONS

QUADRATURE OSCILLATOR



$$f = \frac{1}{2\pi\sqrt{C2R2C3R3}} \quad (R1C1 = R2C2)$$

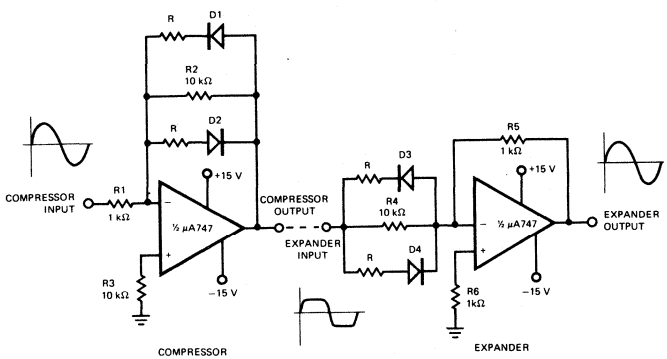
ANALOG MULTIPLIER



*Matched to 0.1%

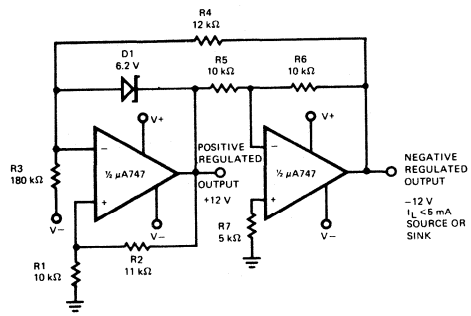
$E_{OUT} = 100\ E_{IN_1} \times E_{IN_2}$

COMPRESSOR/EXPANDER AMPLIFIERS



MUXIMUM COMPRESSION EXPANSION TATIO = R1/R (10 kΩ >R ⩾0)
NOTE: DIODES D1 THROUGH D4 ARE MATCHED FD666 OR EQUIVALENT

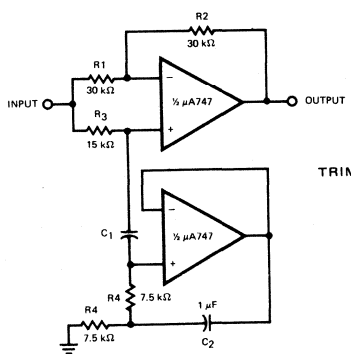
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



$$\text{POSITIVE OUTPUT} = V_{D1} \times \frac{R1 + R2}{R2}$$

$$\text{NEGATIVE OUTPUT} = -\text{POSITIVE OUTPUT} \times \frac{R6}{R5}$$

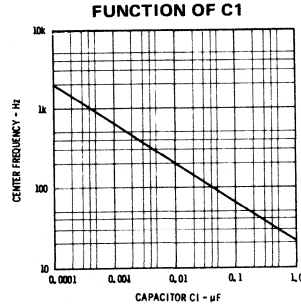
NOTCH FILTER USING THE μA747 AS A GYRATOR



TRIM R3 SUCH THAT

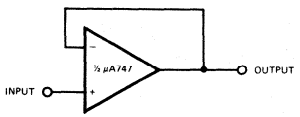
$$\frac{R1}{R2} = \frac{R3}{2\ R4}$$

NOTCH FREQUENCY AS A FUNCTION OF C1



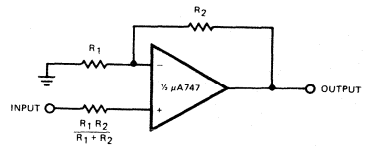
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



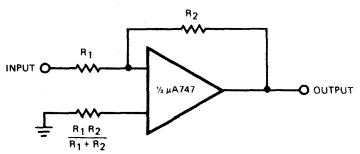
R_{IN} = 400 MΩ
C_{IN} = 1 pF
$R_{OUT} << 1\ \Omega$
B W = 1 MHz

NON-INVERTING AMPLIFIER



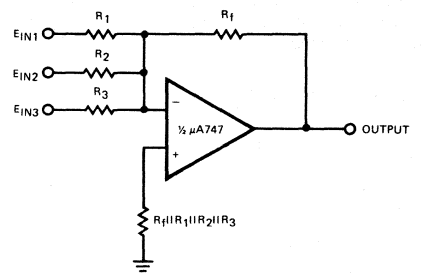
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B W	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

WEIGHTED AVERAGING AMPLIFIER



$$-E_{OUT} = E_{IN1}\left(\frac{R_f}{R_1}\right) + E_{IN2}\left(\frac{R_f}{R_2}\right) + E_{IN3}\left(\frac{R_f}{R_3}\right)$$

12

μA748

OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA748 is a High Performance Monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a high wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of latch-up make the μA748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748 is short-circuit protected and has the same pin configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For superior performance, see μA777 data sheet.

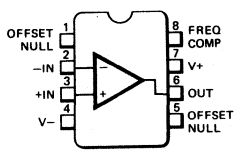
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA748)	−55°C to +125°C
Commercial (μA748C)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, Flatpak, and Hermetic DIPs	300°C
Molded Mini DIP	260°C
Output Short Circuit Duration (Note 3)	Indefinite

CONNECTION DIAGRAMS

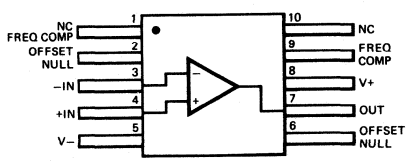
8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA748C	μA748TC

10-LEAD FLATPAK‡
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



‡Available on special request

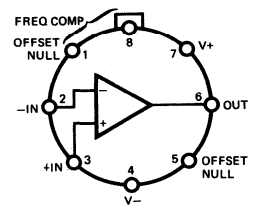
ORDER INFORMATION

TYPE	PART NO.
μA748	μA748FM
μA748A	μA748AFM

Notes and equivalent circuit on following pages.

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

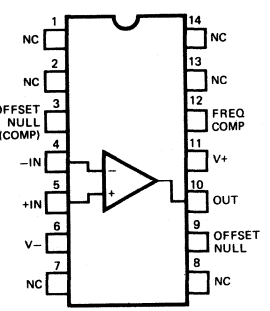


NOTE: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA748	μA748HM
μA748A	μA748AHM
μA748C	μA748HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA748	μA748DM
μA748A	μA748ADM
μA748C	μA748DC

*Planar is a patented Fairchild process.

μA748A

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\ k\Omega$		0.5	2.0	mV
Input Offset Current				2.0	10	nA
Input Bias Current				20	75	nA
Input Resistance			2.0	10.0		MΩ
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				±25		mV
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	50,000	250,000		V/V
Output Resistance				100		Ω
Output Short Circuit Current				±25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2k\Omega$		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2\ k\Omega$, C_C = 3.5 pF		5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:						
Input Offset Voltage		$R_S \leq 50\ k\Omega$		0.5	3.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50\ k\Omega$		2.5	15	μV/°C
Input Offset Current					25	nA
Average Input Offset Current Drift		$25°C \leq T_A \leq +125°C$		2.5	30	pA/°C
		$-55°C \leq T_A \leq 25°C$		6.5	150	pA/°C
Input Bias Current					100	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 50\ k\Omega$	80	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50\ k\Omega$		13	100	μV/V
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing		$R_L \geq 10\ k\Omega$	±12	±14		V
		$R_L \geq 2\ k\Omega$	±10	±13		V
Supply Current		T_A = +125°C		1.5	2.5	mA
		T_A = -55°C		2.0	3.3	mA
Power Consumption		T_A = +125°C		40	75	mW
		T_A = -55°C		60	100	mW

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for the DIP 5.6 mW/°C for the mini DIP and 7.1 mW/°C for the flatpak.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

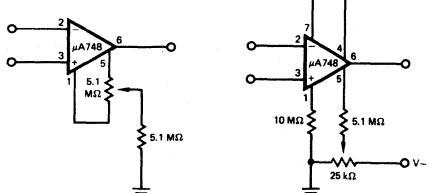
12

μA748

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

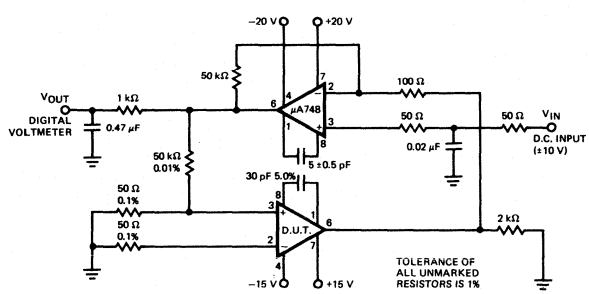
PARAMETERS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				2.0		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	50,000	150,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2$ kΩ, C_C = 3.5 pF		5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:						
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current		T_A = +125°C		10	200	nA
		T_A = −55°C		50	500	nA
Input Bias Current		T_A = +125°C		0.03	0.5	μA
		T_A = −55°C		0.3	1.5	μA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		V
Supply Current		T_A = +125°C		1.5	2.5	mA
		T_A = −55°C		2.0	3.3	mA
Power Consumption		T_A = +125°C		45	75	mW
		T_A = −55°C		60	100	mW

VOLTAGE OFFSET NULL CIRCUIT



SUGGESTED ALTERNATE

GAIN TEST CIRCUIT



$$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}} = \frac{10 \times 10^3}{V_{OUT}} \text{ FOR } V_{IN} \text{ SPECIFIED}$$

μA748C

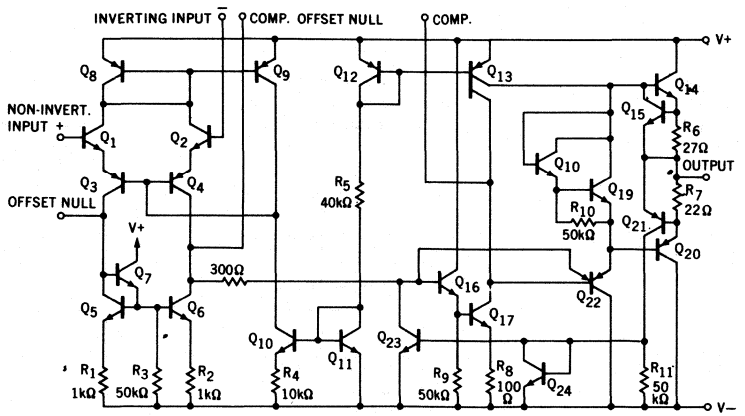
ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		R_S ≤10 kΩ		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				2.0		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		R_L ≥2 kΩ, V_{OUT} = ±10 V	20,000	150,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, C_L ≤100 pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		R_L ≥2 kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, C_L ≤100 pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		R_L ≥2 kΩ, C_C = 3.5 pF		5.5		V/μs

The following specifications apply for 0°C ≤ T_A ≤ +70°C:

Input Offset Voltage	R_S ≤ 10 kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	R_S ≤10 kΩ	70	90		dB
Supply Voltage Rejection Ratio	R_S ≤10 kΩ		30	150	μV/V
Large Signal Voltage Gain	* R_L ≥2 kΩ, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing	R_L ≥10 kΩ	±12	±14		V
	R_L ≥2 kΩ	±10	±13		V
Power Consumption			60	100	mW

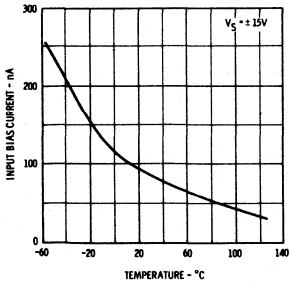
EQUIVALENT CIRCUIT



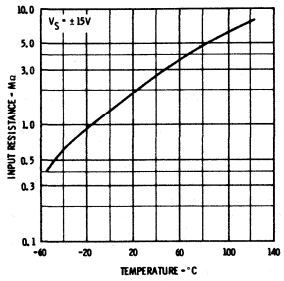
12

TYPICAL PERFORMANCE CURVES FOR μA748

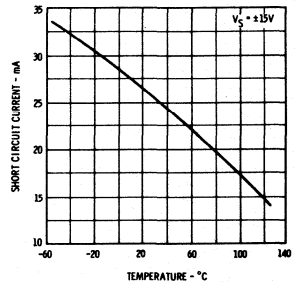
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



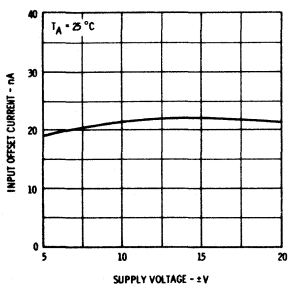
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



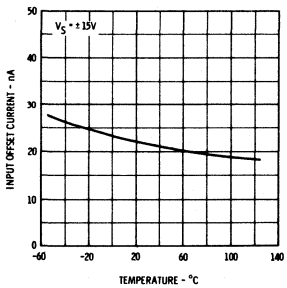
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



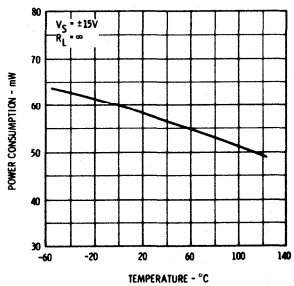
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

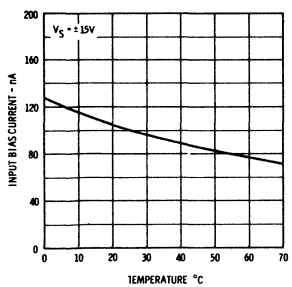


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

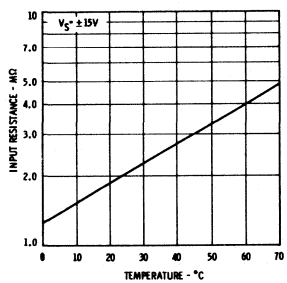


TYPICAL PERFORMANCE CURVES FOR μA748C

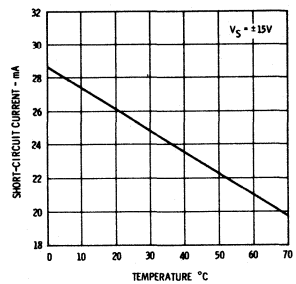
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



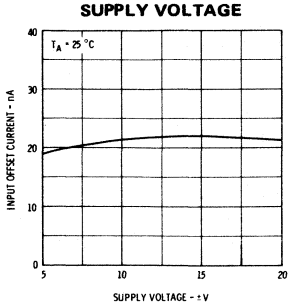
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



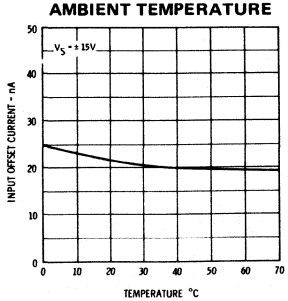
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



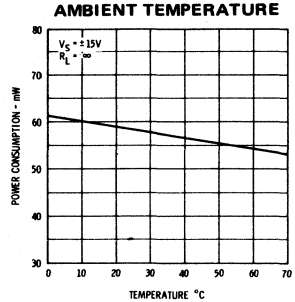
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

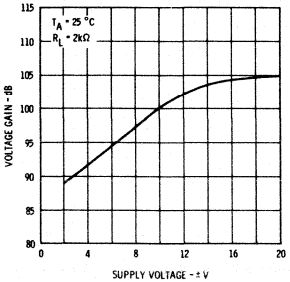


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

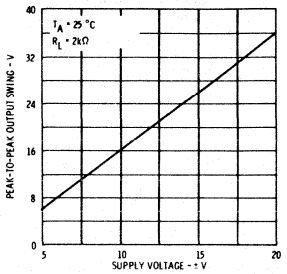


TYPICAL PERFORMANCE CURVES FOR μA748 AND μA748C

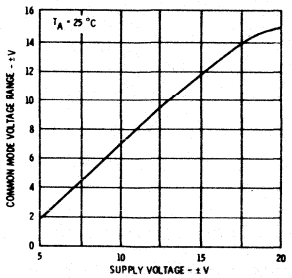
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



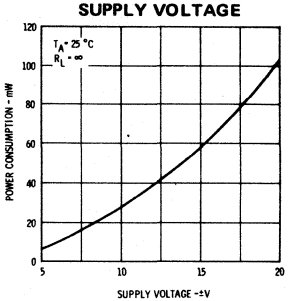
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



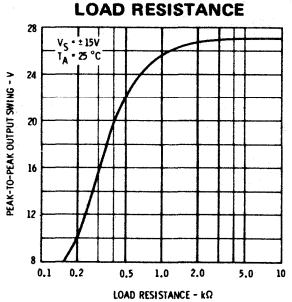
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



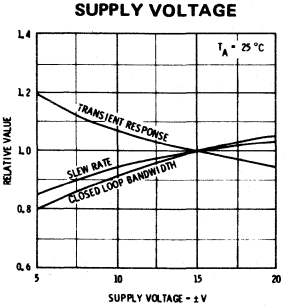
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



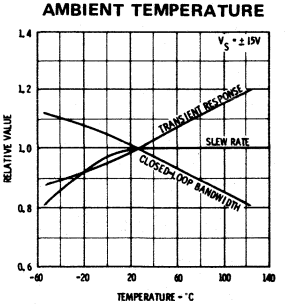
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



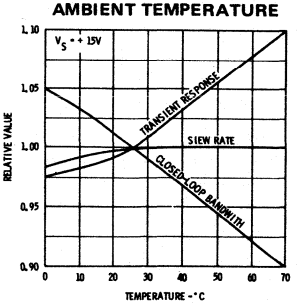
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



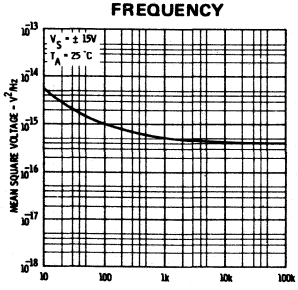
μA748 FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



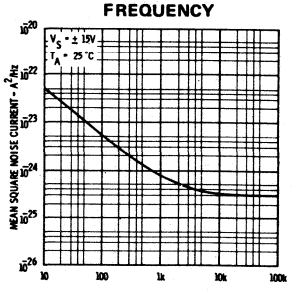
748C FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



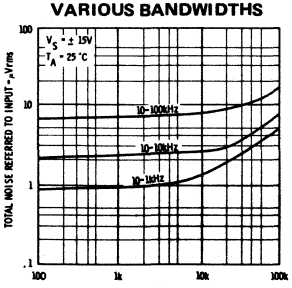
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



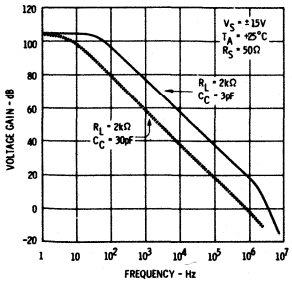
BROAD BAND NOISE FOR VARIOUS BANDWIDTHS



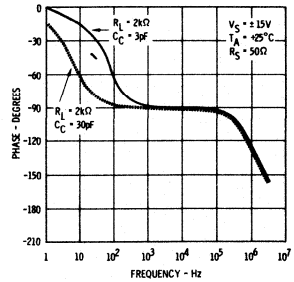
12

TYPICAL PERFORMANCE CURVES FOR μA748 AND μA748C

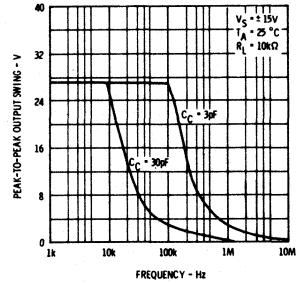
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



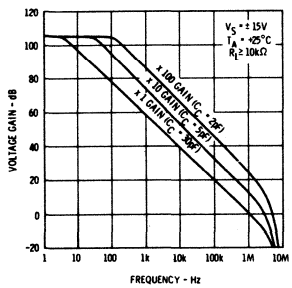
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



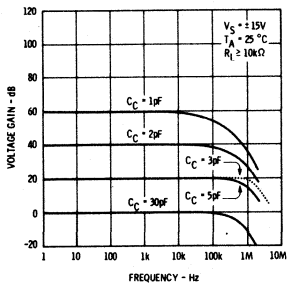
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



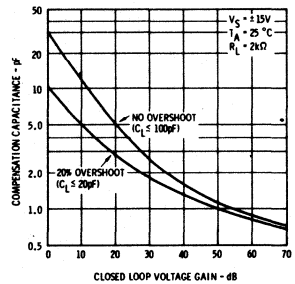
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



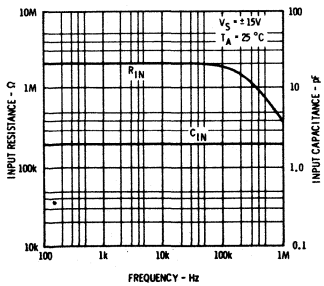
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



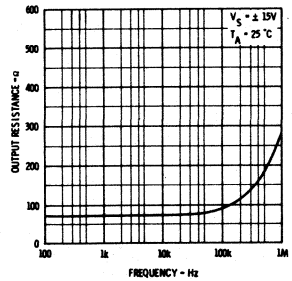
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



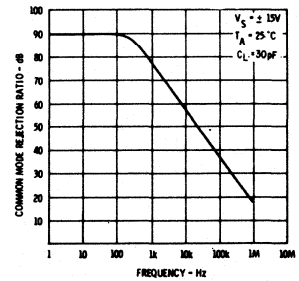
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



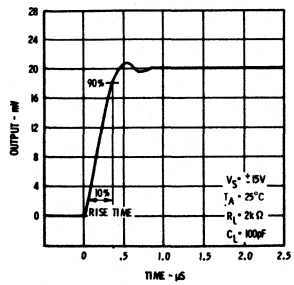
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



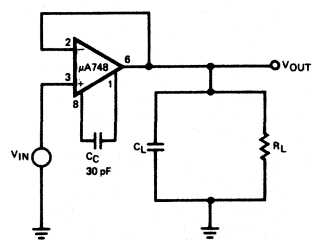
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



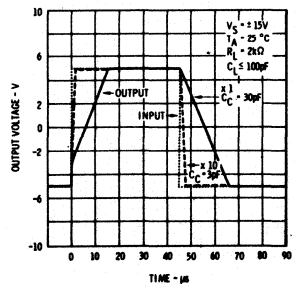
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

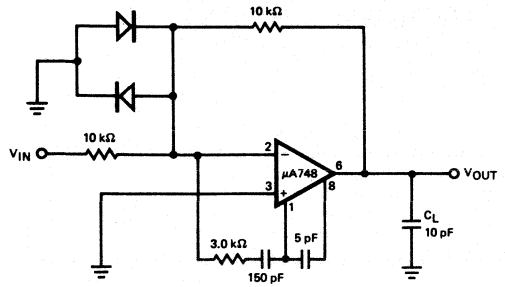


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

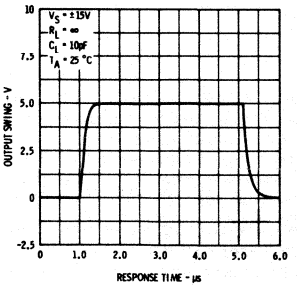


TYPICAL PERFORMANCE CURVES FOR μA748 AND μA748C

FEED FORWARD COMPENSATION

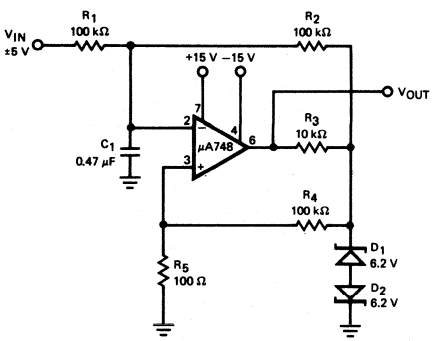


LARGE SIGNAL FEED FORWARD TRANSIENT RESPONSE



TYPICAL APPLICATIONS

PULSE WIDTH MODULATOR



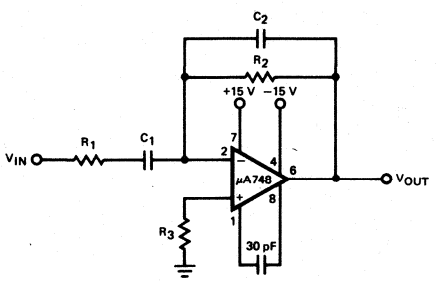
$$f_c = \frac{1}{2\pi\ R2\ C1}$$

$$f_n = \frac{1}{2\pi\ R1\ C1}$$

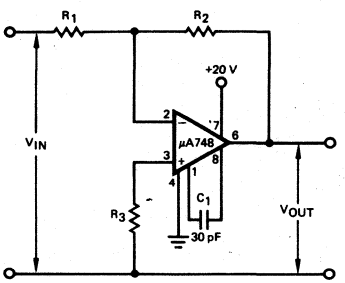
$$= \frac{1}{2\pi\ R2\ C2}$$

$f_c < f_n < f_{unity\ gain}$

PRACTICAL DIFFERENTIATOR



CIRCUIT FOR OPERATING THE μA748 WITHOUT A NEGATIVE SUPPLY



NOTES
1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the metal can, 8.3 mW/°C for the DIP, 5.6 mW/°C for the mini DIP and 7.1 mW/°C for the flatpak.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C case temperature or +75°C ambient temperature.

12

μA749

DUAL AUDIO OPERATIONAL AMPLIFIER/AUDIO PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

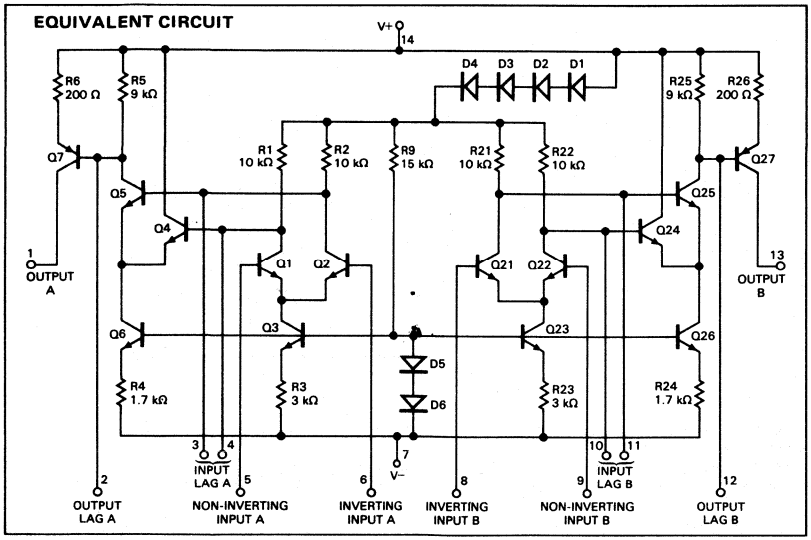
GENERAL DESCRIPTION – The μA749 consists of Two Identical High Gain Operational Amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These three-stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from dc to 10 MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired-OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers and peak detectors.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 25,000 V/V**
- **LARGE COMMON MODE RANGE, +11 V, –13 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

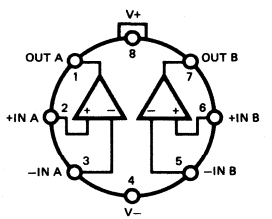
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (μA749 and μA749C)	±18 V
(μA749D)	±12 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	650 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2) (μA749 and μA749C)	±15 V
(μA749D)	±12 V
Storage Temperature Range	
Metal Can, Hermetic DIP	–65°C to +150°C
Molded DIP (μA749PC)	–55°C to +125°C
Operating Temperature Range	
Military (μA749)	–55°C to +125°C
Commercial (μA749C and μA749D)	0°C to +70°C
Lead Temeprature	
Metal Can, Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

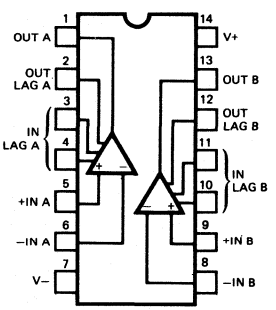


Note: Pin 4 is connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA749D	μA749DHC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA749	μA749DM
μA749C	μA749DC
μA749C	μA749PC

Notes on following pages.

*Planar is a patented Fairchild process.

μA749

ELECTRICAL CHARACTERISTICS ($V+ = \pm 15$ V, R_L = 5 kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	400	nA
Input Bias Current			0.30	0.75	μA
Input Resistance		100	150		kΩ
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V	20,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to −13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Negative Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	V_{OUT} = 0		180	220	mW
Supply Current	V_{OUT} = 0		9.0	10.4	mA
Broadband Noise Figure	R_S = 10 kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μs
Slew Rate (unity gain) (See Fig. 2)	C_1 = 0.02 μF, R_1 = 33 Ω, C_2 = 10 pF		2.0		V/μs
Channel Separation (See Fig. 4)	R_S = 1 kΩ f = 10 kHz		140		dB
The following specifications apply for $V+ = \pm 4.0$ V, R_L = 10 kΩ to Pin 7, $T_A = 25°C$					
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	300	nA
Input Bias Current			0.15	0.75	μA
Supply Current	V_{OUT} = 0		2.5	4.8	mA
Internal Power Dissipation	V_{OUT} = 0		20	36	mW
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V	20,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V
The following specifications apply for $-55°C \leq T_A \leq +125°C$, $V+ = \pm 15$ V, R_L = 5 kΩ to Pin 7:					
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V, $T_A = +125°C$	6,500	20,000		V/V
	$V_{OUT} = \pm 10$ V, $T_A = -55°C$	20,000	30,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		0.05	1.0	μA
	$T_A = -55°C$		0.05	1.5	μA
Input Bias Current	$T_A = +125°C$		0.15	0.75	μA
	$T_A = -55°C$		0.3	3.0	μA
Input Offset Voltage Drift	R_S = 200 Ω, $+25°C \leq T_A \leq +125°C$		3.0		μV/°C
	R_S = 200 Ω, $-55°C \leq T_A \leq +25°C$		3.0		μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		0.5		nA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		nA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		5.0		nA/°C
Supply Current	V_{OUT} = 0, $T_A = +125°C$			9.7	mA
	V_{OUT} = 0, $T_A = -55°C$			13	mA
Internal Power Dissipation	V_{OUT} = 0, $T_A = +125°C$			200	mW
	V_{OUT} = 0, $T_A = -55°C$			300	mW
The following specifications apply for $-55°C \leq T_A \leq +125°C$, $V+ = \pm 4$ V, R_L = 10 kΩ to Pin 7:					
Input Offset Voltage	R_S = 200 Ω		1.5	6.0	mV
Input Offset Current			50	750	nA
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V, $T_A = +125°C$	5,000			V/V
	$V_{OUT} = \pm 2.0$ V, $T_A = -55°C$	20,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C for the DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

12

μA749C

ELECTRICAL CHARACTERISTICS ($V+ = \pm 15$ V, $R_L = 5$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S = 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	750	nA
Input Bias Current			0.30	1.5	μA
Input Resistance		50	150		kΩ
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	$R_S = 200\ \Omega$, $V_{IN} = +11.5$ V to −13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	$R_S = 200\ \Omega$		50	350	μV/V
Negative Supply Voltage Rejection Ratio	$R_S = 200\ \Omega$		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	$V_{OUT} = 0$		180	330	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 10$ kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μs
Slew Rate (unity gain) (See Fig. 2)	$C_1 = 0.02\ \mu F$, $R_1 = 33\ \Omega$, $C_2 = 10$ pF		2.0		V/μs
Channel Separation (See Fig. 4)	$R_S = 1$ kΩ, f = 10 kHz		140		dB

The following specifications apply for $V+ = \pm 4.0$ V, $R_L = 10$ kΩ to Pin 7, $T_A = 25°C$:

Input Offset Voltage	$R_S = 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	600	nA
Input Bias Current			0.3	1.5	μA
Supply Current	$V_{OUT} = 0$		2.5		mA
Internal Power Dissipation	$V_{OUT} = 0$		20		mW
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V	15,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

The following specifications apply for $0°C \leq T_A \leq +70°C$, $V+ = \pm 15$ V, $R_L = 5$ kΩ to Pin 7:

Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V, $T_A = +70°C$	8,000	40,000		V/V
	$V_{OUT} = \pm 10$ V, $T_A = 0°C$	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	$R_S = 200\ \Omega$		1.0	9.0	mV
Input Offset Current			0.05	1.5	μA
Input Bias Current			0.3	3.0	μA
Input Offset Voltage Drift	$R_S = 200\ \Omega$, $+25°C \leq T_A \leq +70°C$		3.0		μV/°C
	$R_S = 200\ \Omega$, $0°C \leq T_A \leq +25°C$		3.0		μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +70°C$		0.5		nA/°C
	$0°C \leq T_A \leq +25°C$		2.0		nA/°C
Input Bias Current Drift	$0°C \leq T_A \leq +70°C$		4.0		nA/°C

The following specifications apply for $0°C \leq T_A \leq +70°C$, $V+ = \pm 4$ V, $R_L = 10$ kΩ to Pin 7:

Input Offset Voltage	$R_S = 200\ \Omega$		1.5	9.0	mV
Input Offset Current			0.05	1.0	μA
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V, $T_A = 70°C$	8,000			V/V
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V, $T_A = 0°C$	15,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

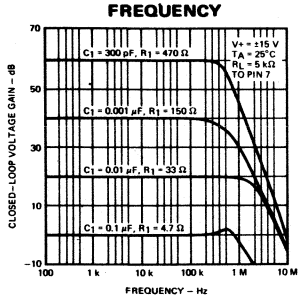
μA749D

ELECTRICAL CHARACTERISTICS ($V+ = \pm 6$ V, $R_L = 10$ kΩ to pin 4. $T_A = 25°C$ unless otherwise specified)

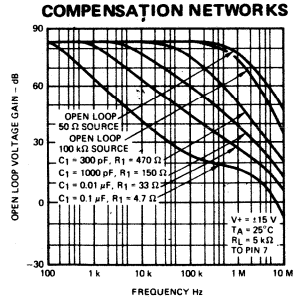
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	10	mV
Input Offset Current			50	600	nA
Input Bias Current			300	1500	nA
Input Resistance		50	150		kΩ
Large Signal Voltage Gain	$V_{OUT} = \pm 4.0$ V	10,000	20,000		V/V
Positive Output Voltage Swing		+4.5	+5.0		V
Negative Output Voltage Swing		−5.5	−6.0		V
Output Resistance	f = 1.0 kHz		10		kΩ
Input Voltage Range		−4.0		+2.5	V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50	100	μV/V
Power Consumption (including load)	$V_{OUT} = 0$	24	36	54	mW
Supply Current (including load)	$V_{OUT} = 0$	2.0	3.0	4.5	mA
Turn On Delay (See Figure 5)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ kΩ		0.2		μs
Turn Off Delay (See Figure 5)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ kΩ		0.3		μs
Channel Separation (See Figure 7)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB

TYPICAL PERFORMANCE CURVES FOR μA749 AND μA749C

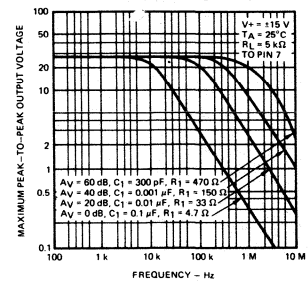
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



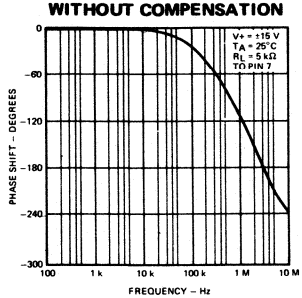
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



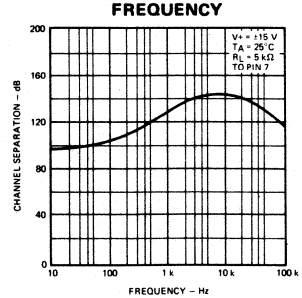
OUTPUT CAPABILITY AS A FUNCTION OF FREQUENCY AND COMPENSATION



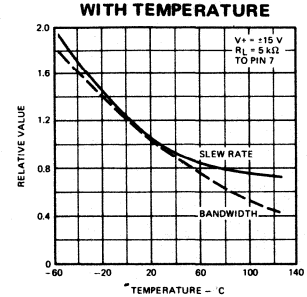
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

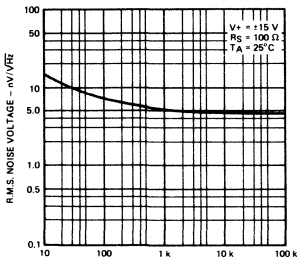


CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE

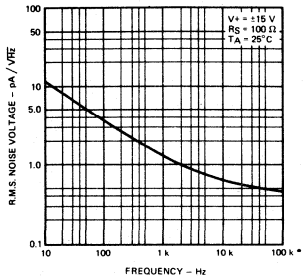


TYPICAL PERFORMANCE CURVES FOR μA749 AND μA749C

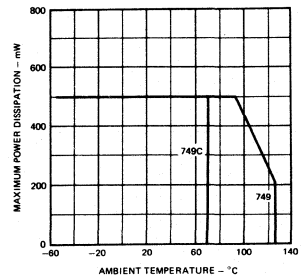
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



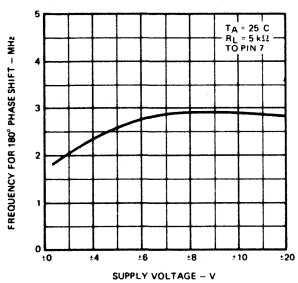
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



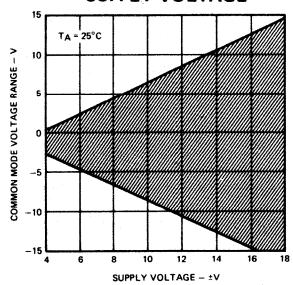
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



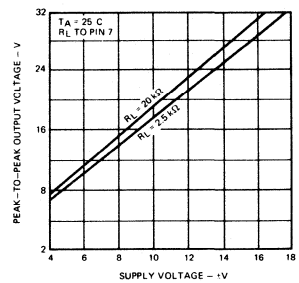
OPEN LOOP 180° PHASE SHIFT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



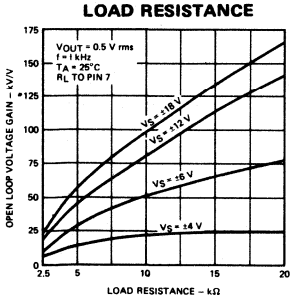
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



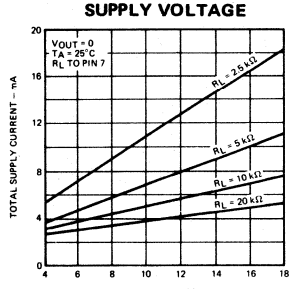
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



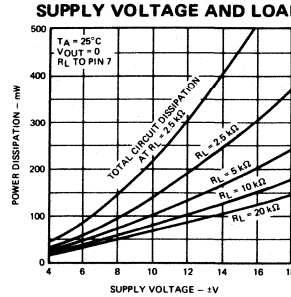
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



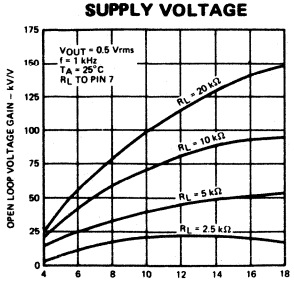
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



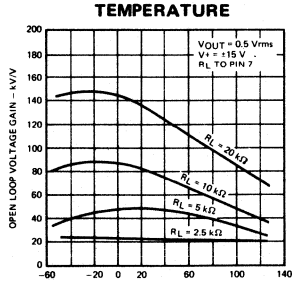
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



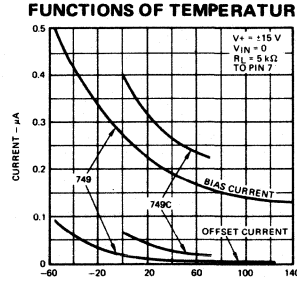
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

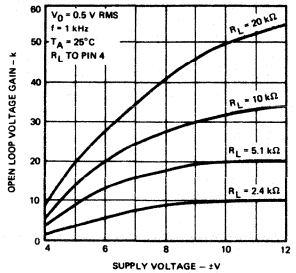


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

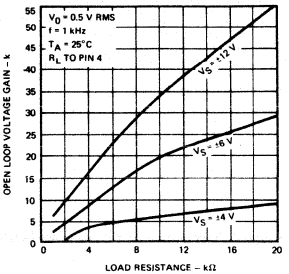


TYPICAL PERFORMANCE CURVES FOR μA749D

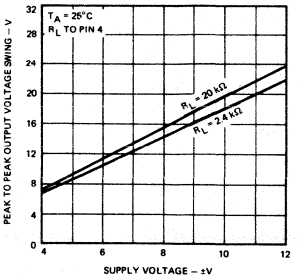
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



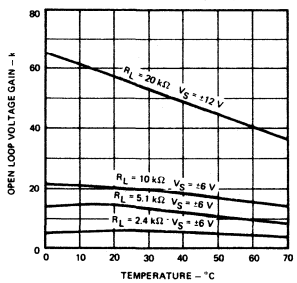
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



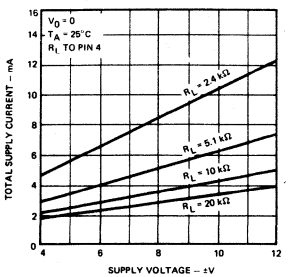
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



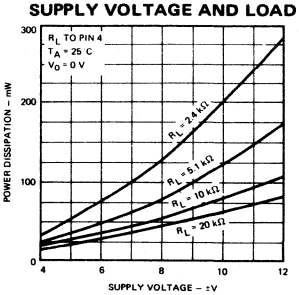
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



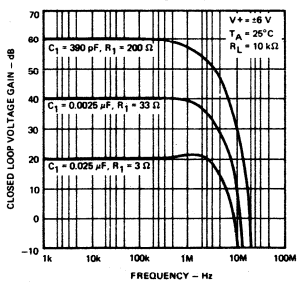
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



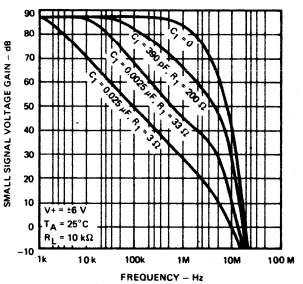
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



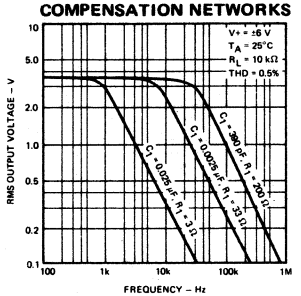
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



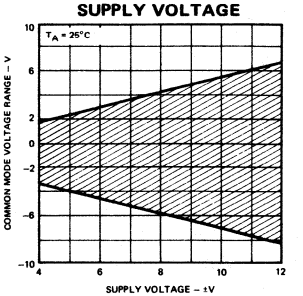
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



12

OFFSET NULL* NETWORK μA749 AND μA749C

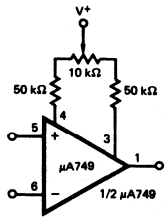


Fig. 1

FREQUENCY RESPONSE* TEST CIRCUIT μA749 AND μA749C

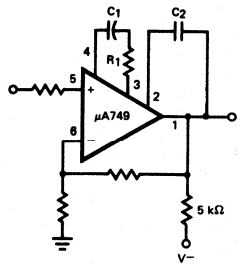


Fig. 2

PULSE RESPONSE* WAVEFORMS μA749 AND μA749C

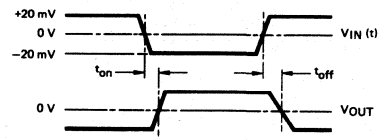


Fig. 3

CHANNEL SEPARATION* TEST CIRCUIT μA749 AND μA749C

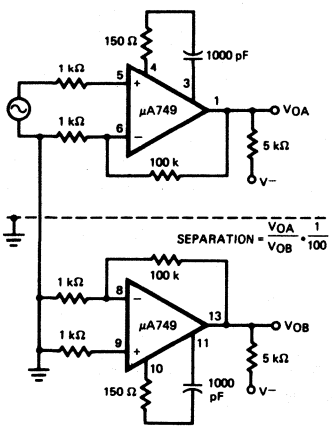


Fig. 4

PULSE RESPONSE WAVEFORMS μA749D

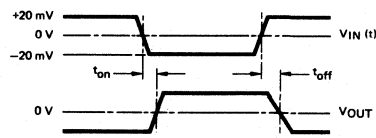


Fig. 5

FREQUENCY RESPONSE TEST CIRCUIT μA749D

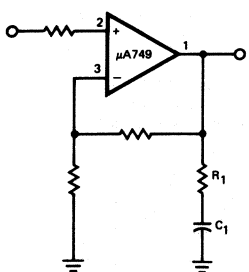


Fig. 6

CHANNEL SEPARATION TEST CIRCUIT μA749D

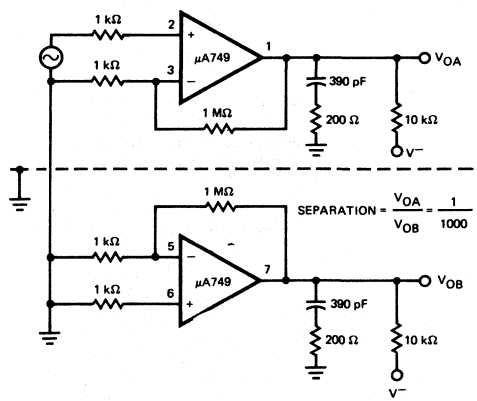
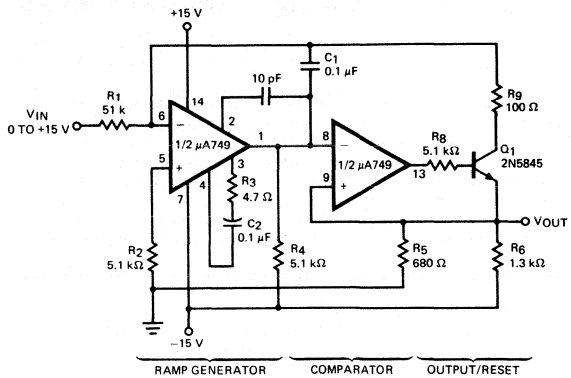


Fig. 7

*Pin numbers refer to Dual-in-line Package

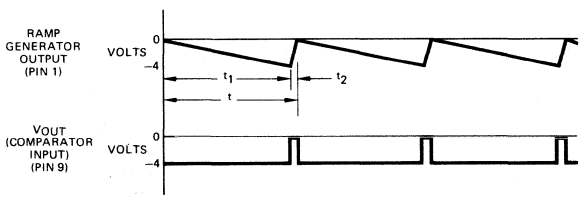
TYPICAL APPLICATIONS

VOLTAGE TO FREQUENCY CONVERTER



$R^* = R$ pin 1 + R9 + R_{CE} Q1 + R6 output stage.

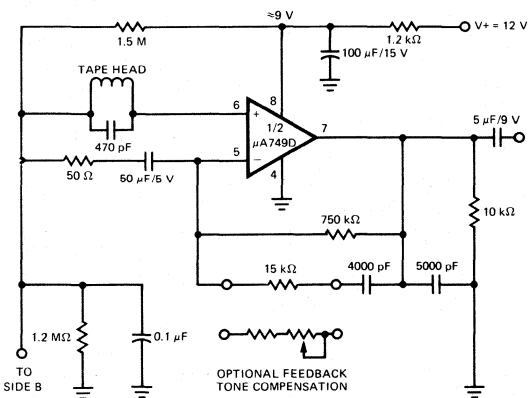
WAVEFORMS

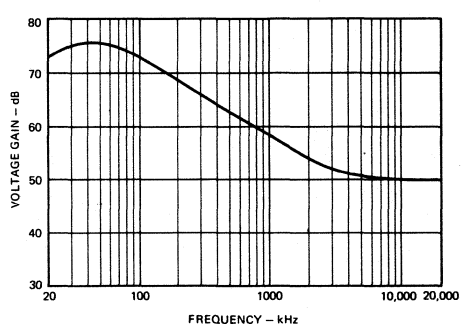


$$t = t1 + t2 = 4\,\frac{R1\,C1}{V_{IN}} + \frac{4R^*\,C1}{15}$$

12

STEREO TAPE PREAMPLIFIER





TYPICAL PERFORMANCE

Gain at 1 kHz	60 dB
Output Voltage Swing	2.8 V rms
Power Consumption	30 mW

μA776

MULTI-PURPOSE PROGRAMMABLE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

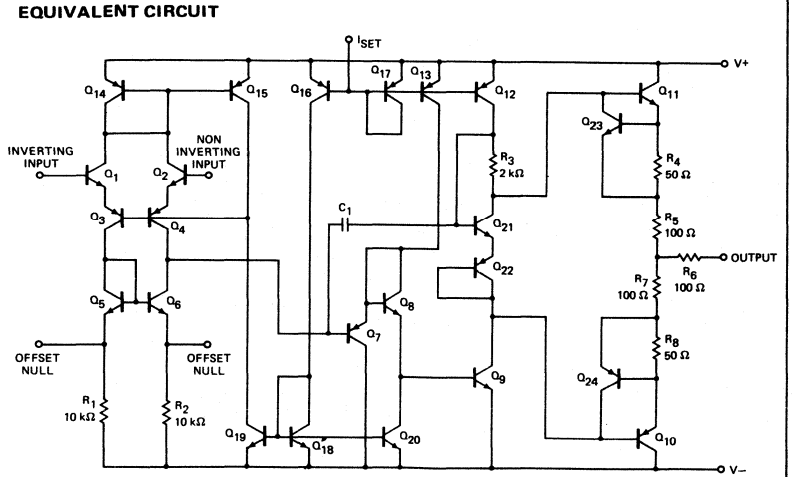
DESCRIPTION – The μA776 Programmable Operational Amplifier is constructed using the Fairchild Planar* epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the μA741. Internal frequency compensation, absence of latch-up, high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

- **MICROPOWER CONSUMPTION**
- **±1.2V to ±18V OPERATION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **LOW INPUT BIAS CURRENTS**
- **WIDE PROGRAMMING RANGE**
- **HIGH SLEW RATE**
- **LOW NOISE**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET NULL CAPABILITY**
- **NO LATCH-UP**

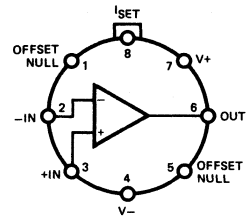
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage Between Offset Null and V–	±0.5 V
I_{SET} (Maximum Current at I_{SET})	500 μA
V_{SET} (Maximum Voltage to Ground at I_{SET})	$(V+ - 2.0\ V) \leq V_{SET} \leq V+$
Storage Temperature Range	
Metal Can, DIP	–65°C to +150°C
Mini DIP	–55°C to +125°C
Operating Temperature Range	
Military (μA776)	–55°C to +125°C
Commercial (μA776C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	
Metal Can, DIP	300°C
Mini DIP	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



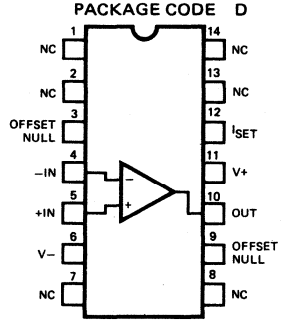
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA776	μA776HM
μA776C	μA776HC

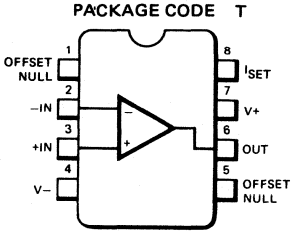
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA776	μA776DM
μA776	μA776DC

8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA776C	μA776TC

*Planar is a patented Fairchild process.

±15 V OPERATION FOR μA776

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

PARAMETERS		CONDITIONS	I_{SET} = 1.5μA			I_{SET} = 15μA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage		$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current		$R_S \leq 10k\Omega$		0.7	3.0		2.0	15	nA
Input Bias Current				2.0	7.5		15	50	nA
Input Resistance				50			5.0		MΩ
Input Capacitance				2.0			2.0		pF
Offset Voltage Adjustment Range				9.0			18		mV
Large Signal Voltage Gain		$R_L \geq 75k\Omega$, V_{OUT} = ±10V	200k	400k					V/V
		$R_L \geq 5k\Omega$, V_{OUT} = ±10V				100k	400k		V/V
Output Resistance				5.0k			1.0k		Ω
Output Short-Circuit Current				3.0			12		mA
Supply Current				20	25		160	180	μA
Power Consumption					0.75			5.4	mW
Transient Response (unity gain)	Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L = 100pF		1.6			0.35		μs
	Overshoot			0			10		%
Slew Rate		$R_L \geq 5k\Omega$		0.1			0.8		V/μs
Output Voltage Swing		$R_L \geq 75k\Omega$	±12	±14					V
		$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply $-55°C \leq T_A \leq +125°C$									
Input Offset Voltage		$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current		T_A = +125°C			5.0			15	nA
		T_A = −55°C			10			40	nA
Input Bias Current		T_A = +125°C			7.5			50	nA
		T_A = −55°C			20			120	nA
Input Voltage Range			±10			±10			V
Common Mode Rejection Ratio		$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10k\Omega$		25	150		25	150	μV/V
Large Signal Voltage Gain		$R_L \geq 75k\Omega$, V_{OUT}=±10V	100k			75k			V/V
Output Voltage Swing		$R_L \geq 75k\Omega$	±10			±10			V
Supply Current					30			200	μA
Power Consumption					0.9			6.0	mW

±3 V OPERATION FOR μA776

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

PARAMETERS	CONDITIONS	I_{SET} = 1.5μA			I_{SET} = 15μA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current			0.7	3.0		2.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	50k	200k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				50k	200k		V/V
Output Resistance			5k			1k		Ω
Output Short-Circuit Current			3.0			5.0		mA
Supply Current			13	20		130	160	μA
Power Consumption			78	120		780	960	μW
Transient Response (unity gain) — Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$		3.0			0.6		μs
Transient Response (unity gain) — Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	T_A = +125°C			5.0			15	nA
	T_A = −55°C			10			40	nA
Input Bias Current	T_A = +125°C			7.5			50	nA
	T_A = −55°C			20			120	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	μV/V
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k						V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±1.9	±2.1		V
Supply Current				25			180	μA
Power Consumption				150			1080	μW

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for the DIP, and 5.6 mW/°C for the Mini DIP.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short Circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for $I_{SET} \leq 30$ μA.

±15 V OPERATION FOR μA776C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

PARAMETERS		CONDITIONS	I_{SET} = 1.5μA MIN	TYP	MAX	I_{SET} = 15μA MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current				0.7	6.0		2.0	25	nA
Input Bias Current				2.0	10		15	50	nA
Input Resistance				50			5.0		MΩ
Input Capacitance				2.0			2.0		pF
Offset Voltage Adjustment Range				9.0			18		mV
Large Signal Voltage Gain		$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k	400k					V/V
		$R_L \geq 5k\Omega$, V_{OUT}=±10V				50k	400k		V/V
Output Resistance				5.0			1.0		kΩ
Output Short-Circuit Current				3.0			12		mA
Supply Current				20	30		160	190	μA
Power Consumption					0.9			5.7	mW
Transient Response (unity gain)	Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$		1.6			0.35		μs
	Overshoot			0			10		%
Slew Rate		$R_L \geq 5k\Omega$		0.1			0.8		V/μs
Output Voltage Swing		$R_L \geq 75k\Omega$	±12	±14					V
		$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply to $0°C \leq T_A \leq +70°C$									
Input Offset Voltage		$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current		T_A = +70°C			6.0			25	nA
		T_A = 0°C			10			40	nA
Input Bias Current		T_A = +70°C			10			50	nA
		T_A = 0°C			20			100	nA
Input Voltage Range			±10			±10			V
Common Mode Rejection Ratio		$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large Signal Voltage Gain		$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k			50k			V/V
Output Voltage Swing		$R_L \geq 75k\Omega$	±10			±10			V
Supply Current					35			200	μA
Power Consumption					1.05			6.0	mW

12

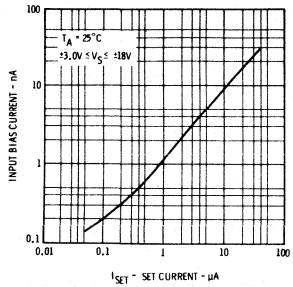
±3 V OPERATION FOR μA776C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

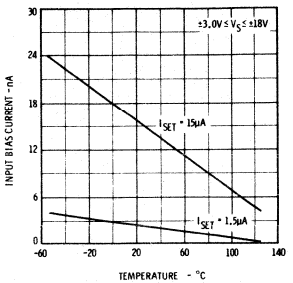
PARAMETERS	CONDITIONS	I_{SET} = 1.5μA			I_{SET} = 15μA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		2.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k	200k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25 k	200k		V/V
Output Resistance			5.0			1.0		kΩ
Output Short-Circuit Current			3.0			5.0		mA
Supply Current			13	20		130	170	μA
Power Consumption			78	120		780	1020	μW
Transient Response (unity gain) — Rise Time	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L = 100pF		3.0			0.6		μs
Transient Response (unity gain) — Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current	T_A = +70°C			6.0			25	nA
	T_A = 0°C			10			40	nA
Input Bias Current	T_A = +70°C			10			50	nA
	T_A = 0°C			20			100	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k						V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±2.0	±2.1		V
Supply Current				25			180	μA
Power Consumption				150			1080	μW

TYPICAL PERFORMANCE CURVES FOR μA776 AND μA776C

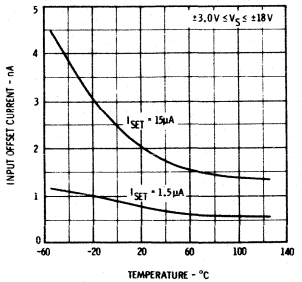
INPUT BIAS CURRENT AS A FUNCTION OF SET CURRENT



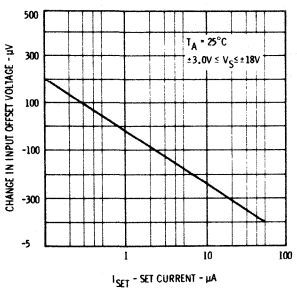
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



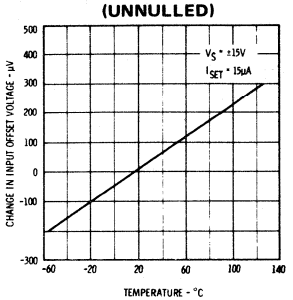
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



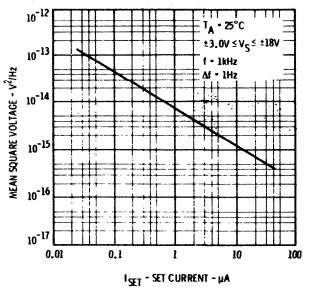
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF SET CURRENT



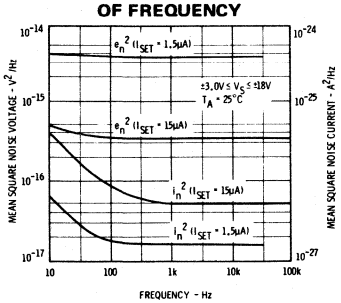
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE (UNNULLED)



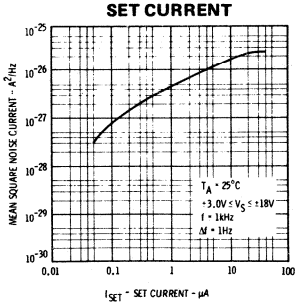
INPUT NOISE VOLTAGE AS A FUNCTION OF SET CURRENT



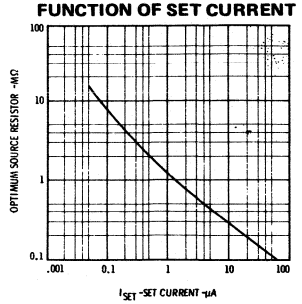
INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY



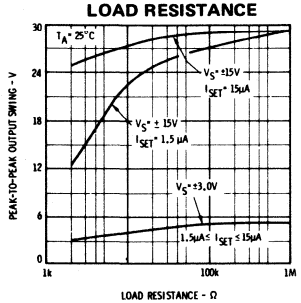
INPUT NOISE CURRENT AS A FUNCTION OF SET CURRENT



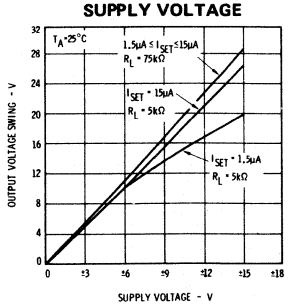
OPTIMUM SOURCE RESISTOR FOR MINIMUM NOISE AS A FUNCTION OF SET CURRENT



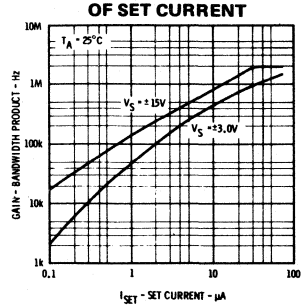
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



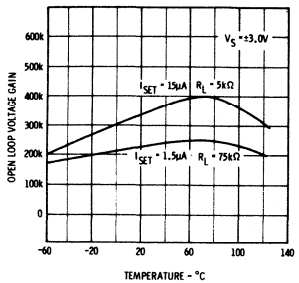
GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF SET CURRENT



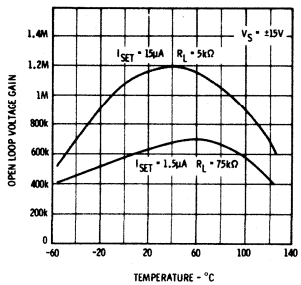
12

TYPICAL PERFORMANCE CURVES FOR μA776 AND μA776C

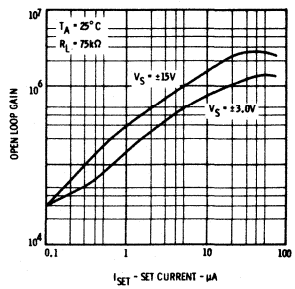
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



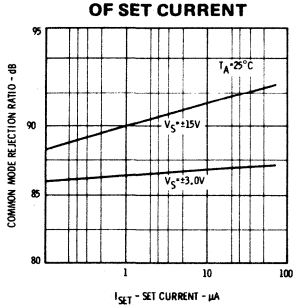
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



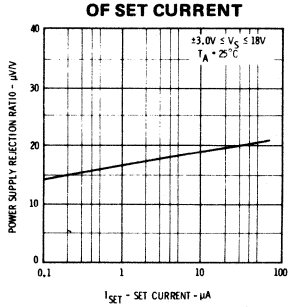
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SET CURRENT



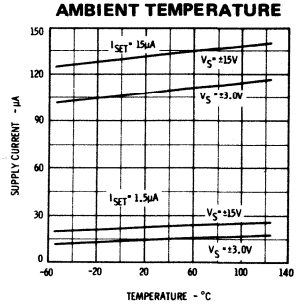
COMMON MODE REJECTION RATIO AS A FUNCTION OF SET CURRENT



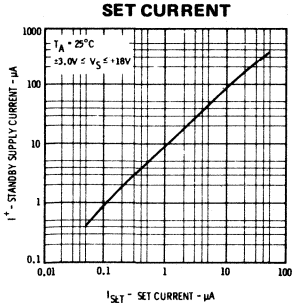
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF SET CURRENT



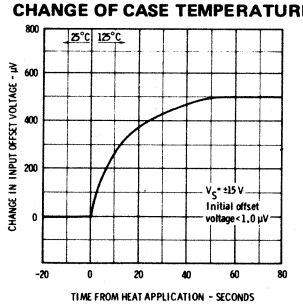
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



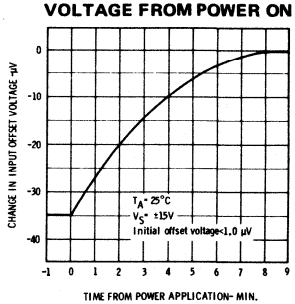
STANDBY SUPPLY CURRENT AS A FUNCTION OF SET CURRENT



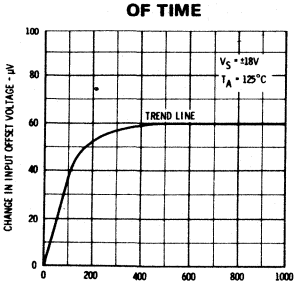
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



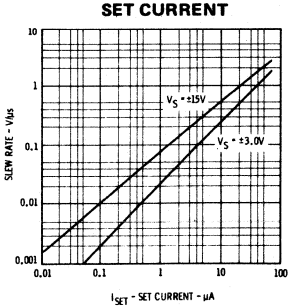
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER ON



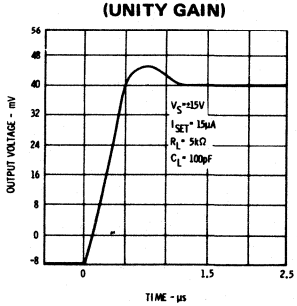
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



SLEW RATE AS A FUNCTION OF SET CURRENT

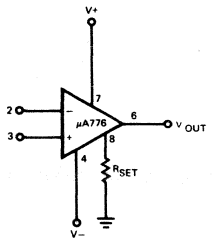


VOLTAGE FOLLOWER TRANSIENT RESPONSE (UNITY GAIN)

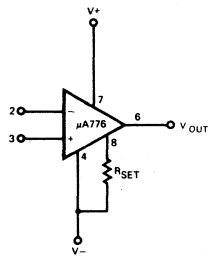


BIASING CIRCUITS

RESISTOR BIASING



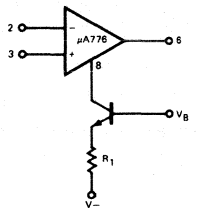
R_{SET} CONNECTED TO GROUND



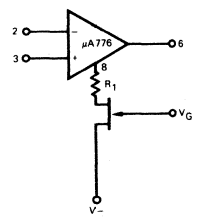
R_{SET} CONNECTED TO V^-

* Recommended for supply voltages less than ±6V.

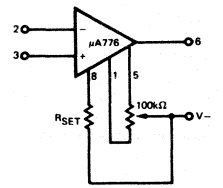
TRANSISTOR CURRENT SOURCE BIASING



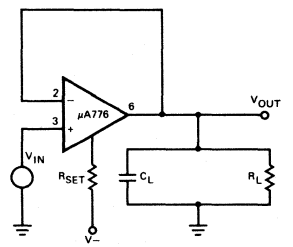
FET CURRENT SOURCE BIASING



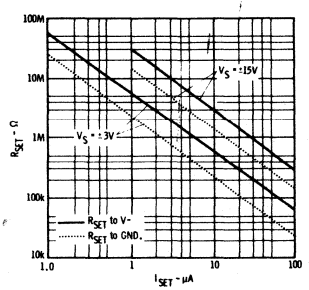
VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



SET CURRENT AS A FUNCTION OF SET RESISTOR



QUIESCENT CURRENT SETTING RESISTOR (I_{SET} TO V^-)

V_S	I_{SET}	
	1.5μA	15μA
±1.5 V	1.7MΩ	170kΩ
±3.0 V	3.6MΩ	360kΩ
±6.0 V	7.5MΩ	750kΩ
±15 V	20MΩ	2.0MΩ

Note: The μA776 may be operated with R_{SET} connected to ground or V−.

I_{SET} EQUATIONS:

$$I_{SET} = \frac{V^+ - 0.7 - V^-}{R_{SET}}$$

where R_{SET} is connected to V^-

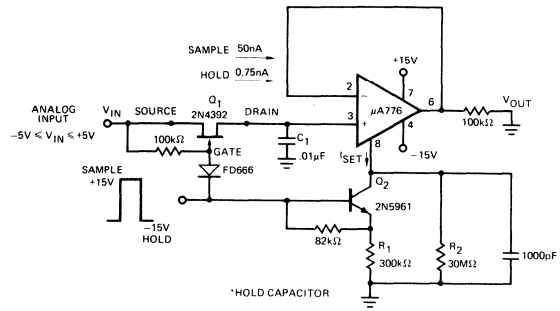
$$I_{SET} = \frac{V^+ - 0.7}{R_{SET}}$$

where R_{SET} is connected to ground.

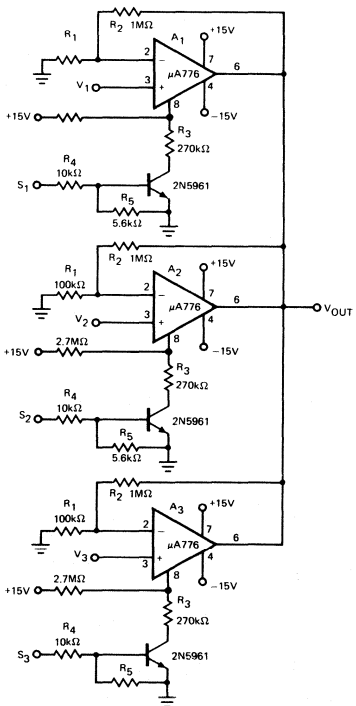
12

TYPICAL APPLICATIONS

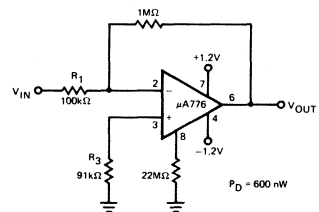
HIGH ACCURACY SAMPLE AND HOLD



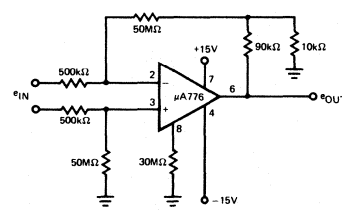
MULTIPLEXING AND SIGNAL CONDITIONING WITHOUT FETs



NANO-WATT AMPLIFIER



HIGH INPUT IMPEDANCE AMPLIFIER



μA777

PRECISION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

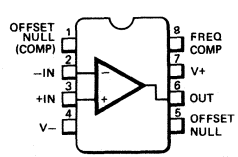
GENERAL DESCRIPTION – The μA777C is a monolithic Precision Operational Amplifier constructed using a low noise Fairchild Planar* epitaxial process. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777C maintains full ±30 V differential voltage range. The internal construction utilizes isothermal layout and special electrical design to maintain system performance despite variations in temperature or output load. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and easily used.

- **LOW OFFSET VOLTAGE AND OFFSET CURRENT**
- **LOW OFFSET VOLTAGE AND CURRENT DRIFT**
- **LOW INPUT BIAS CURRENT**
- **LOW INPUT NOISE VOLTAGE**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can and Hermetic DIP	-65° C to +150° C
Mini DIP	-55° C to +125° C
Operating Temperature Range	0° C to 70° C
Lead Temperature	
Metal Can and Hermetic DIP(Soldering, 60 s)	300° C
Mini DIP (Soldering, 10 s)	260° C
Output Short Circuit Duration (Note 3)	Indefinite

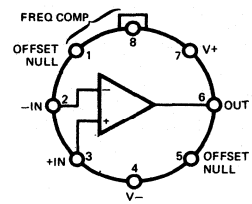
CONNECTION DIAGRAM
8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777TC

CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

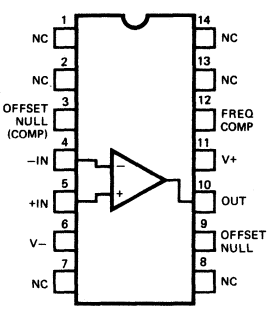


NOTE: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777DC

12

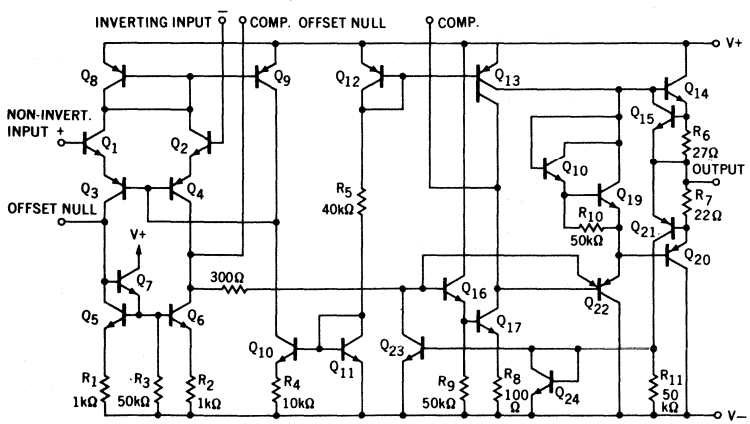
Notes on following pages.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS FOR μA777C (V_S = ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

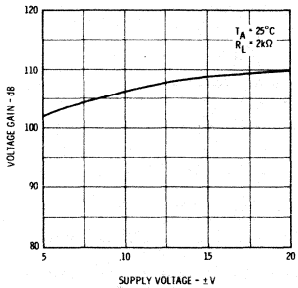
PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\ k\Omega$		0.7	5.0	mV
Input Offset Current				0.7	20.0	nA
Input Bias Current				25	100	nA
Input Resistance			1.0	2.0		MΩ
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				±25		mV
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	25,000	250,000		V/V
Output Resistance				100		Ω
Output Short Circuit Current				±25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2\ k\Omega$		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \leq 2\ k\Omega$, C_C = 3.5 pF		5.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$						
Input Offset Voltage		$R_S \leq 50\ k\Omega$		0.8	5.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50\ k\Omega$		4.0	30	μV/°C
Input Offset Current					40	nA
Average Input Offset Current Drift		$25°C \leq T_A \leq +70°C$		0.01	0.3	nA/°C
		$0°C \leq T_A \leq +25°C$		0.02	0.6	nA/°C
Input Bias Current					200	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 50\ k\Omega$	70	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50\ k\Omega$		15	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing		$R_L \geq 10\ k\Omega$	±12	±14		V
		$R_L \geq 2\ k\Omega$	±10	±13		V
Power Consumption				60	100	mW

EQUIVALENT CIRCUIT

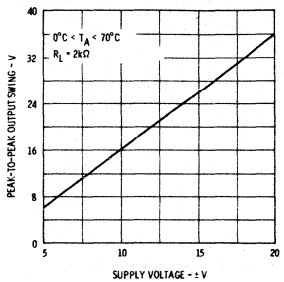


TYPICAL PERFORMANCE CURVES

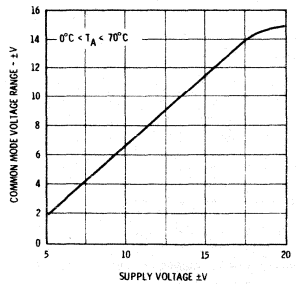
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



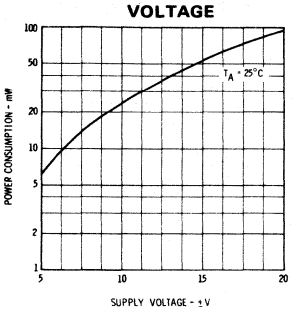
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



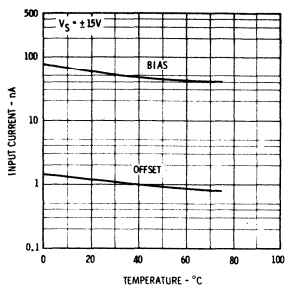
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



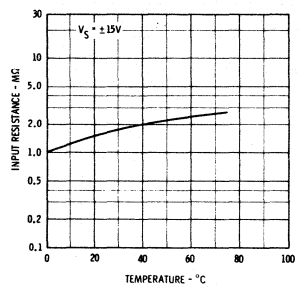
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



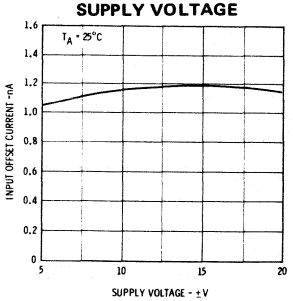
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



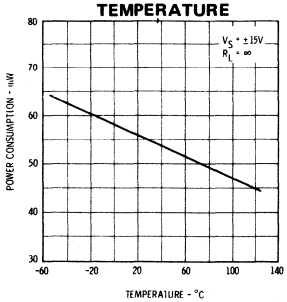
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



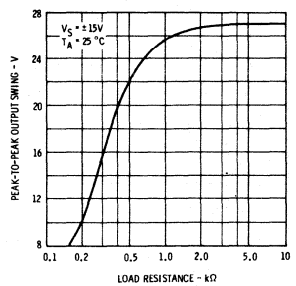
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



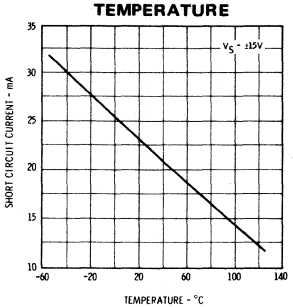
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



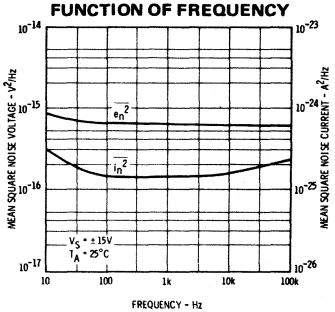
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



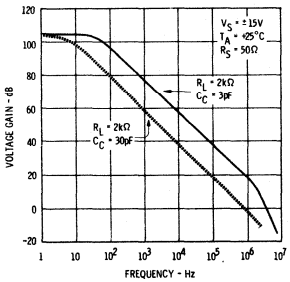
INPUT NOISE AND CURRENT AS A FUNCTION OF FREQUENCY



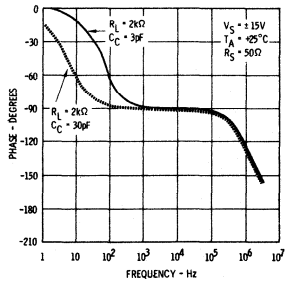
12

TYPICAL PERFORMANCE CURVES

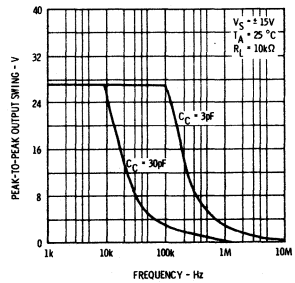
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



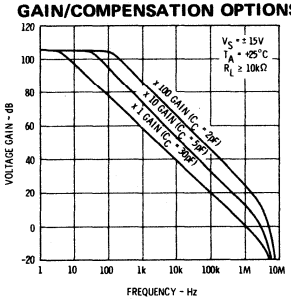
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



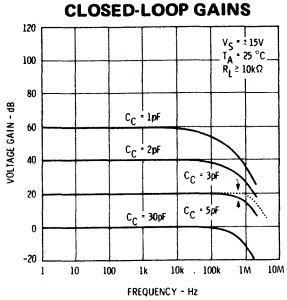
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



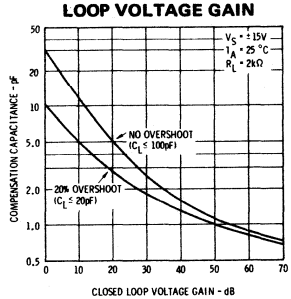
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



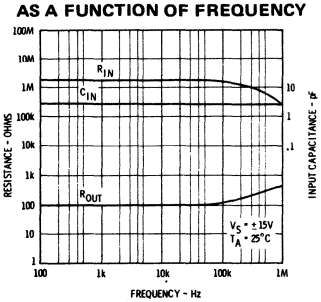
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



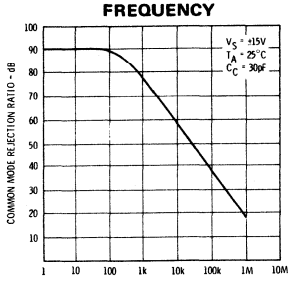
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



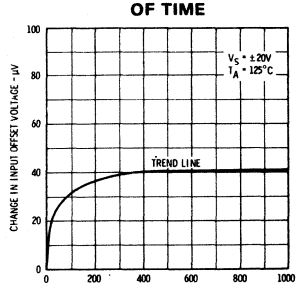
INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



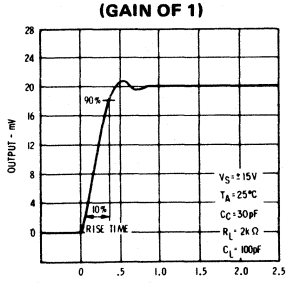
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



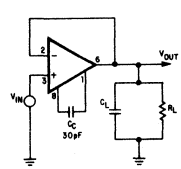
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



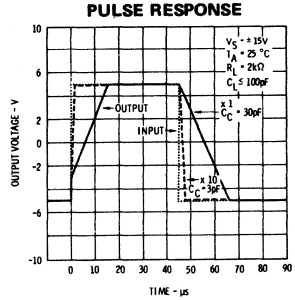
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

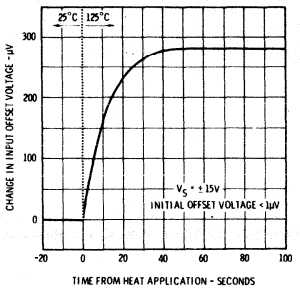


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

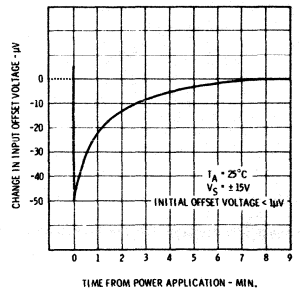


TYPICAL PERFORMANCE CURVES

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

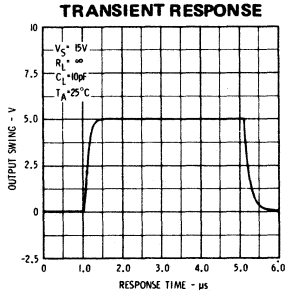


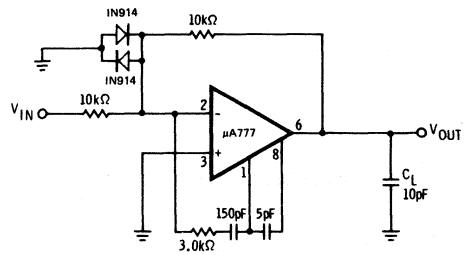
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



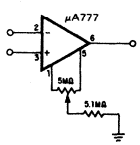
FEED FORWARD COMPENSATION

LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE

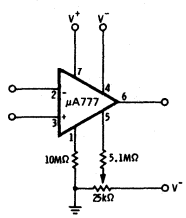




VOLTAGE OFFSET NULL CIRCUIT

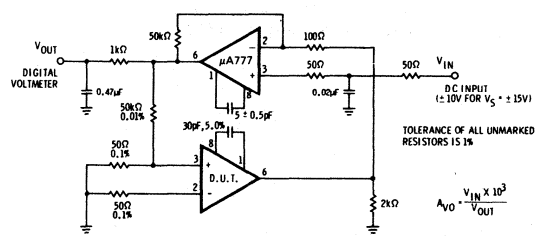


SUGGESTED



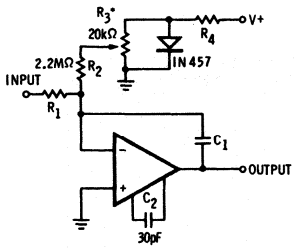
ALTERNATE

GAIN TEST CIRCUIT



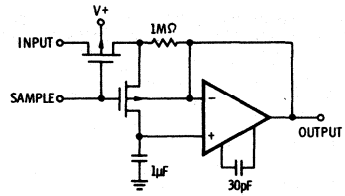
TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR

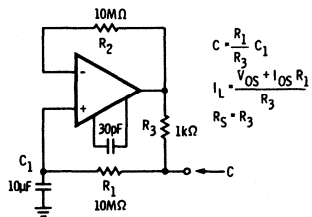


*Adjust R_3 for minimum integrator drift

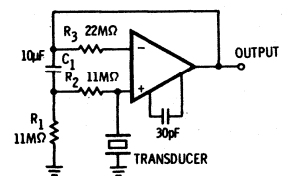
SAMPLE AND HOLD



CAPACITANCE MULTIPLIER

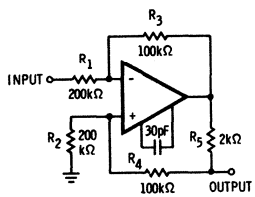


AMPLIFIER FOR CAPACITANCE TRANSDUCERS



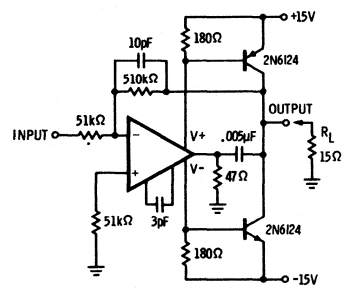
Low Frequency Cutoff $R_1 \times C_1$

BILATERAL CURRENT SOURCE

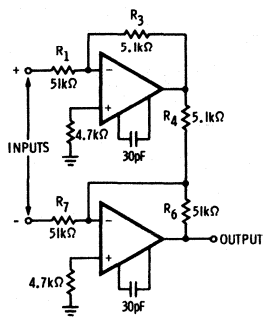


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5} \; ; \; R_1 = R_2; R_3 = R_4 + R_5$$

HIGH SLEW RATE POWER AMPLIFIER



± 100 V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER



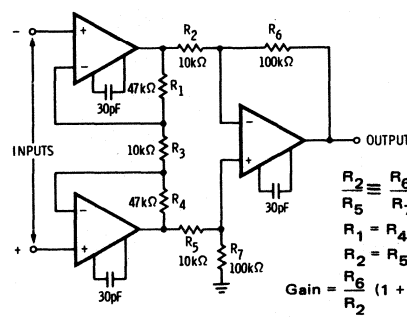
$\frac{R_1}{R_7} \equiv \frac{R_3}{R_4}$ for best CMRR

$R_3 = R_4$

$R_1 = R_6 = 10R_3$

$\text{Gain} = \frac{R_7}{R_6}$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$\frac{R_2}{R_5} \equiv \frac{R_6}{R_7}$ for best CMRR

$R_1 = R_4$

$R_2 = R_5$

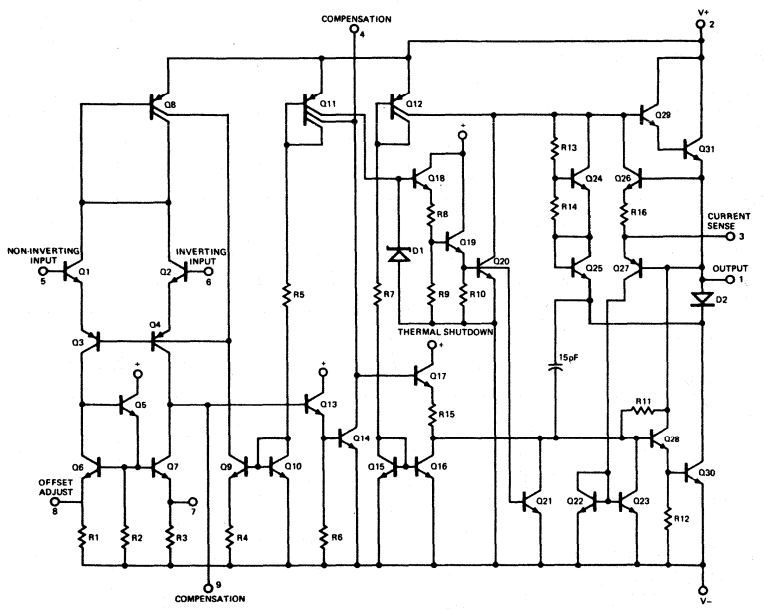
$\text{Gain} = \frac{R_6}{R_2}\left(1 + \frac{2R_1}{R_3}\right)$

μA791
POWER OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA791 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* Epitaxial process with input characteristics similar to the μA741 operational amplifier and 1A available output current. It is intended for use in a wide variety of applications including audio amplifiers, servo amplifiers, and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required. The μA791 is thermal overload and short circuit protected.

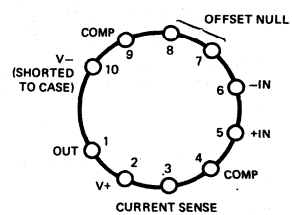
- **CURRENT OUTPUT TO 1 A**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **NO LATCH UP**
- **LARGE COMMON MODE AND DIFFERENTIAL MODE RANGES**
- **THERMAL OVERLOAD PROTECTION**

EQUIVALENT CIRCUIT



NOTE: Lead connections shown are for metal can

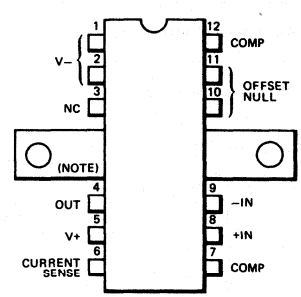
CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5H
PACKAGE CODE K



ORDER INFORMATION

TYPE	PART NO.
μA791C	μA791KC
μA791	μA791KM

12-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODE P5



ORDER INFORMATION

TYPE	PART NO.
μA791C	μA791P5

NOTES:
The heat sink wings on the P-package are internally connected to V–.
Both pin 1 and pin 2 must be connected externally to V–.

12

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military (μA791)	±22 V
Commercial (μA791C)	±18 V
Peak Output Current	1.25 A
Continuous Internal Power Dissipation (Total Package) (Note 1)	Internally Limited
Peak Internal Power Dissipation (Per Output Transistor for $t \leq 5$ s, Note 2)	15 W
Differential Input Voltage	±30 V
Input Voltage (Note 3)	±15 V
Voltages between offset Null and V−	±0.5 V
Operating Junction Temperature	
Military (μA791)	−55°C to +150°C
Commercial (μA791C)	0° C to +125° C
Storage Temperature Range	
Metal Can	-65° C to +150° C
Molded Power DIP	-55° C to +125° C
Lead Temperatures	
Metal Can (Soldering, 60 s max.)	280° C
Molded Power DIP (Soldering, 10 s max.)	260° C

NOTES:

1. Thermal resistance of the packages (without a heat sink)

Package	Junction to Case		Junction to Ambient		Unit
	Typ	Max	Typ	Max	
TO-3 Type (5H)	4	6	35	40	°C/W
Dual In-Line Power (9W)	8	12	50	55	

2. Under short circuit conditions, the safe operating area and dc power dissipation limitations must be observed.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

μA791C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_J = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	1.0		MΩ
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10 V	20k			V/V
	R_L = 10 Ω V_{OUT} = ±10 V	20k			V/V
Output Voltage Swing	R_{SC} = 0, R_L = 1kΩ	±11.5	±14		V
	R_{SC} = 0, R_L = 10 Ω	±10	±12.2		V
Output Short Circuit Current	R_{SC} = 0.7Ω		1000		mA
	R_{SC} = 1.5Ω		500		mA
Supply Current (Zero Signal)				30	mA
The following specifications apply for $0°C \leq T_J \leq 125°C$					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10 V	15k			V/V
	R_L = 10 Ω, V_{OUT} = ±10 V	15k			V/V
Output Voltage Swing	R_{SC} = 0, R_L = 1 kΩ	±10			V
	R_{SC} = 0, R_L = 10 Ω	±10			V
Supply Current (Zero signal)				30	mA

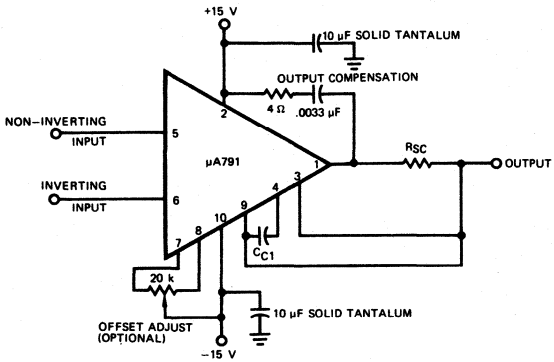
μA791

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_J = 25°C unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	R_L = 1 kΩ	50,000			V/V
	R_L = 10 Ω	50,000			V/V
Output Voltage Swing	R_{SC} = 0, R_L = 1 kΩ	±12	±14		V
	R_{SC} = 0, R_L = 10 Ω	±10	±12.2		V
Output Short Circuit Current	R_{SC} = 0.7Ω		1000		mA
	R_{SC} = 1.5Ω		500		mA
Supply Current (Zero Signal)				25	mA
The following specifications apply for $-55°C \leq T_J \leq 150°C$					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Common Mode Rejection Ratio		70			dB
Power Supply Rejection Ratio				150	μV/V
Large Signal Voltage Gain	R_L = 1 kΩ	25,000			V/V
	R_L = 10 Ω	25,000			V/V
Output Voltage Swing	R_{SC} = 0, R_L = 1 kΩ	±10			V
	R_{SC} = 0, R_L = 10 Ω	±10			V
Supply Current (Zero Signal)				30	mA

12

FREQUENCY COMPENSATION



GAIN	C_{C1}
1	100 pF
10	10 pF
100	2 pF

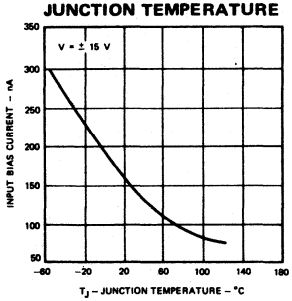
R_{SC}	I_{SC}
0.6Ω	1.0 A
1.5Ω	500 mA
3.0Ω	250 mA

NOTES

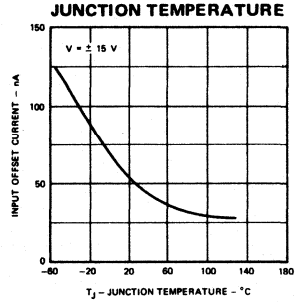
1. Power supply decoupling capacitors and compensation networks must have short leads and must be located at the amplifier pins.
2. When short circuit limiting is not required, short terminals one and three together.
3. Lead connections shown are for Metal Can only.

TYPICAL PERFORMANCE CURVES FOR μA791 AND μA791C

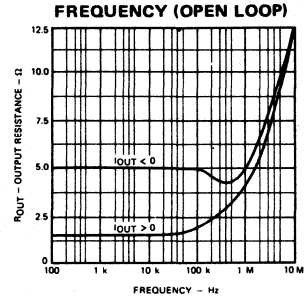
INPUT BIAS CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



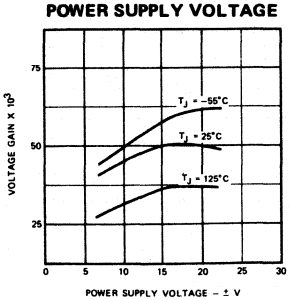
INPUT OFFSET CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



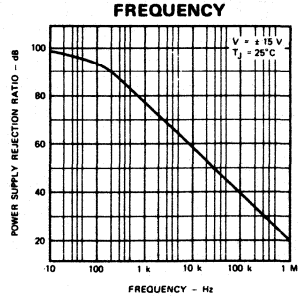
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY (OPEN LOOP)



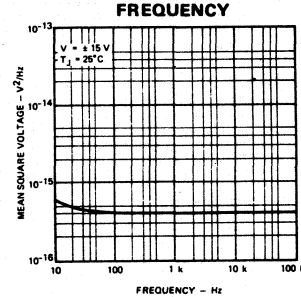
VOLTAGE GAIN AS A FUNCTION OF POWER SUPPLY VOLTAGE



POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREQUENCY

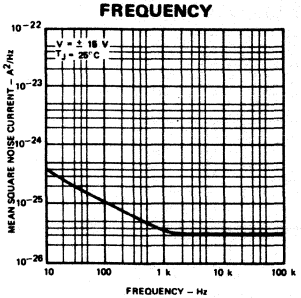


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

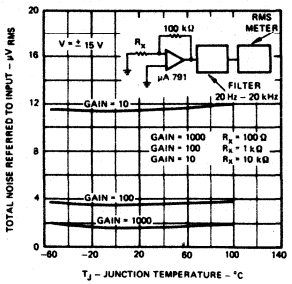


TYPICAL PERFORMANCE CURVES FOR μA791 and μA791C (Cont'd)

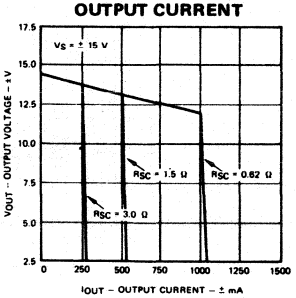
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



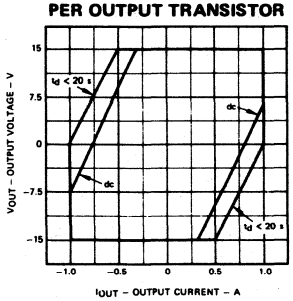
TOTAL NOISE (20 Hz-20 kHz) AS A FUNCTION OF JUNCTION TEMPERATURE



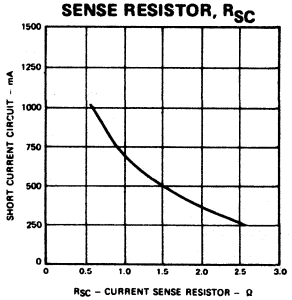
OUTPUT VOLTAGE SWING AS A FUNCTION OF OUTPUT CURRENT



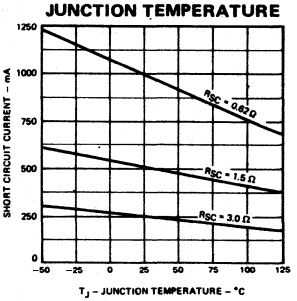
OUTPUT SAFE OPERATING AREA PER OUTPUT TRANSISTOR



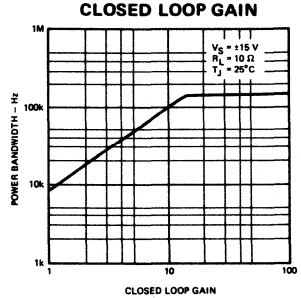
SHORT CIRCUIT CURRENT AS A FUNCTION OF CURRENT SENSE RESISTOR, R_{SC}



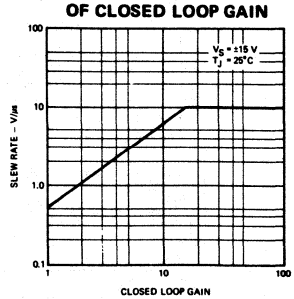
SHORT CIRCUIT CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



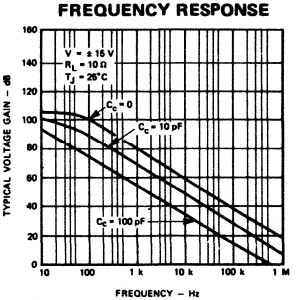
POWER BANDWIDTH AS A FUNCTION OF CLOSED LOOP GAIN



SLEW RATE AS A FUNCTION OF CLOSED LOOP GAIN



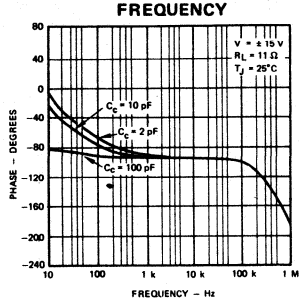
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY RESPONSE



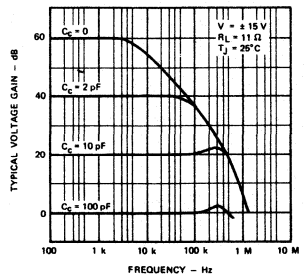
12

TYPICAL PERFORMANCE CURVES FOR μA791 and μA791C (Cont'd)

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

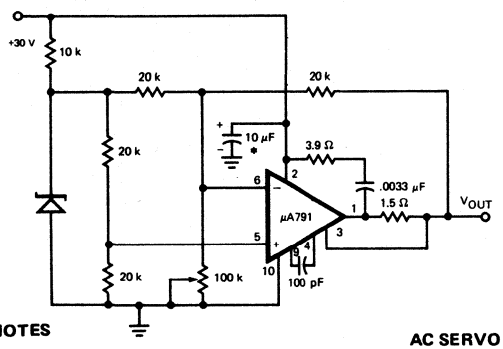


CLOSED LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



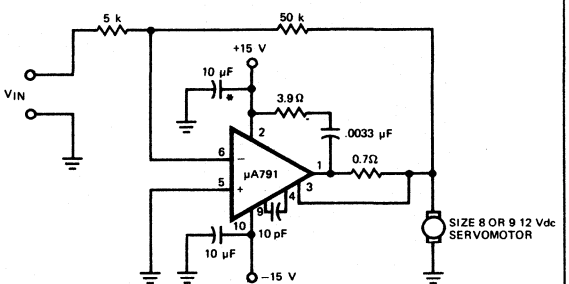
TYPICAL APPLICATIONS

POSITIVE VOLTAGE REGULATOR

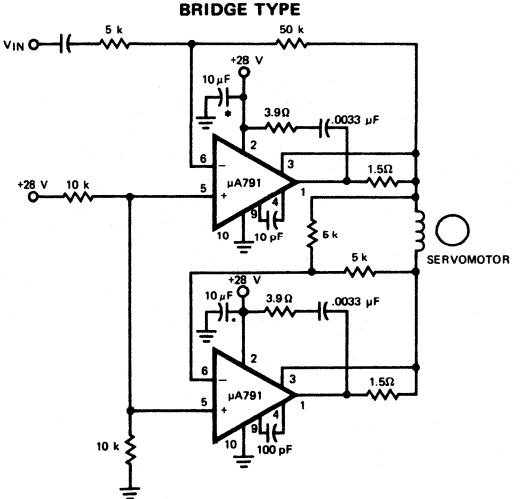


NOTES
3.0 V to 27 V regulator
500 mA output current

DC SERVO AMPLIFIER



AC SERVO AMPLIFIER BRIDGE TYPE



*Solid tantalum recommended.

μA798
DUAL OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

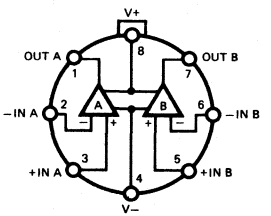
GENERAL DESCRIPTION – The μA798 is a monolithic pair of independent, high gain, internally frequency compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components ni many applications. The output voltage range also includes the negative power supply voltage. They are constructed using the Fairchild Planar* epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING TO GROUND OR NEGATIVE SUPPLY**
- **INTERNALLY COMPENSATED**
- **WIDE POWER SUPPLY RANGE: SINGLE SUPPLY OF 3.0 TO 36 V**
  DUAL SUPPLY OF ±1.5 TO ±18 V
- **CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION**
- **SHORT CIRCUIT PROTECTED OUTPUT**
- **HIGH OPEN LOOP GAIN – 200 k**
- **EXCEEDS 1458 TYPE PERFORMANCE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V–	36 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (V–) (Note 1)	–0.3 V (V–) to V+
Internal Power Dissipation (Note 2)	
Metal Can, Hermetic Mini DIP	500 mW
Molded Mini DIP	310 mW
Operating Temperature Range	
Commercial (C)	0°C to +70°C
Military (M)	–55°C to +125°C
Storage Temperature Range	
Molded Package (9T)	–55°C to +125°C
Hermetic Package (5S, 6T)	–65°C to +150°C
Lead Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C
Output Short Circuit Duration	Note 5

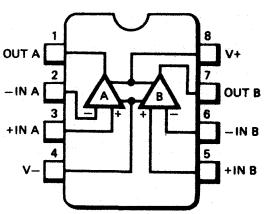
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μ798	μA798HM
μ798C	μA798HC

8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 6T 9T
PACKAGE CODE R T



ORDER INFORMATION

TYPE	PART NO.
μA798	μA798RM
μA798C	μA798RC
μA798C	μA798TC

*Planar is a patented Fairchild process.

12

μA798

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			10	25	nA
Input Bias Current			–50	–100	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 2kΩ	50	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = –10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		20		%
Phase Margin	A_V = 1, R_L = 2k Ω, C_L = 200 pF		60		Degree
Crossover Distortion at f = 10 kHz	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk		1.0		%
Output Voltage Range	R_L = 10k Ω	±13	±14		V
	R_L = 2 kΩ	±12	±13.5		V
Individual Output Short Circuit Current	(Note 3)	±20	±30		mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		2.0	3.0	mA
The following specification apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage				6.0	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				–300	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	25	300		V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS (V_S = +5 V and Ground, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			30	100	nA
Input Bias Current			–200	–500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 4)	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, 5.0 V $\leq V_S \leq$ 30 V	(V+)–1.5			V pk-pk
Output Sink Current	$V_{IN} \leq$ –10 mV, V_{OUT} = 400 mV	1.0			mA
Power Supply Current			2.0	3.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		–120		dB

NOTES:

1. For supply voltage less than 30 V between V+ and V–, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly 6.3 mW/°C for the Metal Can (5S) and Hermetic Mini DIP (6T), 5.6 mW/°C for the Molded Mini DIP (9T).
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.
5. Indefinite on shorts to ground or V– supply. Shorts to V+ supply may result in power dissipation exceeding the absolute maximum rating.

μA798C

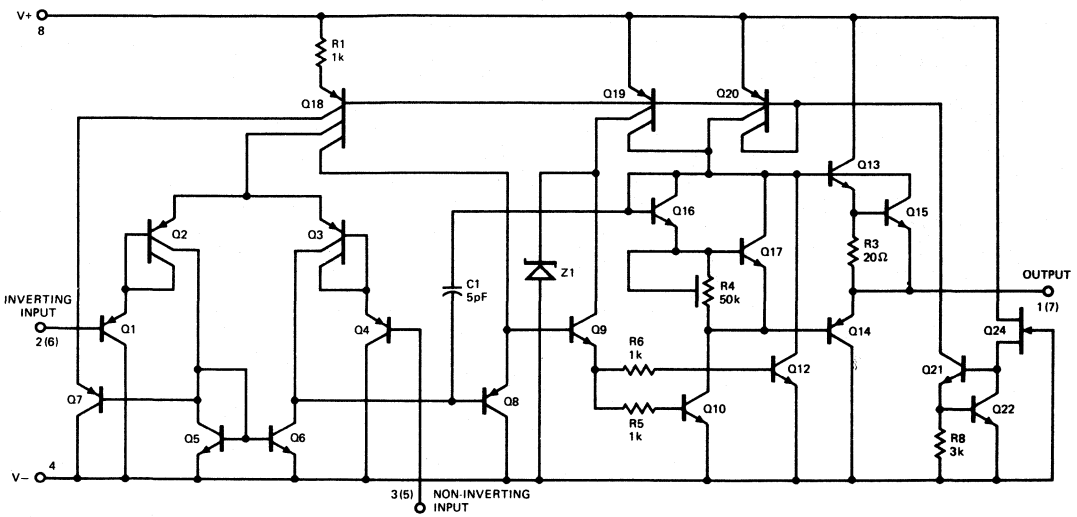
ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	6.0	mV
Input Offset Current			10	75	nA
Input Bias Current			–50	–250	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Range	V_{OUT} = ±10 V, R_L = 2 kΩ	20	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk THD = 5%		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = –10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		20		%
Phase Margin	A_V = 1, R_L = 2 kΩ, C_L = 200 pF		60		Degree
Crossover Distortion	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk f = 10 kHz		1.0		%
Output Voltage Range	R_L = 10 kΩ	±13	±14		V
	R_L = 2 kΩ	±12	±13.5		V
Individual Output Short Circuit Current	(Note 3)	±10	±30		mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		2.0	4.0	mA
The following specification apply for 0°C ≤ T_A ≤ 70°C					
Input Offset Voltage				7.5	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				–400	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	15			V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS (V_S = +5.0 V and Ground, T_A = 25°C unless otherwise noted)

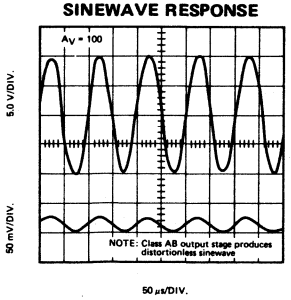
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	10	mV
Input Offset Current			30	100	nA
Input Bias Current			–200	–500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, 5.0 V ≤ V_S ≤ 30 V	(V+)–1.5			V pk-pk
Output Sink Current	$V_{IN} \leq -10$ mV, V_{OUT} = 400 mW	1.0			mA
Power Supply Current			2.0	4.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		–120		dB

1/2 OF EQUIVALENT CIRCUIT

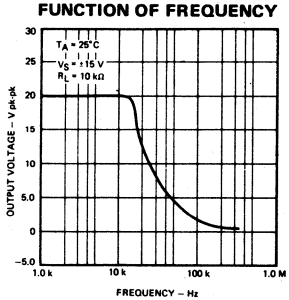


TYPICAL PERFORMANCE CURVES

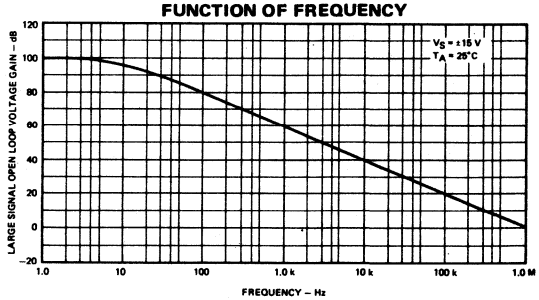
SINEWAVE RESPONSE



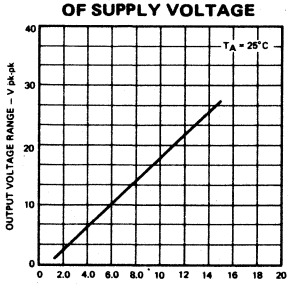
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



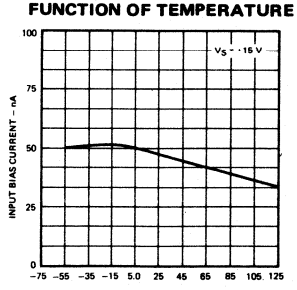
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



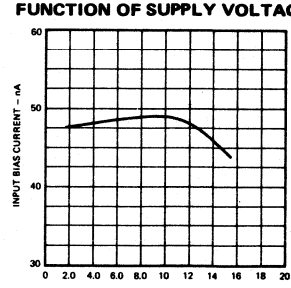
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

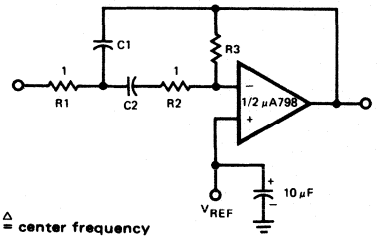


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TYPICAL APPLICATIONS

MULTIPLE FEEDBACK BANDPASS FILTER



$f_o \triangleq$ center frequency

BW $\triangleq$ Bandwidth

R in kΩ

C in μF

$Q = \frac{f_o}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$

$R3 = 9Q^2 - 1$

} Use scaling factors in these expressions.

Design example:

given: $Q = 5$, $f_o = 1$ kHz

Let $R1 = R2 = 10$ kΩ

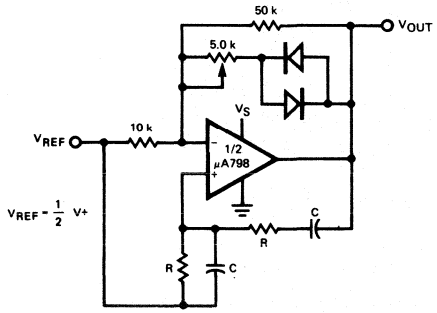
then $R3 = 9(5)^2 - 10$

$R3 = 215$ kΩ

$C = \frac{5}{3} = 1.6$ nF

If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

WEIN BRIDGE OSCILLATOR

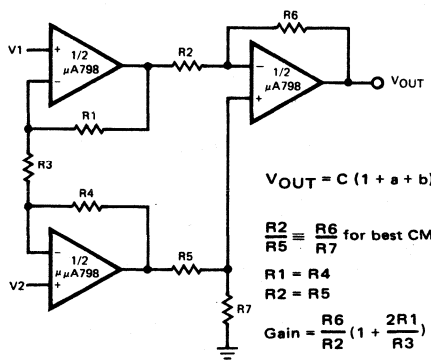


$f_o = \frac{1}{2\pi RC}$ for $f_o = 1$ kHz

$R = 16$ kΩ

$C = 0.01$ μF

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$V_{OUT} = C(1 + a + b)(V2 - V1)$

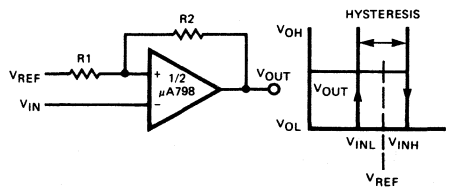
$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

$R1 = R4$

$R2 = R5$

$\text{Gain} = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right) = C(1 + a + b)$

COMPARATOR WITH HYSTERESIS

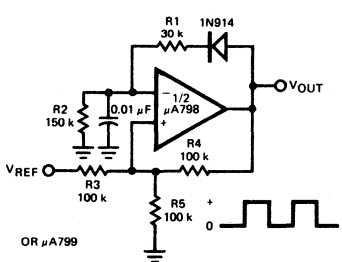


$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$

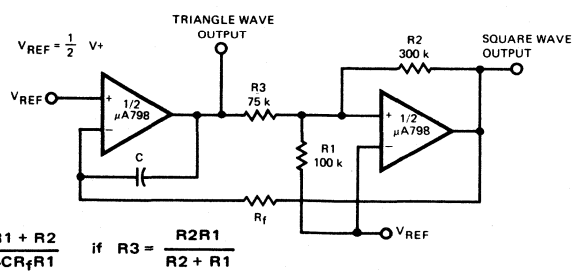
$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

PULSE GENERATOR



FUNCTION GENERATOR

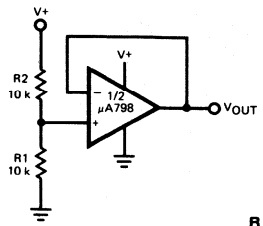


$f = \frac{R1 + R2}{4CR_fR1}$ if $R3 = \frac{R2R1}{R2 + R1}$

12

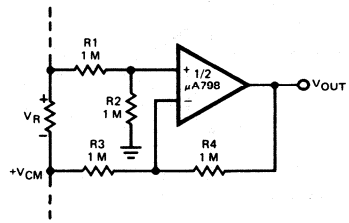
TYPICAL APPLICATIONS (Cont'd)

VOLTAGE REFERENCE



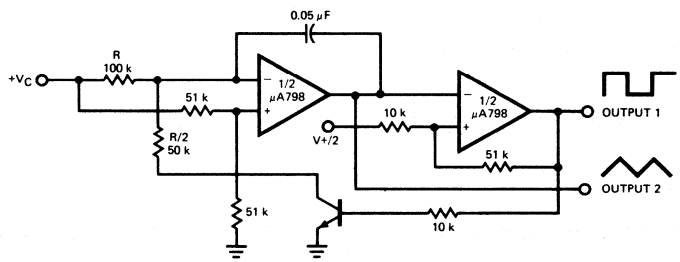
$$V_{OUT} = \frac{R1}{R1 - R2} = \frac{V+}{2}$$

GROUND REFERENCING A DIFFERENTIAL INPUT SIGNAL



$$V_{OUT} = V_R$$

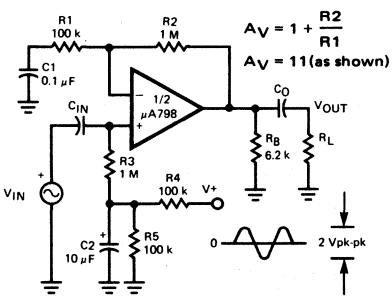
VOLTAGE CONTROLLED OSCILLATOR



*Wide Control Voltage Range:

$$0V_{DC} \leq V_C \leq 2(V+ - 1.5V_{DC})$$

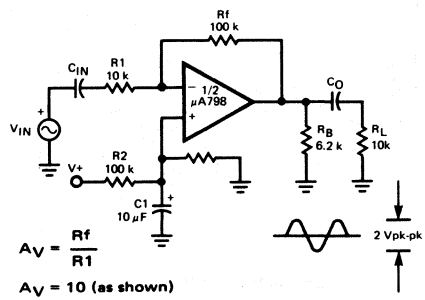
AC COUPLED NON-INVERTING AMPLIFIER



$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (as shown)

AC COUPLED INVERTING AMPLIFIER



$$A_V = \frac{Rf}{R1}$$

A_V = 10 (as shown)

μA799
OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

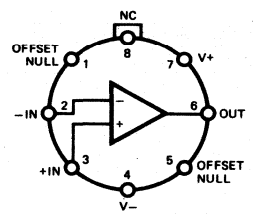
GENERAL DESCRIPTION – The μA799 is a monolithic Operational Amplifier consisting of a high gain, internally frequency compensated operational amplifier designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. It is constructed using the Fairchild Planar* epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING TO GROUND OR NEGATIVE SUPPLY**
- **INTERNALLY COMPENSATED**
- **WIDE POWER SUPPLY RANGE: SINGLE SUPPLY OF 3.0 TO 36 V**
  DUAL SUPPLY OF ±1.5 TO ±18 V
- **CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION**
- **SHORT CIRCUIT PROTECTED OUTPUTS**
- **HIGH OPEN LOOP GAIN – 200 k**
- **EXCEEDS μA741 TYPE PERFORMANCE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V–	36 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (V–) (Note 1)	–0.3 V(V–) to V+
Internal Power Dissipation (Note 2)	
Metal Can, Hermetic Mini DIP	500 mW
Molded Mini DIP	310 mW
Operating Temperature Range	
μA799C	0°C to +70°C
μA799	–55°C to +125°C
Storage Temperature Range	
Molded Package (9T)	–55°C to +125°C
Hermetic Package (5S, 6T)	–65°C to +150°C
Lead Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C
Output Short-Circuit Duration	Note 5

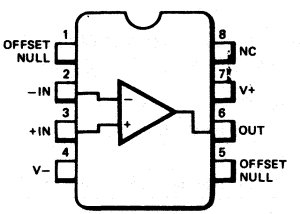
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA799	μA799HM
μA799C	μA799HC

8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 6T
PACKAGE CODE R



ORDER INFORMATION

TYPE	PART NO.
μA799C	μA741TC
μA799C	μA741RC
μA799	μA741RM

*Planar is a patented Fairchild process.

12

μA799

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			10	25	nA
Input Bias Current			−50	−100	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 2kΩ	50	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = −10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		20		%
Phase Margin	A_V = 1, R_L = 2k Ω, C_L = 200 pF		60		Degree
Crossover Distortion at f = 10 kHz	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk		1.0		%
Output Voltage Range	R_L = 10k Ω	±13	±14		V
	R_L = 2 kΩ	±12	±13.5		V
Individual Output Short Circuit Current	(Note 3)	±20	±30		mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		1.0	4.0	mA
The following specification apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage				6.0	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−300	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	25	300		V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS (V_S = +5 V and Ground, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			30	100	nA
Input Bias Current			−200	−500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 4)	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, 5.0 V ≤ V_S ≤ 30 V	(V+)−1.5			V pk-pk
Output Sink Current	$V_{IN} \leq -10$ mV, V_{OUT} = 400 mV	1.0			mA
Power Supply Current			1.0	3.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB

NOTES:

1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly 6.3 mW/°C for the Metal Can (5S) and Hermetic Mini DIP (6T), 5.6 mW/°C for the Molded Mini DIP (9T).
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.
5. Indefinite on shorts to ground or V− supply. Shorts to V+ supply may result in power dissipation exceeding the absolute maximum rating.

μA799C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise noted)

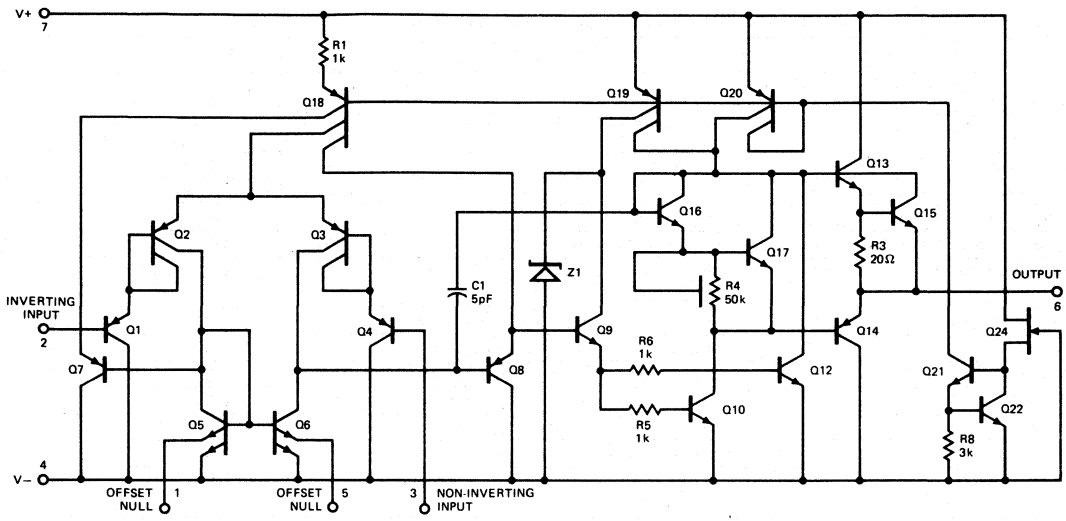
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	6.0	mV
Input Offset Current			10	75	nA
Input Bias Current			–50	–250	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Range	V_{OUT} = ±10 V, R_L = 2 kΩ	20	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk THD = 5%		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = –10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		20		%
Phase Margin	A_V = 1, R_L = 2 kΩ, C_L = 200 pF		60		Degree
Crossover Distortion	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk f = 10 kHz		1.0		%
Output Voltage Range	R_L = 10 kΩ	±13	±14		V
	R_L = 2 kΩ	±12	±13.5		V
Individual Output Short Circuit Current	(Note 3)	±10	±30		mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		1.0	4.0	mA
The following specification apply for 0°C ≤ T_A ≤ 70°C					
Input Offset Voltage				7.5	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				–400	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	15			V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS (V_S = +5.0 V and Ground, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	10	mV
Input Offset Current			30	100	nA
Input Bias Current			–200	–500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, 5.0 V ≤ V_S ≤ 30 V	(V+)–1.5			V pk-pk
Output Sink Current	$V_{IN} \leq -10$ mV, V_{OUT} = 400 mV	1.0			mA
Power Supply Current			1.0	4.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		–120		dB

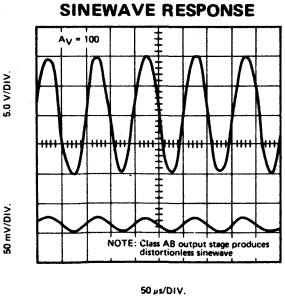
12

EQUIVALENT CIRCUIT

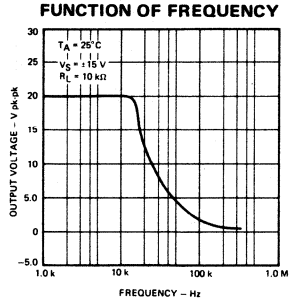


TYPICAL PERFORMANCE CURVES

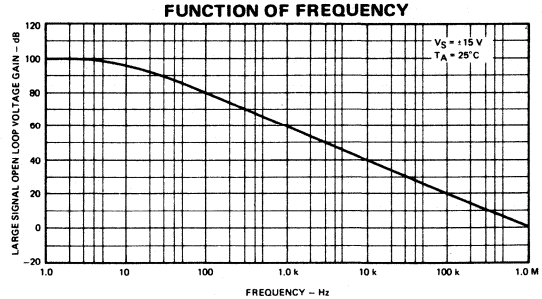
SINEWAVE RESPONSE



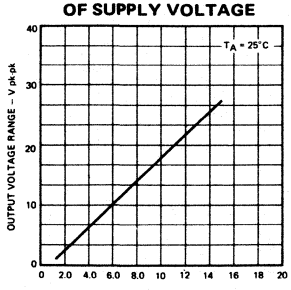
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



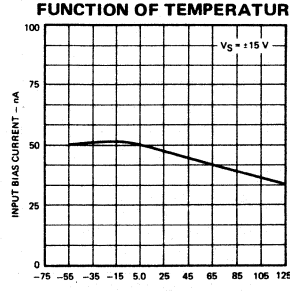
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



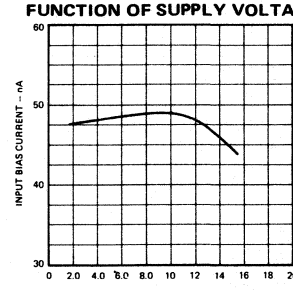
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

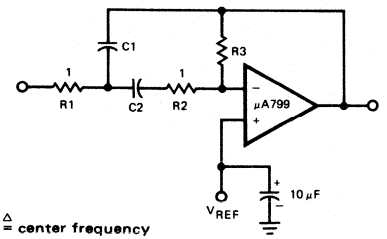


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TYPICAL APPLICATIONS

MULTIPLE FEEDBACK BANDPASS FILTER



$f_o \triangleq$ center frequency

BW $\triangleq$ Bandwidth

R in kΩ

C in μF

$Q = \frac{f_o}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$

$R3 = 9Q^2 - 1$

} Use scaling factors in these expressions.

Design example:

given: $Q = 5$, $f_o = 1$ kHz

Let $R1 = R2 = 10$ kΩ

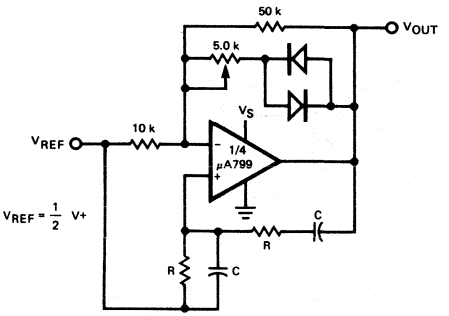
then $R3 = 9(5)^2 - 10$

$R3 = 215$ kΩ

$C = \frac{5}{3} = 1.6$ nF

If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

WEIN BRIDGE OSCILLATOR

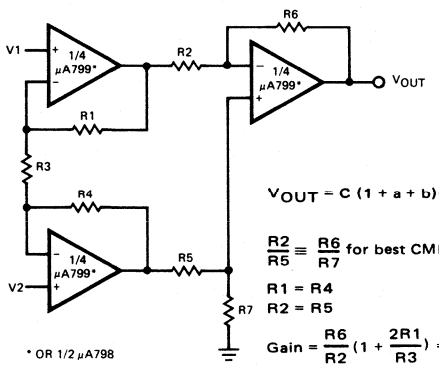


$f_o = \frac{1}{2\pi RC}$ for $f_o = 1$ kHz

$R = 16$ kΩ

$C = 0.01$ μF

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$V_{OUT} = C(1 + a + b)(V2 - V1)$

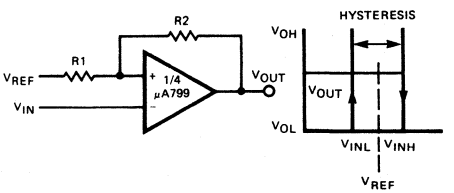
$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

$R1 = R4$

$R2 = R5$

$\text{Gain} = \frac{R6}{R2}(1 + \frac{2R1}{R3}) = C(1 + a + b)$

COMPARATOR WITH HYSTERESIS

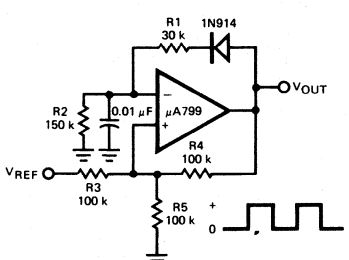


$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$

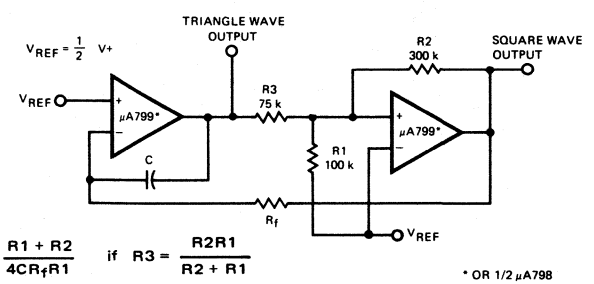
$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

PULSE GENERATOR



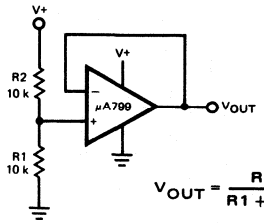
FUNCTION GENERATOR



$f = \frac{R1 + R2}{4CR_fR1}$ if $R3 = \frac{R2R1}{R2 + R1}$

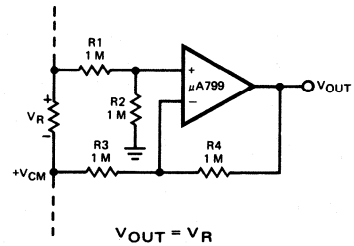
TYPICAL APPLICATIONS (Cont'd)

VOLTAGE REFERENCE



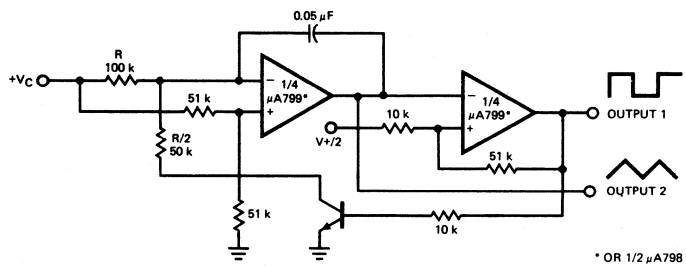
$$V_{OUT} = \frac{R1}{R1 + R2} = \frac{V+}{2}$$

GROUND REFERENCING A DIFFERENTIAL INPUT SIGNAL



$$V_{OUT} = V_R$$

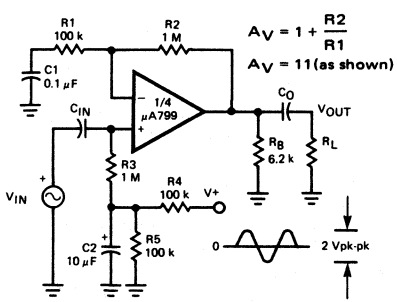
VOLTAGE CONTROLLED OSCILLATOR



*Wide Control Voltage Range:

$$0V_{DC} \leq V_C \leq 2(V+ - 1.5V_{DC})$$

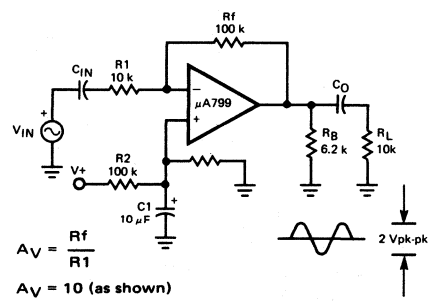
AC COUPLED NON-INVERTING AMPLIFIER



$$A_V = 1 + \frac{R2}{R1}$$

$A_V = 11$ (as shown)

AC COUPLED INVERTING AMPLIFIER



$$A_V = \frac{Rf}{R1}$$

$A_V = 10$ (as shown)

μA1558 • μA1458 • μA1458C

INTERNALLY COMPENSATED, HIGH PERFORMANCE DUAL MONOLITHIC OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 1558 / 1458 are a monolithic pair of Internally Compensated High Performance Amplifiers constructed using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the 1558 / 1458 ideal for use as voltage followers. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

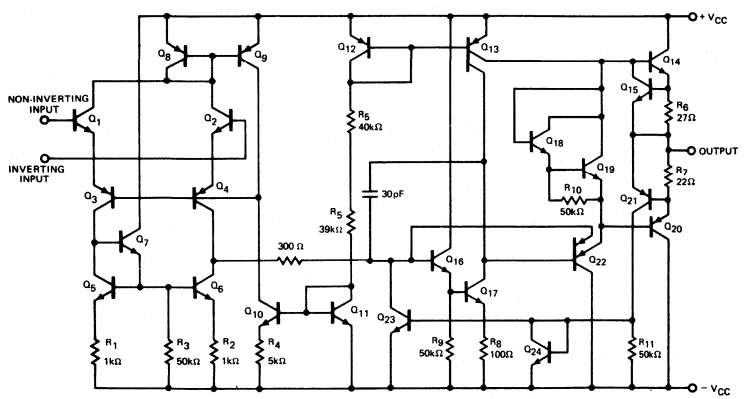
The 1558 / 1458 are short-circuit protected and require no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see the μA741 data sheet.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**
- **MINI DIP PACKAGE**

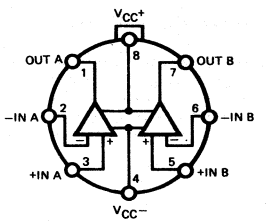
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military (μA1558)	±22 V
Commercial (μA1458 and μA1458C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	800 mW
Mini DIP	560 mW
Differential Input Voltage (Note 2)	±30 V
Common-Mode Input Swing (Note 2)	±15 V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (μA1558)	−55°C to +125°C
Commercial (μA1458 and μA1458C)	0°C to 70°C
Lead Temperature	
Metal Can (Soldering, 60 s)	300°C
Mini DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT
(EACH SIDE)



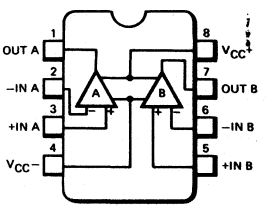
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA1558	μA1558HC
μA1458	μA1458HC
μA1458C	μA1458CHC

8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
μA1458	μA1458TC
μA1458C	μA1458CTC
μA1458	μA1458RI
μA1458C	μA1458CRC

Notes on following page.

*Planar is a patented Fairchild process.

μA1558

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current			0.03	0.2	μA
Input Bias Current			0.2	0.5	μA
Differential Input Impedance					
Parallel Input Resistance	f = 20Hz, Open Loop	0.3	1.0		MΩ
Parallel Input Capacitance			6.0		pF
Common-Mode Input Impedance	f = 20Hz		200		MΩ
Common-Mode Input Voltage Swing		±12	±13		V
Equivalent Input Noise Voltage	A_V = 100, R_S = 10kΩ, f = 1.0kHz, BW = 1.0Hz		45		nV/√Hz
Common-Mode Rejection Ratio	f = 100Hz	70	90		dB
Open-Loop Voltage Gain	V_{OUT} = ±10V, R_L = 2.0kΩ	50k	200k		V/V
Power Bandwidth	A_V = 1, R_L = 2.0kΩ, THD ≤ 5%, $V_{OUT} = 20V_{p-p}$		14		kHz
Unity Gain Crossover Frequency (Open Loop)			1.1		MHz
Phase Margin (Open Loop)			65		Degrees
Gain Margin			11		dB
Slew Rate	A_V = 1		0.8		V/μs
Output Impedance	f = 20Hz		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	R_L = 10kΩ	±12	±14		V
Power Supply Sensitivity					
V_{CC}− = Constant	$R_S \leq 10k\Omega$		30	150	μV/V
V_{CC}+ = Constant			30	150	μV/V
Power Supply Current	I_+		2.3	5.0	mA
	I_-		2.3	5.0	mA
Power Dissipation	V_{OUT} = 0		70	150	mW

The Following Specifications Apply For $-55°C \leq T_A \leq +125°C$

Input Offset Voltage	$R_S \leq 10k\Omega$			6.0	mV
Input Offset Current				0.5	μA
Input Bias Current				1.5	μA
Open-Loop Voltage Gain	V_{OUT} = ±10V, R_L = 2.0kΩ	25k			V/V
Output Voltage Swing	R_L = 2kΩ	±10	±13		V
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω		15		μV/°C

NOTES:
1. Rating applies to ambient temperatures up to 25°C. Above 25°C ambient derate linearly at 6.3 mW/°C for the metal can and 5.6 mW/°C for the mini DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 70°C ambient temperature.

μA1458

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
Input Offset Current			.03	0.2	μA
Input Bias Current			0.2	0.5	μA
Differential Input Impedance					
Parallel Input Resistance	f = 20Hz, Open Loop	0.3	1.0		MΩ
Parallel Input Capacitance			6.0		pF
Common-Mode Input Impedance	f = 20Hz		200		MΩ
Common-Mode Input Voltage Swing		±12	±13		V
Equivalent Input Noise Voltage	A_V = 100, R_S = 10kΩ, f = 1.0kHz, BW = 1.0Hz		45		nV/√Hz
Common-Mode Rejection Ratio	f = 100Hz	70	90		dB
Open-Loop Voltage Gain	V_{OUT} = ±10V, R_L = 2.0kΩ	20k	100k		V/V
Power Bandwidth	A_V = 1, R_L = 2.0kΩ, THD ≤ 5%, $V_{OUT} = 20V_{p-p}$		14		kHz
Unity Gain Crossover Frequency (Open-Loop)			1.1		MHz
Phase Margin (Open Loop)			65		Degrees
Gain Margin			11		dB
Slew Rate	A_V = 1		0.8		V/μs
Output Impedance	f = 20Hz		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	R_L = 10kΩ	±12	±14		V
Power Supply Sensitivity					
$V_{CC}-$ = Constant	$R_S \leq 10k\Omega$		30	150	μV/V
$V_{CC}+$ = Constant			30	150	μV/V
Power Supply Current	I_+		2.3	5.6	mA
	I_-		2.3	5.6	mA
Power Dissipation	V_{OUT} = 0		70	170	mW
The Following Specifications Apply For 0°C ≤ T_A ≤ 70°C					
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5	mV
Input Offset Current				0.3	μA
Input Bias Current				0.8	μA
Open Loop Voltage Gain	V_{OUT} = ±10V, R_L = 2.0kΩ	15k			V/V
Output Voltage Swing	R_L = 2.0kΩ	±10	±13		V
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω		15		μV/°C

μA1458C

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	10	mV
Input Offset Current			.03	0.3	μA
Input Bias Current			0.2	0.7	μA
Differential Input Impedance					
Parallel Input Resistance	f = 20Hz, Open Loop		1.0		MΩ
Parallel Input Capacitance			6.0		pF
Common-Mode Input Impedance	f = 20Hz		200		MΩ
Common-Mode Input Voltage Swing		±11	±13		V
Equivalent Input Noise Voltage	A_V = 100, R_S = 10kΩ, f = 1.0kHz, BW = 1.0Hz		45		nV/√Hz
Common-Mode Rejection Ratio	f = 100Hz	60	90		dB
Open-Loop Voltage Gain	V_{OUT} = ±10V, R_L = 10kΩ	20k	100k		V/V
Power Bandwidth	A_V = 1, R_L = 2.0kΩ, THD ≤ 5%, $V_{OUT} = 20V_{p-p}$		14		kHz
Unity Gain Crossover Frequency (Open-Loop)			1.1		MHz
Phase Margin (Open Loop)			65		Degrees
Gain Margin			11		dB
Slew Rate	A_V = 1		0.8		V/μs
Output Impedance	f = 20Hz		75		Ω
Short-Circuit Output Current			20		mA
Output Voltage Swing	R_L = 10kΩ	±11	±14		V
Power Supply Sensitivity					
$V_{CC}-$ = Constant	$R_S \leq 10k\Omega$		30		μV/V
$V_{CC}+$ = Constant			30		μV/V
Power Supply Current	I_+		2.3	8.0	mA
	I_-		2.3	8.0	mA
Power Dissipation	V_{OUT} = 0		70	240	mW

The Following Specifications Apply For 0°C ≤ T_A ≤ +70°C

Input Offset Voltage	$R_S \leq 10k\Omega$			12	mV
Input Offset Current				0.4	μA
Input Bias Current				1.0	μA
Open Loop Voltage Gain	V_{OUT} = ±10V, R_L = 10kΩ	15k			V/V
Output Voltage Swing	R_L = 2.0kΩ	±9.0	±13		V
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω		15		μV/°C

TYPICAL PERFORMANCE CURVES FOR μA1558, μA1458 AND μA1458C

(V_{CC} = +15 V, V_{CC-} = −15 V, T_A = 25°C unless otherwise noted)

OPEN-LOOP VOLTAGE GAIN AS A FUNCTION OF POWER SUPPLY VOLTAGES

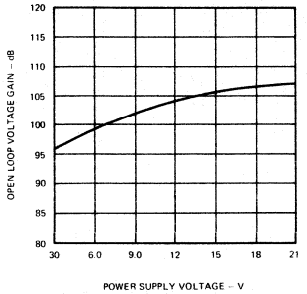


Fig. 1

OPEN-LOOP FREQUENCY RESPONSE

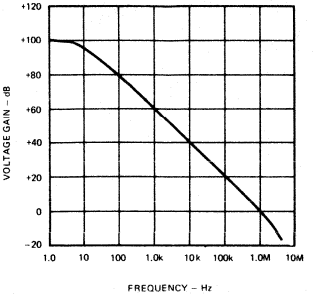


Fig. 2

POWER BANDWIDTH (LARGE SIGNAL SWING AS A FUNCTION OF FREQUENCY)

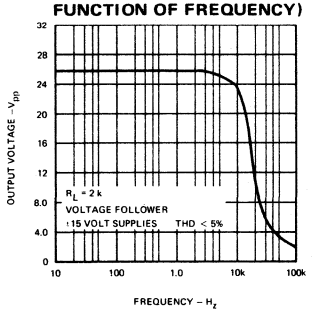


Fig. 3

POWER DISSIPATION AS A FUNCTION OF POWER SUPPLY VOLTAGE

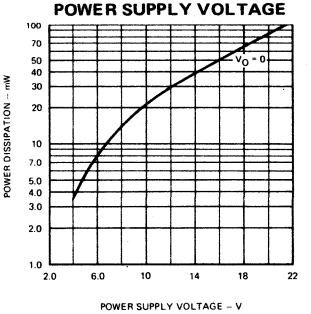


Fig. 4

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

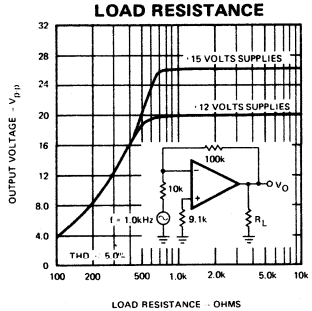


Fig. 5

OUTPUT NOISE AS A FUNCTION OF SOURCE RESISTANCE

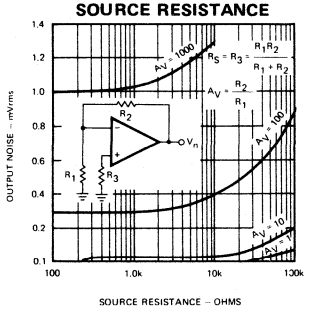


Fig. 6

12

HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER

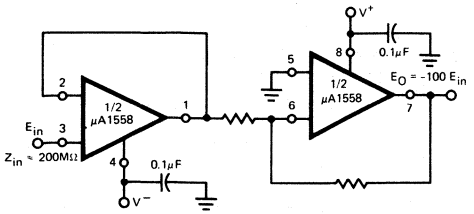
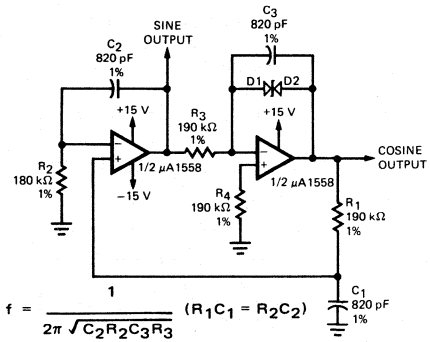


Fig. 7

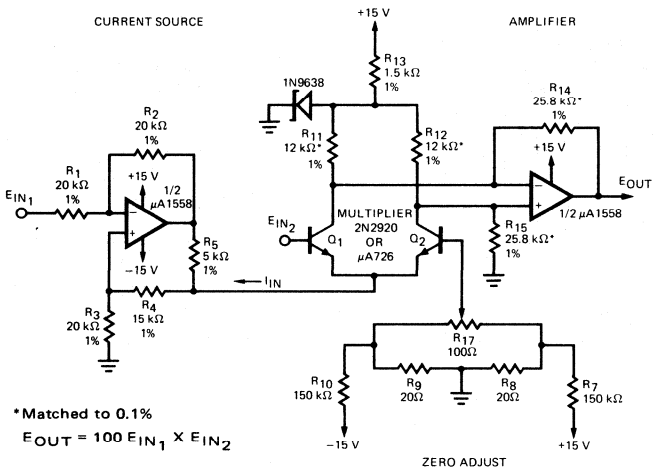
QUADRATURE OSCILLATOR



$$f = \frac{1}{2\pi\sqrt{C_2R_2C_3R_3}} \quad (R_1C_1 = R_2C_2)$$

Fig. 8

ANALOG MULTIPLIER

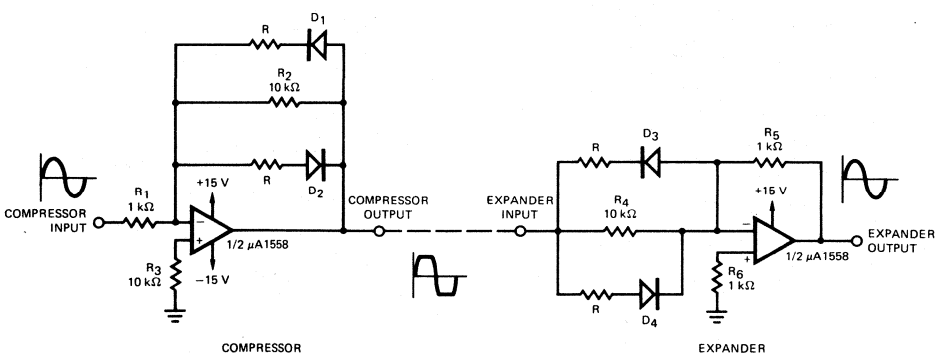


*Matched to 0.1%

$E_{OUT} = 100\ E_{IN_1} \times E_{IN_2}$

Fig. 9

COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION EXPANSION RATIO = R_1/R $(10\ k\Omega > R \geq 0)$

NOTE: DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT.

Fig.10

μA3301 • μA3401

QUAD SINGLE SUPPLY AMPLIFIERS

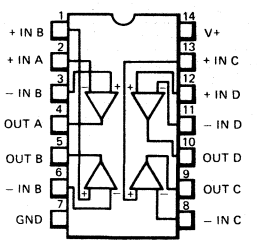
FAIRCHILD INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 3301/3401 are monolithic Quad Amplifiers consisting of four independent, dual input, internally compensated amplifiers. They are constructed using the Fairchild Planar* epitaxial process. They were designed specifically to operate from a single power supply voltage and to provide a large output voltage swing. The non-inverting input function is achieved by using a current mirror. Applications for the 3301/3401 are ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

- **SINGLE SUPPLY OPERATION – +4.0 Vdc to +28 Vdc**
- **INTERNALLY COMPENSATED**
- **WIDE UNITY GAIN BANDWIDTH – 5.0 MHz**
- **LOW INPUT BIAS CURRENT – 50 nA TYPICAL**
- **HIGH OPEN LOOP GAIN – 1000 V/V MINIMUM**

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)

PACKAGE OUTLINE 9A
PACKAGE CODE P



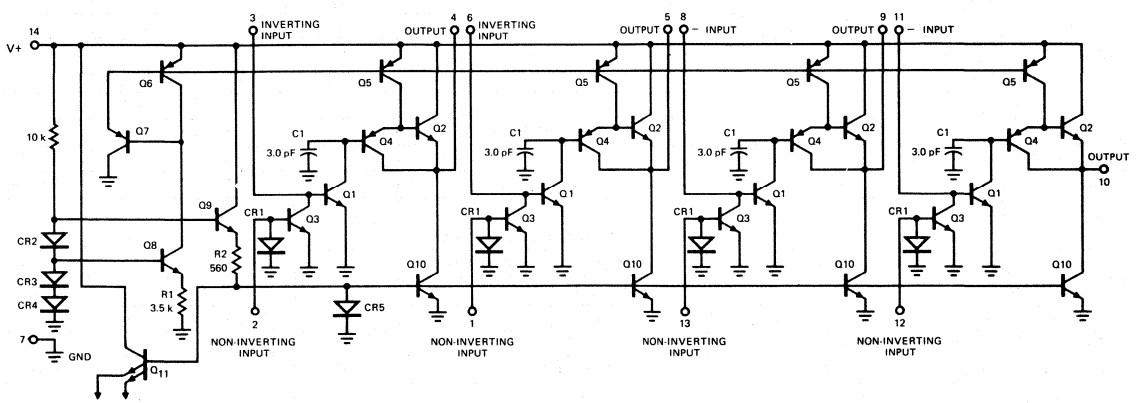
ORDER INFORMATION

TYPE	PART NO.
μA3301	μA3301P
μA3401	μA3401P

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA3301	+28 V
μA3401	+18 V
Non-Inverting Input Current	5.0 mA
Sink Current	50 mA
Source Current	50 mA
Internal Power Dissipation (Note 1)	670 mW
Operating Temperature Range	
μA3301	–40°C to +85°C
μA3401	0°C to +70°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (soldering 10 s)	260°C

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA3301

ELECTRICAL CHARACTERISTICS – V_S = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C, each amplifier, unless otherwise noted.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Open Loop Voltage Gain (Note 2)	Inverting Input	1000	2000		V/V
Input Bias Current (Note 3)	R_L = ∞, Inverting Input		50	300	nA
Input Resistance		0.1	1.0		MΩ
Current Mirror Gain (Note 4)	(I_{Mirror} = 200 μAdc)	0.80	0.98	1.16	A/A
Output Current					
Source	V_{OH} = 0.4 Vdc	3.0	10		mA
	V_{OH} = 9.0 Vdc		7.0		mA
Sink (Note 5)	V_{OL} = 0.4 Vdc	0.5	0.87		mA
Output Voltage (Note 6)					
HIGH		13.5	14.2		V
LOW			0.03	0.1	V
Slew Rate	C_L = 100 pF, R_L = 5.0 kΩ		0.6		V/μs
Unity Gain Bandwidth (Note 7)			5.0		MHz
Phase Margin (Note 7)			70		Degrees
Quiescent Power Supply Current (Note 8)					
Non-Inverting Inputs Open	Total for Four Amplifiers		6.9	10	mA
Non-Inverting Inputs Grounded	Total for Four Amplifiers		7.8	14	mA
Power Supply Rejection (Note 9)	(f = 100 Hz)		75		dB
Channel Separation	(f = 1.0 kHz)		85		dB
The following specifications apply for −40°C ≤ T_A ≤ +85°C.					
Open Loop Voltage Gain (R_L = 10 kΩ)	Inverting Input		1600		V/V
Input Bias Current	R_L = ∞			500	nA
Output Voltage (Note 10) Undistorted Output Swing		10	13.5		V_{pk-pk}

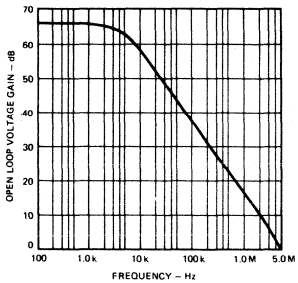
μA3401

ELECTRICAL CHARACTERISTICS – V_S = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C, each amplifier, unless otherwise noted.

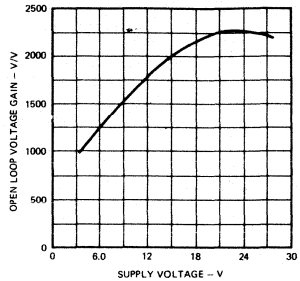
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Open Loop Voltage Gain (Note 2)	Inverting Input	1000	2000		V/V
Input Bias Current (Note 3)	R_L = ∞, Inverting Input		50	300	nA
Input Resistance		0.1	1.0		MΩ
Output Current					
Source		5.0	10		mA
Sink (Note 5)		0.5	1.0		mA
Output Voltage (Note 6)					
HIGH		13.5	14.2		V
LOW			0.03	0.1	V
Slew Rate	C_L = 100 pF, R_L = 5.0 kΩ		0.6		V/μs
Unity Gain Bandwidth (Note 7)			5.0		MHz
Phase Margin (Note 7)			70		Degrees
Quiescent Power Supply Current (Note 8)					
Non-Inverting Inputs Open	Total for Four Amplifiers		6.9	10	mA
Non-Inverting Inputs Grounded	Total for Four Amplifiers		7.8	14	mA
Power Supply Rejection (Note 9)	(f = 100 Hz)		75		dB
Channel Separation	(f = 1.0 kHz)		85		dB
The following specifications apply for 0°C ≤ T_A ≤ 70°C.					
Open Loop Voltage Gain (R_L = 10 kΩ)	Inverting Input	800			V/V
Input Bias Current	R_L = ∞			500	nA
Output Voltage (Note 10) Undistorted Output Swing		10	13.5		V_{pk-pk}

TYPICAL PERFORMANCE CURVES

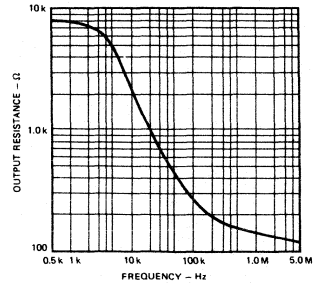
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



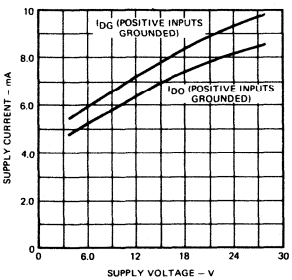
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



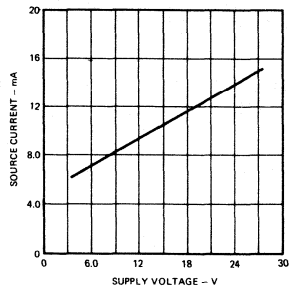
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



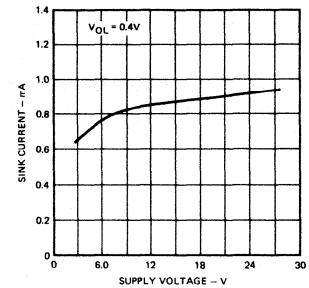
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



LINEAR SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



LINEAR SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



NOTES:

1. Rating applies to T_A up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
2. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
3. Input bias current can be defined only for the inverting input. The non-inverting input is not a true "differential input" — as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the non-inverting input.
5. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
6. When used as a non-inverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
7. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.
8. The quiescent current will increase approximately 0.3 mA for each non-inverting input which is grounded. Leaving the non-inverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
9. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.
10. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration as shown in the peak-to-peak output voltage test circuit.

TEST CIRCUITS

SMALL SIGNAL TRANSIENT RESPONSE

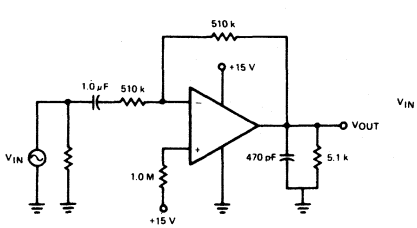
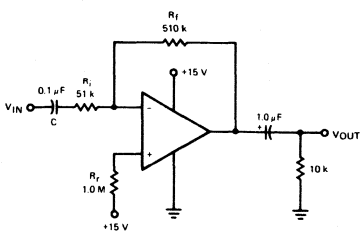


Fig. 1

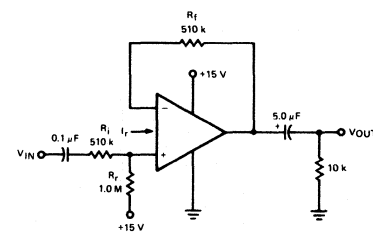
INVERTING AMPLIFIER



$$A_v = -\frac{R_f}{R_i} \text{ for } \frac{1}{\omega C} \ll R_i$$

Fig. 2

NON-INVERTING AMPLIFIER

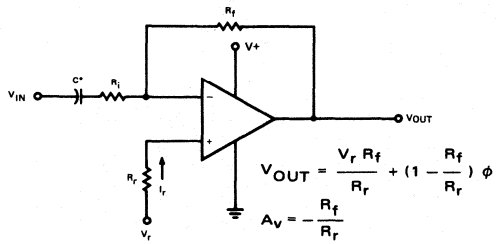


$$A_v = \frac{R_f}{R_i + \frac{26}{I_F \text{ (mA)}}} \simeq 1 \qquad \text{BW} = 250 \text{ kHz}$$

Fig. 3

TEST CIRCUITS (Cont'd)

INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



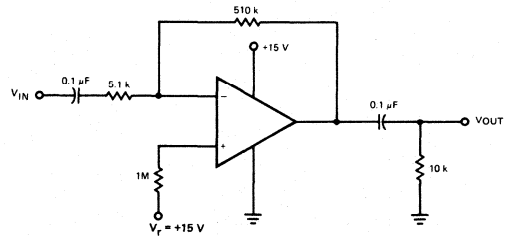
$$V_{OUT} = \frac{V_r R_f}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

$$A_V = -\frac{R_f}{R_r}$$

*Select for low frequency response.

Fig. 4

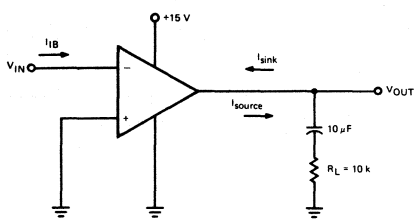
INVERTING AMPLIFIER WITH A_v = 100 AND V_r = V+



A_V = 100 f_L = 300 Hz, f_H = 50 kHz

Fig. 5

OPEN LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)

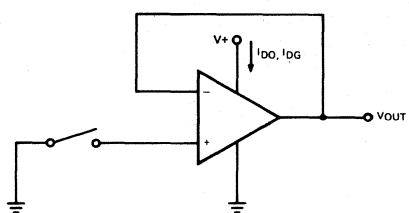


$$R_{in} = \frac{\Delta V_{IN}}{\Delta I_{IB}} \qquad A_{vol} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

Amplifier must be biased by V_{IN} in the linear operating region

Fig. 6

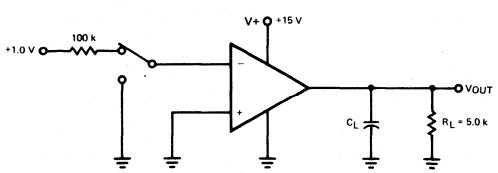
QUIESCENT POWER SUPPLY CURRENT



I_{DO} is total supply current with noninverting input open.
I_{DG} is total supply current with noninverting input grounded.

Fig. 7

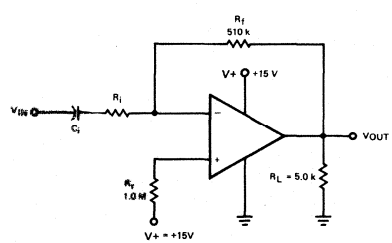
OUTPUT VOLTAGE SWING



V_{OL} measured with inverting input biased as shown.
V_{OH} measured with inverting input grounded.

Fig. 8

PEAK-TO-PEAK OUTPUT VOLTAGE



$$V_{OUT} \simeq V+ \frac{R_f}{R_r} \simeq \frac{V+}{2} \text{ for } R_r \simeq 2\,R_f$$

Fig. 9

NORMAL DESIGN PROCEDURE

Output Q-Point Biasing

A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the non-inverting input to effect the biasing as shown in Figures 2 and 3. The high impedance of the collector of the non-inverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the non-inverting input current be in the 5.0 μA to 100 μA range.

V+ Reference Voltage (Figures 2 and 3)

The non-inverting input is normally returned to the V+ voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5.0 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to 1/2 R_r will now bias the amplifier output dc level to approximately:

$$\frac{V+}{2}$$

This allows for maximum dynamic range of the output voltage.

Reference Voltage Other Than V+ (Figure 4)

The biasing resistor R_r may be returned to a voltage (V_r) other than V+. By setting $R_f = R_r$, (still keeping I_r between 5.0 μA and 100 μA) the output dc level will be equal to V_r. Neglecting error terms, the expression for determining V_{Odc} is:

$$V_{OUT} = \frac{(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 V @ +25°C).

The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5.0 μA to 100 μA.

Gain Determination — Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_v = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

Non-Inverting Amplifier

Although recommended as an inverting amplifier, the 3301/3401 may be used in the non-inverting mode (Figure 3). The amplifier gain in this configuration is subject to the same error terms that affects the output Q point biasing so the gain may deviate as much as ±20 % from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately:

$$\frac{26}{I_r}\ \Omega,$$

where I_r is input current in mA. The non-inverting gain expression is given by:

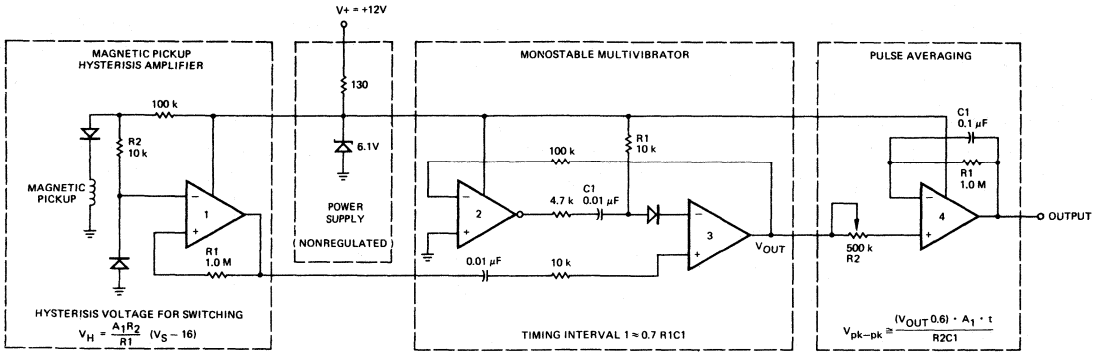
$$A_v = \frac{R_f}{R_i + \frac{26}{I_r\ (mA)}} \quad \pm 20\%.$$

The bandwidth of the non-inverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for non-inverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

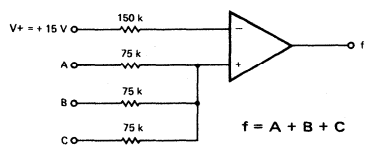
12

TYPICAL APPLICATIONS

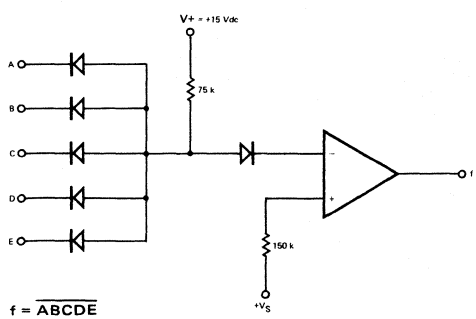
TACHOMETER CIRCUIT



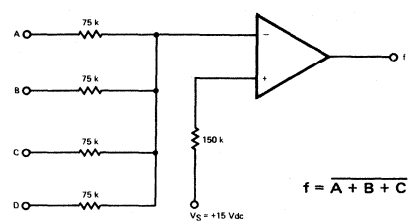
LOGIC OR GATE



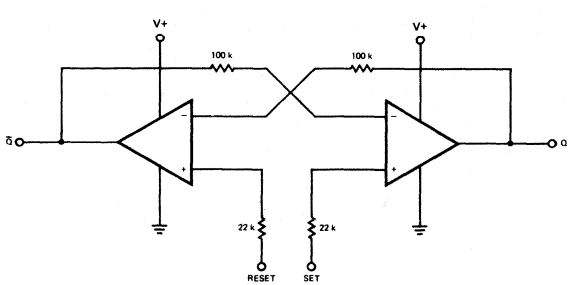
LOGIC NAND GATE (Large Fan In)



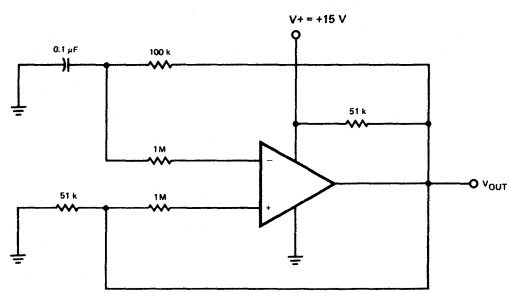
LOGIC NOR GATE



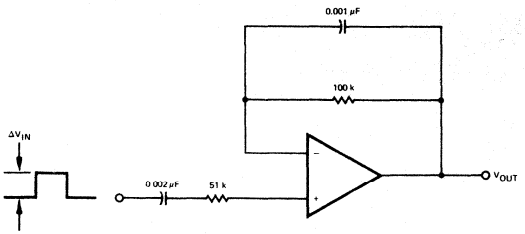
R-S FLIP-FLOP



ASTABLE MULTIVIBRATOR

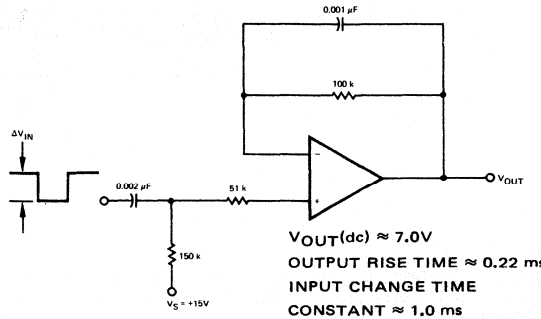


POSITIVE EDGE DIFFERENTIATOR



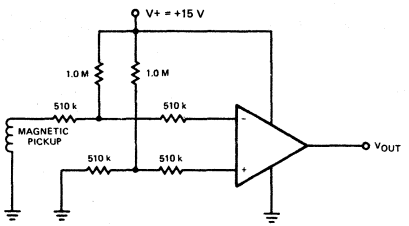
OUTPUT RISE TIME ≈ 0.22 ms
INPUT CHANGE TIME CONSTANT ≈ 1.0 ms

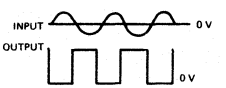
NEGATIVE EDGE DIFFERENTIATOR



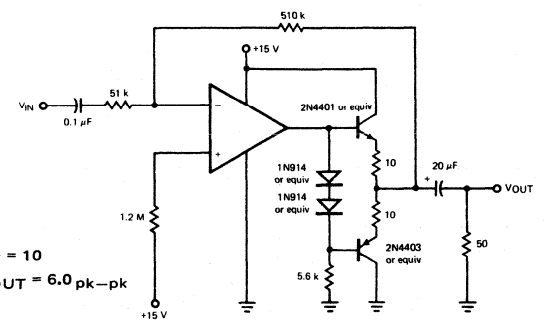
V_{OUT}(dc) ≈ 7.0V
OUTPUT RISE TIME ≈ 0.22 ms
INPUT CHANGE TIME CONSTANT ≈ 1.0 ms

ZERO CROSSING DETECTOR



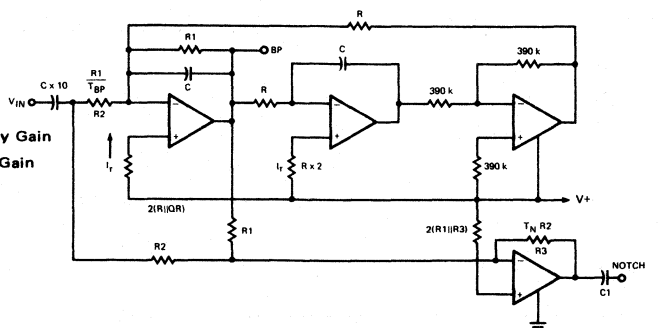


AMPLIFIER AND DRIVER FOR 50 Ω LINE



A_V = 10
V_{OUT} = 6.0 pk–pk

BASIC BANDPASS AND NOTCH FILTER



T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain
$\omega 0 = \frac{1}{RC}$
R1 = QR
$R2 = \frac{R1}{T_{BP}}$
$R3 = T_N R2$

μA3303 • μA3403 • μA3503

QUAD OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

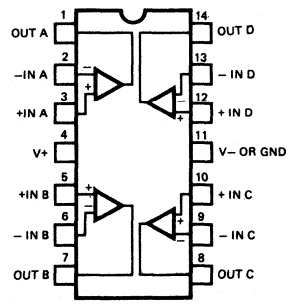
GENERAL DESCRIPTION – The 3303, 3403 and 3503 are monolithic Quad Operational Amplifiers consisting of four independent high gain, internally frequency compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. They are constructed using the Fairchild Planar* epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING TO GROUND OR NEGATIVE SUPPLY**
- **FOUR INTERNALLY COMPENSATED OPERATIONAL AMPLIFIERS IN A SINGLE PACKAGE**
- **WIDE POWER SUPPLY RANGE: SINGLE SUPPLY OF 3.0 TO 36 V**
  DUAL SUPPLY OF ±1.5 TO ±18 V
- **CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION**
- **SHORT CIRCUIT PROTECTED OUTPUTS**
- **HIGH OPEN LOOP GAIN – 200k**
- **μA741 OPERATIONAL AMPLIFIER TYPE PERFORMANCE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V–		36 V
Differential Input Voltage (Note 1)		±30 V
Input Voltage (V–) (Note 1)		–0.3 V(V–) to V+
Internal Power Dissipation (Note 2)		670 mW
Operating Temperature Range	μA3303	–40°C to +85°C
	μA3403	0°C to +70°C
	μA3503	–55°C to +125°C
Storage Temperature Range		
Molded Package		–55°C to +125°C
Hermetic Package		–65°C to +150°C
Lead Temperature		
Molded Package (Soldering, 10 s)		260°C
Hermetic Package (Soldering, 60 s)		300°C

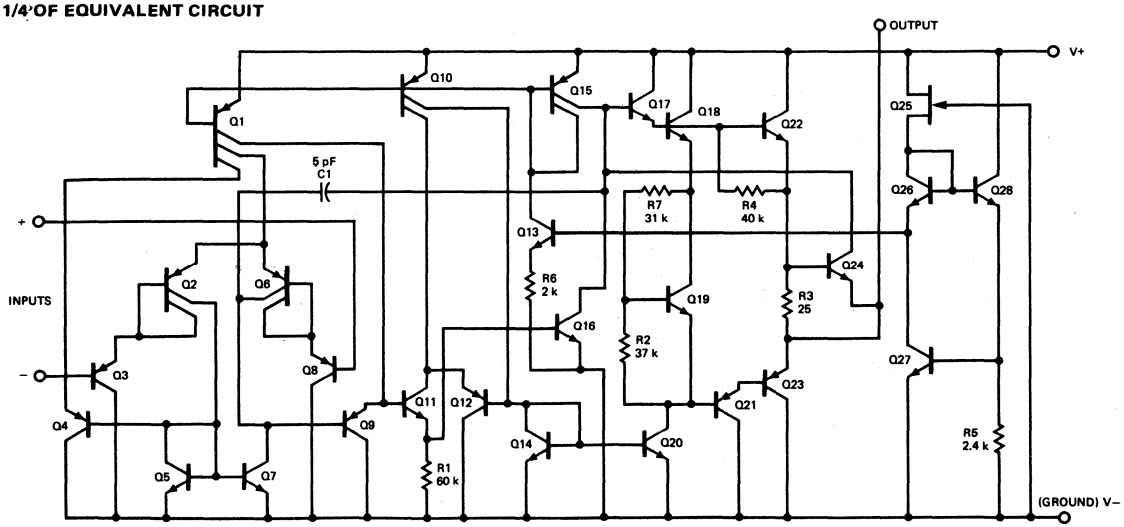
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA3403	μA3403D
μA3503	μA3503D
μA3303	μA3303P
μA3403	μA3403P

1/4 OF EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA3503

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 2kΩ	50	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = −10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		20		%
Phase Margin	A_V = 1, R_L = 2k Ω, C_L = 200 pF		60		Degree
Crossover Distortion at f = 10 kHz	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk		1.0		%
Output Voltage Range	R_L = 10k Ω	±12	±13.5		V
	R_L = 2 kΩ	±10	±13		V
Individual Output Short Circuit Current	(Note 3)	±20	±30	±45	mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		2.8	4.0	mA
The following specification apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage				6.0	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current			−300	−1500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	25	300		V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS (V_S = +5 V and Ground, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	5.0	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 4)	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, 5.0 V ≤ V_S ≤ 30 V	(V+) −1.7			V pk-pk
Power Supply Current			2.5	4.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB

NOTES:

1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.

12

μA3403

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	8.0	mV
Input Offset Current			30	50	nA
Input Bias Current			-200	-500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	V_{OUT} = ±10 V, R_L = 2 kΩ	20	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk THD = 5%		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = -10 V to +10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		20		%
Phase Margin	A_V = 1, R_L = 2 kΩ, C_L = 200 pF		60		Degree
Crossover Distortion	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk f = 10 kHz		1.0		%
Output Voltage Range	R_L = 10 kΩ	±12	±13.5		V
	R_L = 2 kΩ	±10	±13		V
Individual Output Short Circuit Current		±10	±30	±45	mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive		30	150	μV/V
	Negative		30	150	μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		2.8	7.0	mA
The following specification apply for 0°C ≤ T_A ≤ 70°C					
Input Offset Voltage				10	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				-800	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10 V	15			V/mV
Output Voltage Range	R_L = 2 kΩ	±10			V

ELECTRICAL CHARACTERISTICS (V_S = +5.0 V and Ground, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	10	mV
Input Offset Current			30	50	nA
Input Bias Current			-200	-500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range	R_L = 10 kΩ	3.5			V pk-pk
	R_L = 10 kΩ, 5.0 V ≤ V_S ≤ 30 V	(V+) -1.7			V pk-pk
Power Supply Current			2.5	7.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		-120		dB

μA3303

ELECTRICAL CHARACTERISTICS ($V+ = +14$ V, $V- = GND$, $T_A = 25°C$ unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	8.0	mV
Input Offset Current			30	75	nA
Input Bias Current			200	−500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+12 to GND	+12.5 to GND		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open-Loop Voltage Gain	$R_L = 2$ kΩ	20	200		V/mV
Power Bandwidth	$A_V = 1$, $R_L = 2$ kΩ, $V_{OUT} = 10$ V pk-pk THD = 5%		18		kHz
Small Signal Bandwidth	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		1.0		MHz
Slew Rate	$A_V = 1$		0.6		V/μs
Rise Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Fall Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Overshoot	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		20		%
Phase Margin	$A_V = 1$, $R_L = 2$ kΩ, $C_L = 200$ pF		60		Degree
Crossover Distortion	$V_{IN} = 30$ mV pk-pk, $V_{OUT} = 2$ V pk-pk f = 10 kHz		1.0		%
Output Voltage Range	$R_L = 10$ kΩ	12	12.5		V
	$R_L = 2$ kΩ	10	12		V
Individual Output Short Circuit Current		±10	±30	±45	mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio			30	150	μV/V
Power Supply Current	$V_{OUT} = 0$, $R_L = \infty$		2.8	7.0	mA
The following specification apply for $-40°C \leq T_A \leq 85°C$					
Input Offset Voltage				10	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				250	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−1000	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ	15			V/mV
Output Voltage Range	$R_L = 2$ kΩ	+10			V

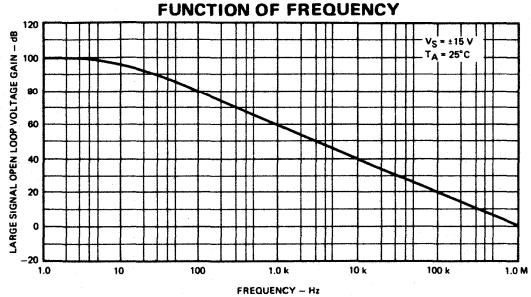
ELECTRICAL CHARACTERISTICS ($V+ = +5.0$ V, $V- = GND$, $T_A = 25°C$ unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage				10	mV
Input Offset Current				75	nA
Input Bias Current				−500	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range	$R_L = 10$ kΩ	3.5			V pk-pk
	$R_L = 10$ kΩ, $5.0 \text{ V} \leq V_S \leq 30$ V	(V+) −1.7			V pk-pk
Power Supply Current			2.5	7.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB

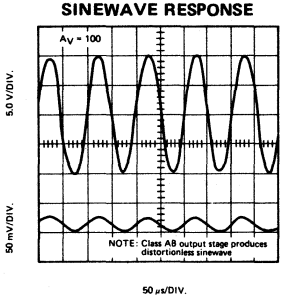
12

TYPICAL PERFORMANCE CURVES

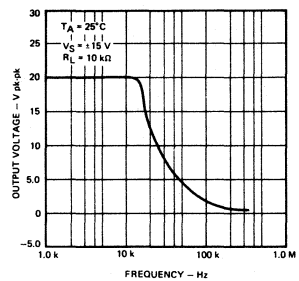
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



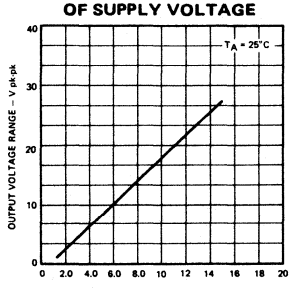
SINEWAVE RESPONSE



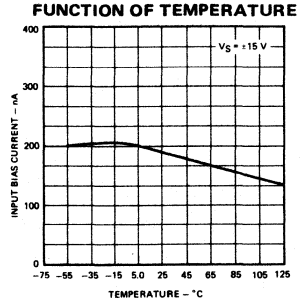
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



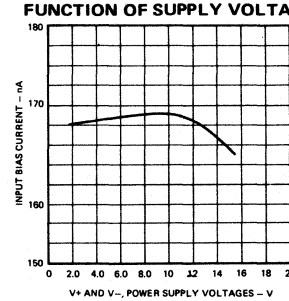
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

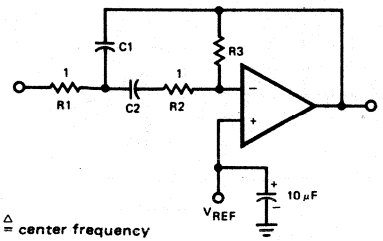


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TYPICAL APPLICATIONS

MULTIPLE FEEDBACK BANDPASS FILTER



$f_o \triangleq$ center frequency

BW $\triangleq$ Bandwidth

R in kΩ

C in μF

$Q = \frac{f_o}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$

$R3 = 9Q^2 - 1$

} Use scaling factors in these expressions.

Design example:

given: $Q = 5$, $f_o = 1$ kHz

Let $R1 = R2 = 10$ kΩ

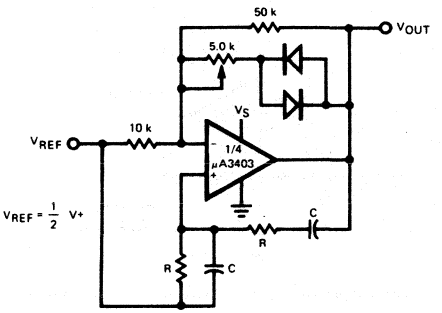
then $R3 = 9(5)^2 - 10$

$R3 = 215$ kΩ

$C = \frac{5}{3} = 1.6$ nF

If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

WEIN BRIDGE OSCILLATOR

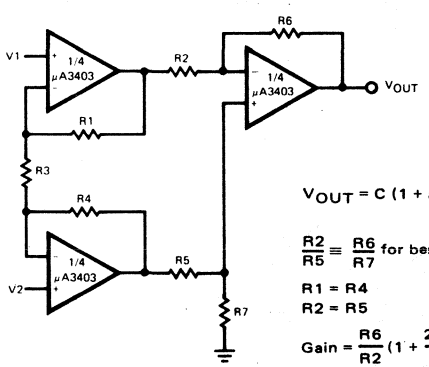


$f_o = \frac{1}{2\pi RC}$ for $f_o = 1$ kHz

$R = 16$ kΩ

$C = 0.01$ μF

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$V_{OUT} = C(1 + a + b)(V2 - V1)$

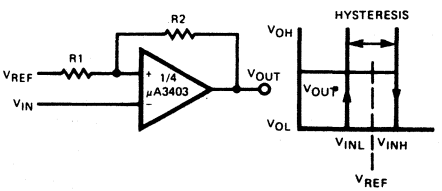
$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

$R1 = R4$

$R2 = R5$

$Gain = \frac{R6}{R2}(1 + \frac{2R1}{R3}) = C(1 + a + b)$

COMPARATOR WITH HYSTERESIS

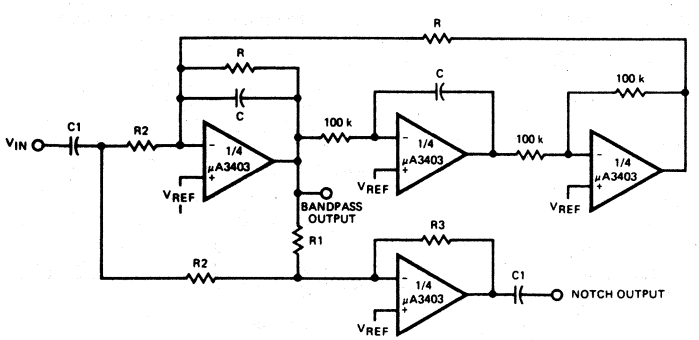


$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$

$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

BI-QUAD FILTER



$Q = \frac{f_o}{BW}$

where

T_{BP} = Center Frequency Gain

T_N = Bandpass Notch Gain

$f_o = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$

$C1 = 10C$

Example:

$f_o = 1000$ Hz

BW = 100 Hz

$T_{BP} = 1$

$T_N = 1$

$R = 160$ kΩ

$R1 = 1.6$ MΩ

$R2 = 1.6$ MΩ

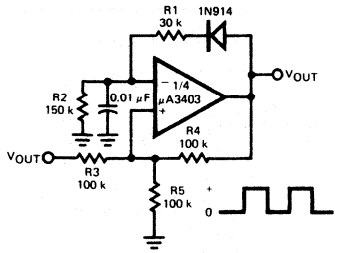
$R3 = 1.6$ MΩ

$C = 0.001$ μF

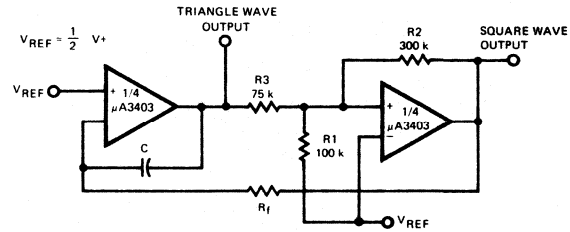
12

TYPICAL APPLICATIONS (Cont'd)

PULSE GENERATOR

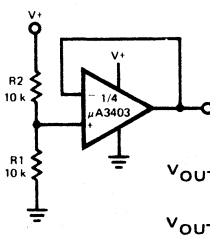


FUNCTION GENERATOR



$$f = \frac{R1 + R2}{4CR_fR1} \quad \text{if} \quad R3 = \frac{R2R1}{R2 + R1}$$

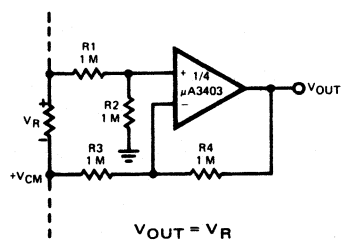
VOLTAGE REFERENCE



$$V_{OUT} = \frac{R1}{R1 + R2} \left(= \frac{V+}{2} \text{ as shown} \right)$$

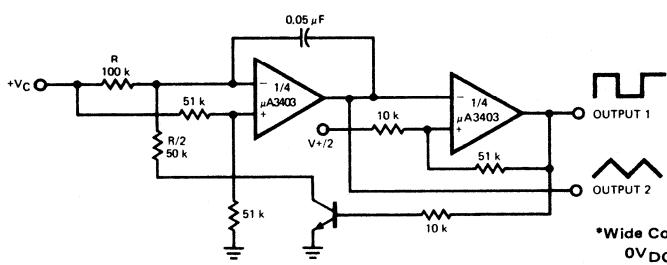
$$V_{OUT} = \frac{1}{2} V_{CC}$$

GROUND REFERENCING A DIFFERENTIAL INPUT SIGNAL



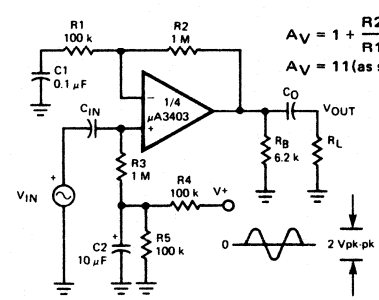
$$V_{OUT} = V_R$$

VOLTAGE CONTROLLED OSCILLATOR



*Wide Control Voltage Range:
$0V_{DC} \leq V_C \leq 2(V+ - 1.5\ V_{DC})$

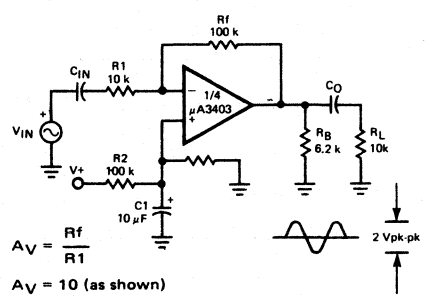
AC COUPLED NON-INVERTING AMPLIFIER



$$A_V = 1 + \frac{R2}{R1}$$

$A_V = 11$ (as shown)

AC COUPLED INVERTING AMPLIFIER



$$A_V = \frac{Rf}{R1}$$

$A_V = 10$ (as shown)

μA4136
QUAD OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

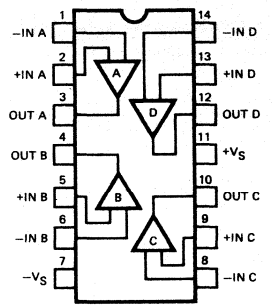
GENERAL DESCRIPTION – The μA4136 monolithic Quad Operational Amplifiers consists of four independent high gain, internally frequency compensated operational amplifiers. The specifically designed low noise input transistors allow the μA4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. They are constructed using the Fairchild Planar* Epitaxial process. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short-circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

- **UNITY GAIN BANDWIDTH 3 MHz**
- **CONTINUOUS SHORT CIRCUIT PROTECTION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **NO LATCH-UP**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **μA741 OPERATIONAL AMPLIFIER TYPE PERFORMANCE**
- **PARAMETER TRACKING OVER TEMPERATURE RANGE**
- **GAIN AND PHASE MATCH BETWEEN AMPLIFIERS**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA4136	±22 V
μA4136C	±18 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	670 mW
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
μA4136	−55°C to +125°C
μA4136C	0°C to +70°C
Storage Temperature Range	
Molded Package	−55°C to +125°C
Hermetic Package	−65°C to +150°C
Lead Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P

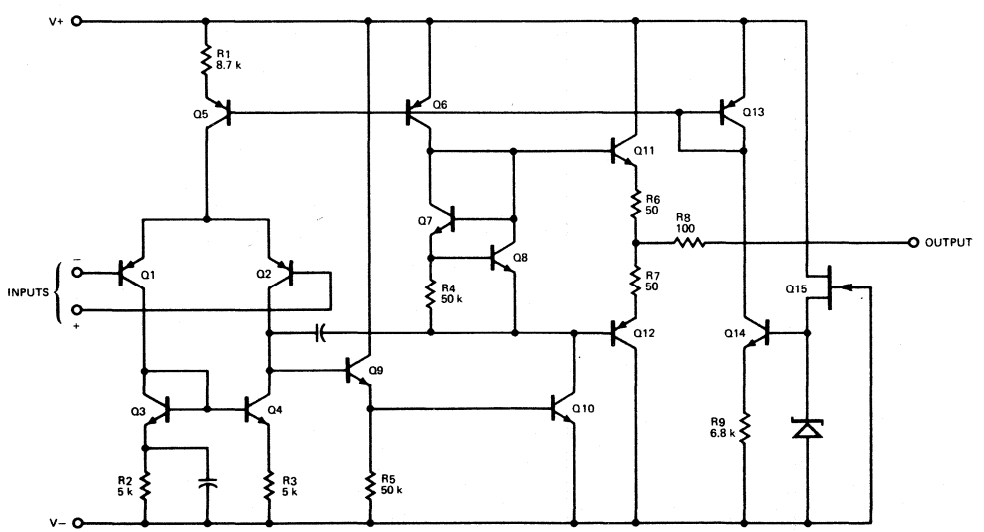


ORDER INFORMATION

TYPE	PART NO.
μA4136	μA4136DM
μA4136C	μA4136DC
μA4136C	μA4136PC

12

1/4 OF EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15 V unless otherwise specified)

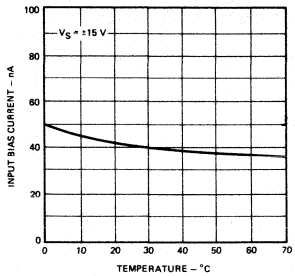
PARAMETER	CONDITIONS	μA4136			μA4136C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ± 10 V	50,000	300,000		20,000	300,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		+12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Power Consumption			210	340		210	340	mW
Transient Response (Unity Gain) Risetime	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.13			0.13		μs
Transient Response (Unity Gain) Overshoot	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		5.0			5.0		%
Unity Gain Bandwidth		2.0	3.0			3.0		MHz
Slew Rate (Unity Gain)	$R_L \geq 2$ kΩ		1.5			1.0		V/μs
Channel Separation (Open Loop)	f = 10 kHz, R_S = 1 kΩ		105			105		dB
(Gain = 100)	f = 10 kHz, R_S = 1 kΩ		105			105		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for μA4136; $0°C \leq T_A \leq +70°C$ for μA4136C.								
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ± 10 V	25,000			15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ V_S = ± 15 V	±12			±10			V
Power Consumption	T_A = High		180	300		180	300	mW
	T_A = Low		240	400		240	400	

NOTES:

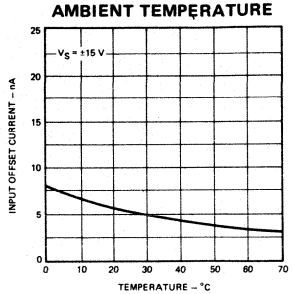
1. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
3. Short-circuit may be to ground, one amplifier only. I_{SC} = 45 mA (Typical).

TYPICAL PERFORMANCE CURVES

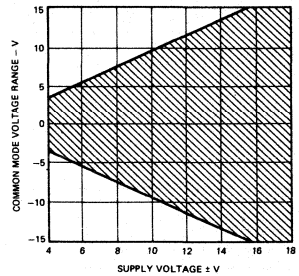
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



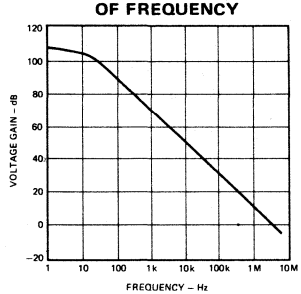
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



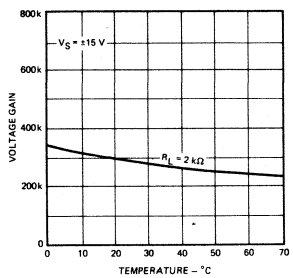
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



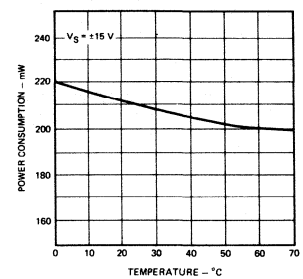
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



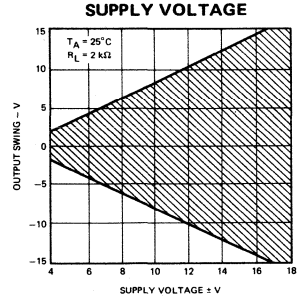
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



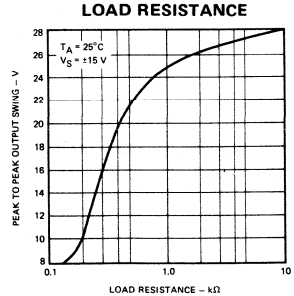
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



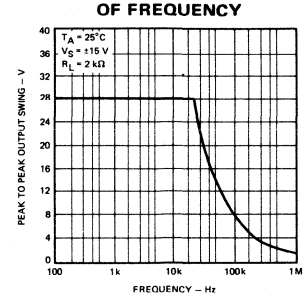
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



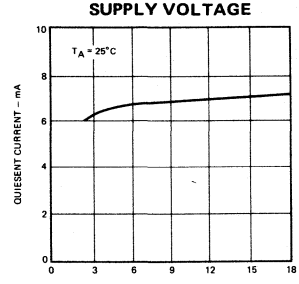
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



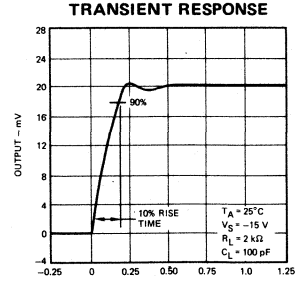
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



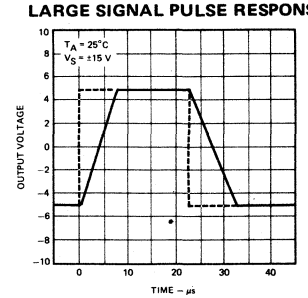
QUIESENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TRANSIENT RESPONSE



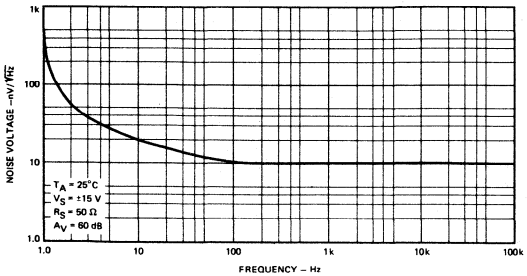
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



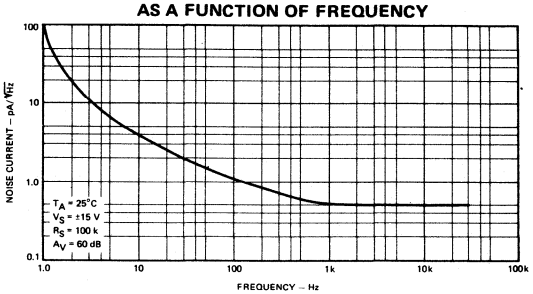
12

TYPICAL PERFORMANCE CURVES (Cont'd)

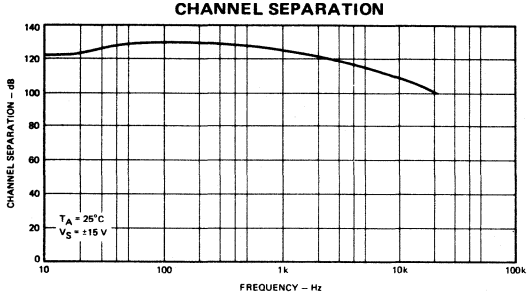
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



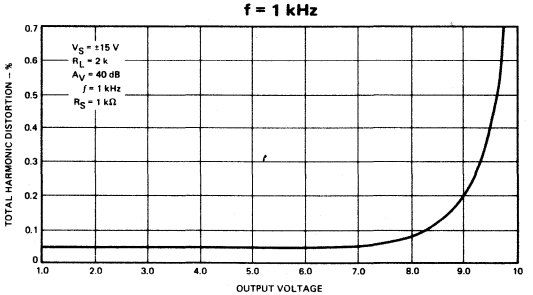
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



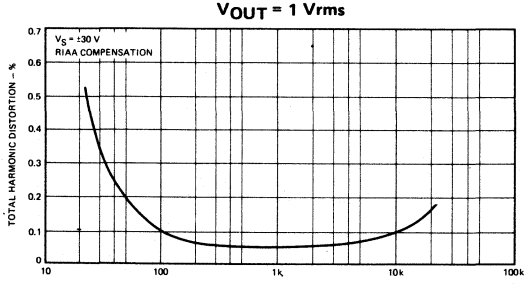
CHANNEL SEPARATION



TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT VOLTAGE f = 1 kHz

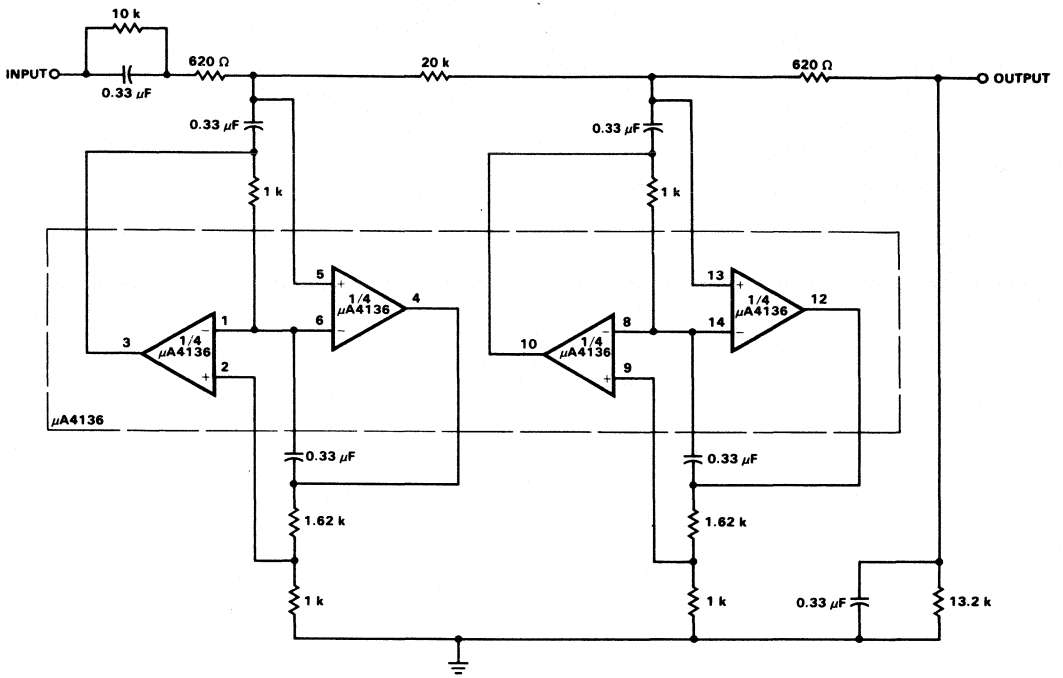


DISTORTION AS A FUNCTION OF FREQUENCY V_{OUT} = 1 Vrms

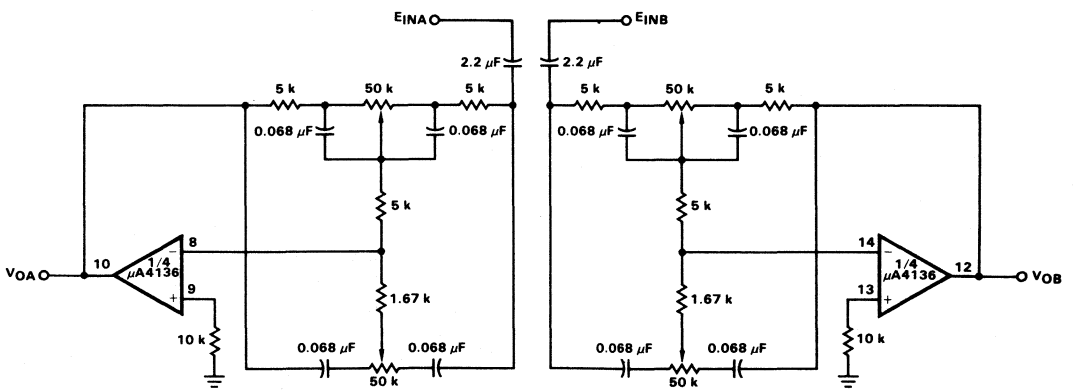


TYPICAL APPLICATIONS

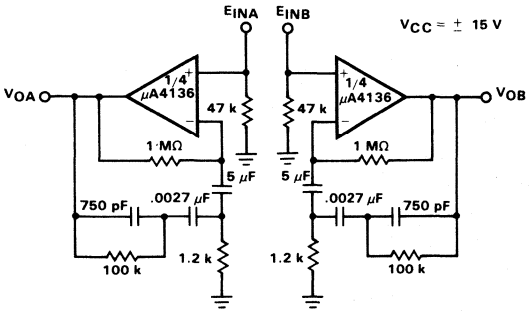
400 Hz LOWPASS BUTTERWORTH ACTIVE FILTER



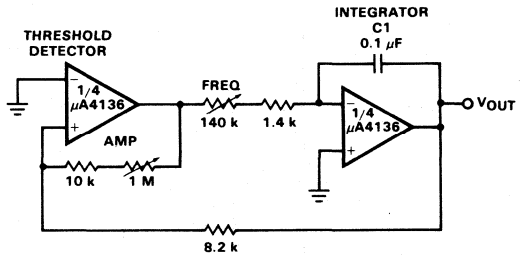
STEREO TONE CONTROL



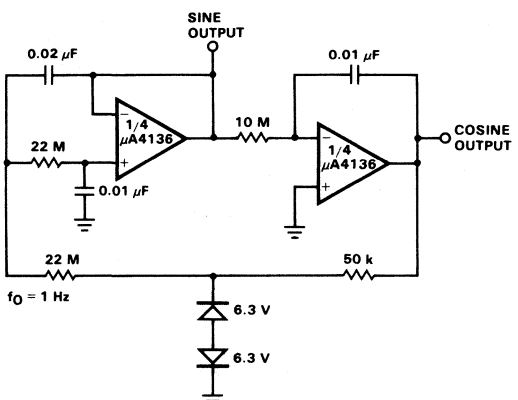
RIAA PREAMPLIFIER



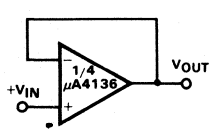
TRIANGULAR-WAVE GENERATOR



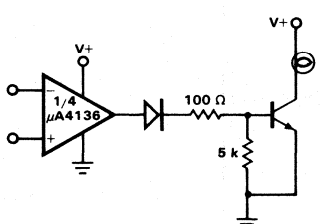
LOW FREQUENCY SINE WAVE GENERATOR WITH QUADRATURE OUTPUT



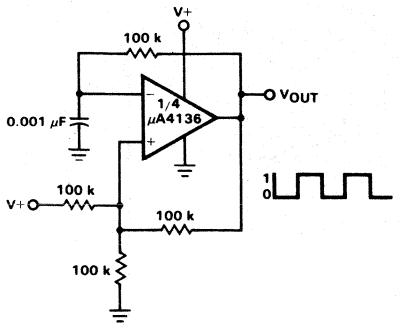
VOLTAGE FOLLOWER



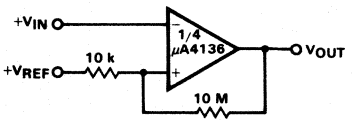
LAMP DRIVER



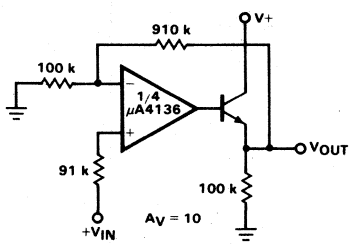
SQUAREWAVE OSCILLATOR



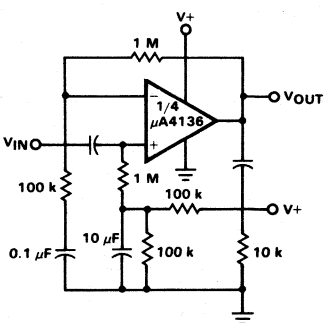
COMPARATOR WITH HYSTERESIS



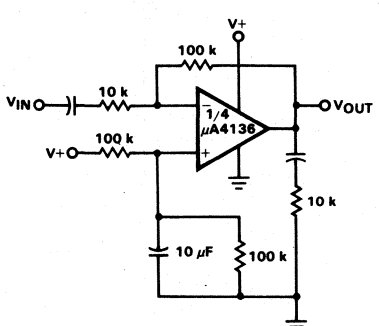
POWER AMPLIFIER



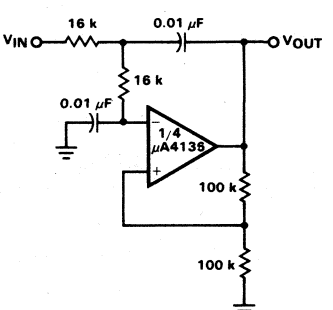
AC COUPLED NON-INVERTING AMPLIFIER



AC COUPLED INVERTING AMPLIFIER

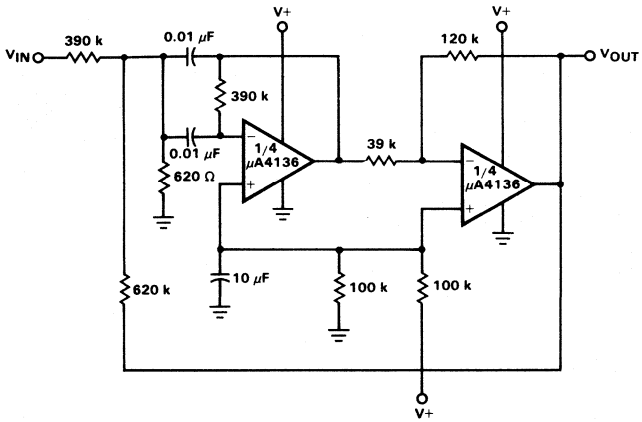


DC COUPLED 1 kHz LOW-PASS ACTIVE FILTER

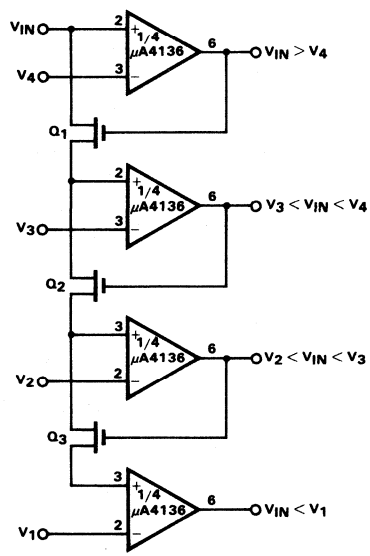


12

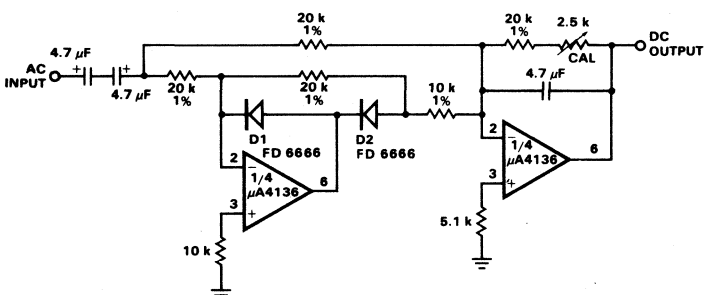
1 kHz BANDPASS ACTIVE FILTER



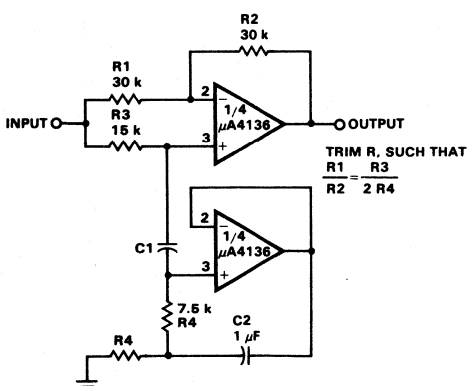
MULTIPLE APERTURE WINDOW DISCRIMINATOR



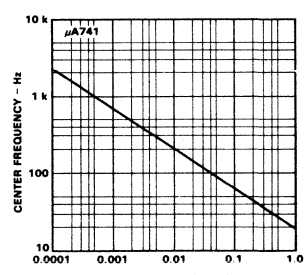
FULL-WAVE RECTIFIER AND AVERAGING FILTER



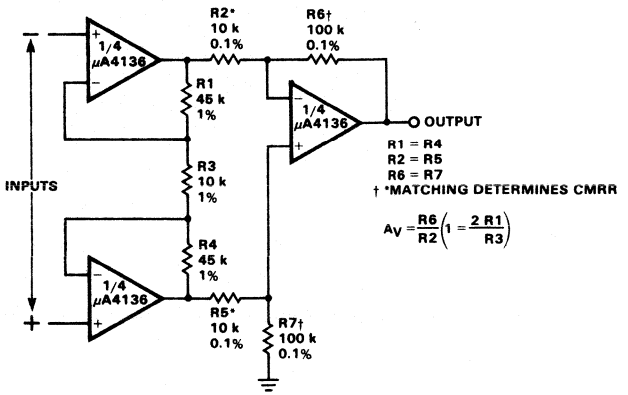
NOTCH FILTER USING THE μA4136 AS A GYRATOR



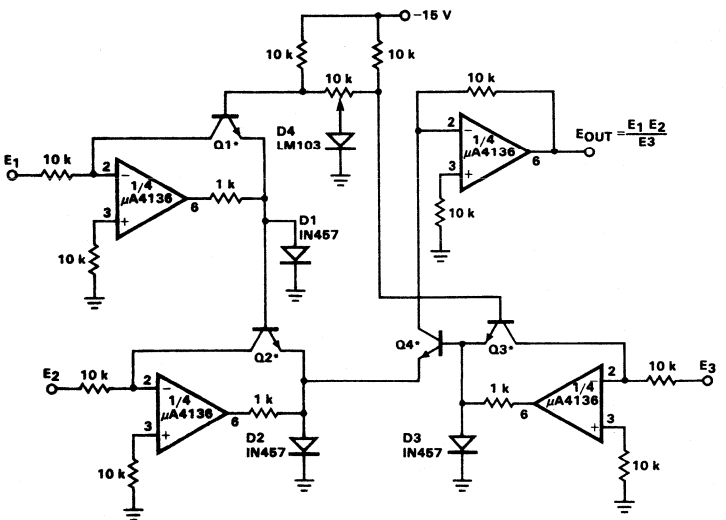
NOTCH FREQUENCY AS A FUNCTION OF C1



DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



ANALOG MULTIPLIER/DIVIDER



OPERATIONAL AMPLIFIERS –
NEW PRODUCTS TO BE ANNOUNCED

12

μA714

OFFSET VOLTAGE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION – The μA714 represents a breakthrough in monolithic operational amplifier performance. V_{OS} of 10 μV, drift temperature coefficient of 0.2 μV/°C, and long-term stability of 0.2 μV/month are achieved by a low noise, chopperless bipolar input transistor amplifier circuit. Complete elimination of external components for offset nulling, frequency compensation, and device protection permits extreme miniaturization and optimization of system Mean-Time-Between-Failure Rates in high performance aerospace/defense and industrial applications. Excellent device interchangeability provides reduced system assembly time and eliminates field recalibrations.

True differential inputs with wide input voltage range and outstanding common mode rejection provide maximum flexibility and performance in high noise environments and non-inverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

Low cost, high volume production of μA714 is achieved by electronic adjustment of an on-chip offset trimming network during initial factory testing. The μA714 provides unparalleled performance for low noise, high accuracy amplification of very low level signals in transducer applications. Other applications include use in stable integrators, precision summing amplifiers for analog computation and test equipment and in ultra-precise voltage threshold detectors and comparators.

● Super Low V_{OS}	10 μV
● Super Low V_{OS} Drift	0.2 μV/°C
● Super Stable versus Time	0.2 μV/Mo.
● Super Low Noise	0.35 μV/p-p
● Low Input Offset Current	300 pA
● Low Input Bias Current	700 pA
● No External Components Required	
● Replaces Chopper Amps at Lower Cost	
● High Common Mode Input Range	±14 V
● Wide Supply Voltage Range	±3 V to ±18 V

INDEX

μA555
SINGLE TIMING CIRCUIT
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out.

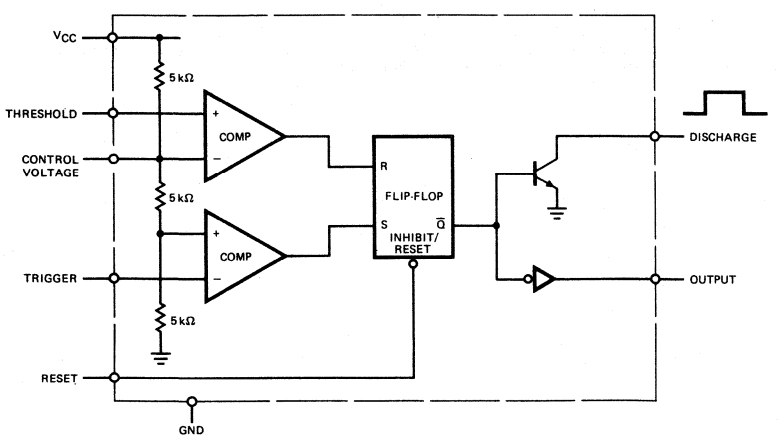
The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

- **MICROSECONDS THROUGH HOURS TIMING CONTROL**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT CAPABILITY**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**
- **DIRECT REPLACEMENT FOR SE555/NE555**

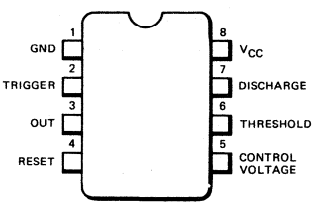
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
μA555TC/HC	0°C to +70°C
μA555HM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Plastic Mini DIP(9T) (Soldering, 10 s)	260°C
Metal Can (5T) (Soldering, 60 s)	300°C

BLOCK DIAGRAM



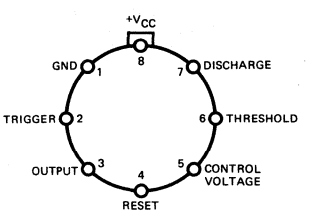
CONNECTION DIAGRAMS
8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
μA555	μA555TC

8-LEAD TO-100
(TOP VIEW)
PACKAGE OUTLINE 5T



ORDER INFORMATION

TYPE	PART NO.
μA555	μA555HM
μA555	μA555HC

13

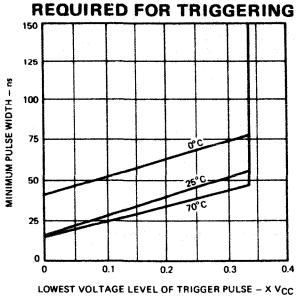
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V to +15 V, unless otherwise specified)

PARAMETER	TEST CONDITIONS	μA555HM			μA555TC/HC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5.0 V, R_L = ∞		3.0	5.0		3.0	6.0	mA
	V_{CC} = 15 V, R_L = ∞ LOW State (Note 1)		10	12		10	15	mA
Timing Error								
Initial Accuracy	R_A, R_B = 1 kΩ to 100 kΩ		0.5	2.0		1.0		%
Drift with Temperature	C = 0.1 μF (Note 2)		30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%V
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15 V	4.8	5.0	5.2		5.0		V
	V_{CC} = 5.0 V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15 V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5.0 V	2.9	3.33	3.8	2.6	3.33	4.0	V
Output Voltage Drop (LOW)	V_{CC} = 15 V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5.0 V							
	I_{SINK} = 8.0 mA		0.1	0.25				V
	I_{SINK} = 5.0 mA					0.25	0.35	V
Output Voltage Drop (HIGH)	I_{SOURCE} = 200 mA							
	V_{CC} = 15 V		12.5			12.5		V
	I_{SOURCE} = 100 mA							
	V_{CC} = 15 V	13	13.3		12.75	13.3		V
	V_{CC} = 5.0 V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

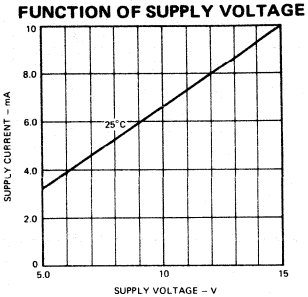
NOTES:
1. Supply Current is typically 1.0 mA less when output is HIGH.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B. For 15 V operation, the max total R = 20 MΩ.
4. For operating at elevated temperatures the device must be derated based on a +125°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

TYPICAL PERFORMANCE CURVES

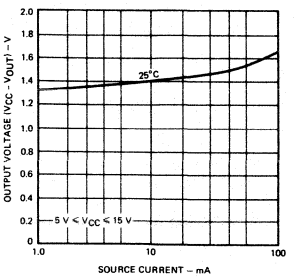
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



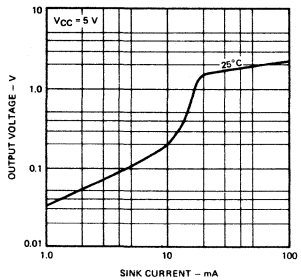
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



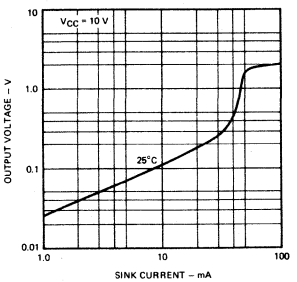
HIGH OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SOURCE CURRENT



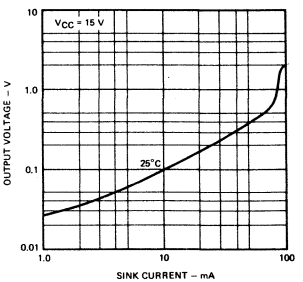
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



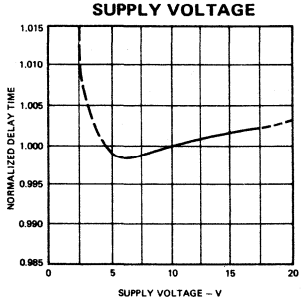
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



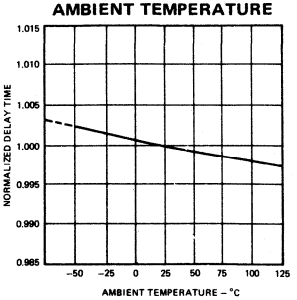
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



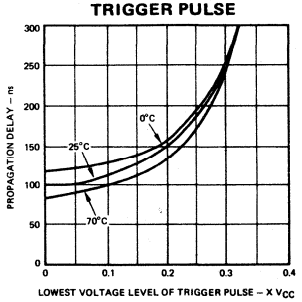
DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE



DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE

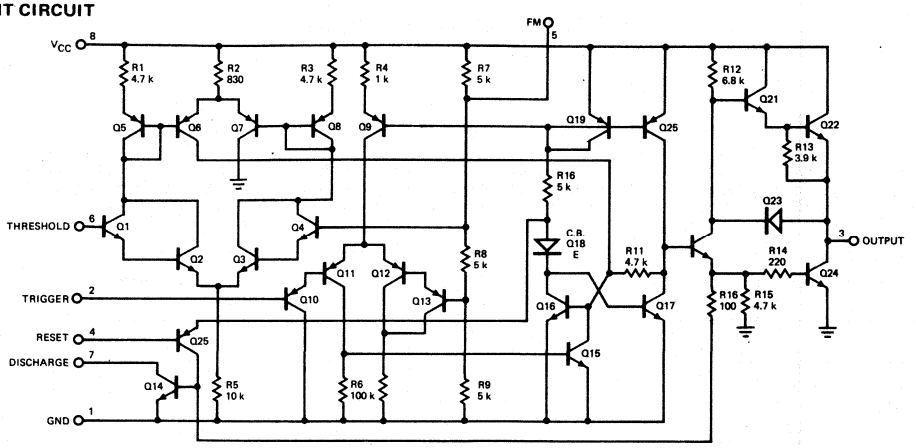


PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



13

EQUIVALENT CIRCUIT



TYPICAL APPLICATIONS

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 2, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant τ = R1C1. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the Trigger terminal (lead 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

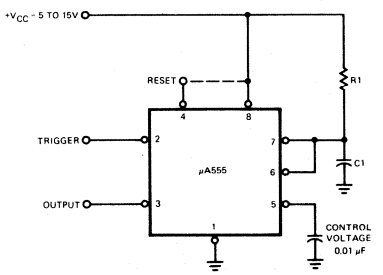


Fig. 1

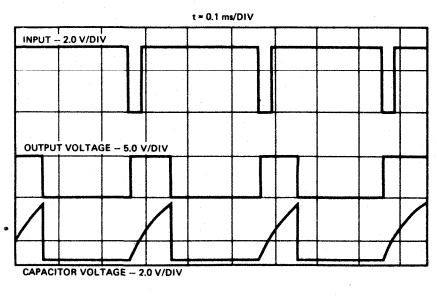


Fig. 2

TIME DELAY AS A FUNCTION OF R1 AND C1

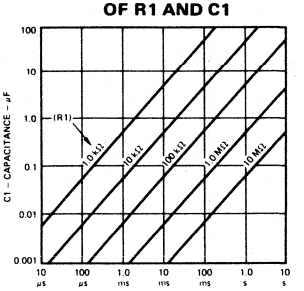


Fig. 3

TYPICAL APPLICATIONS (Cont'd)

ASTABLE OPERATION

When the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

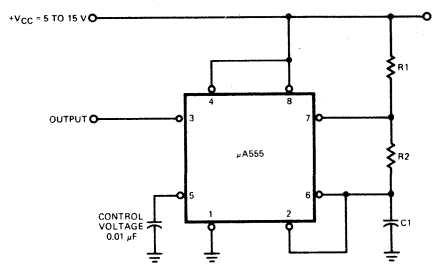


Fig. 4

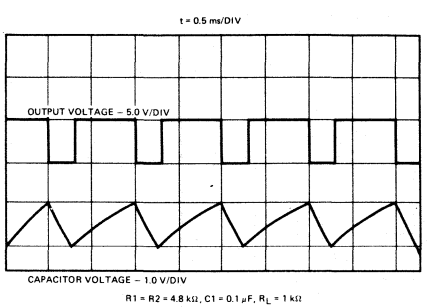


Fig. 5

FREE RUNNING FREQUENCY AS A FUNCTION OF R1, R2 AND C1

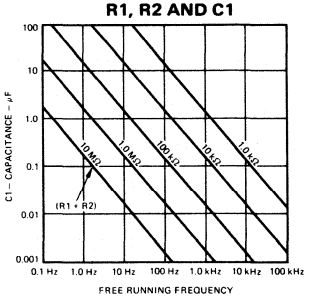


Fig. 6

μA556
DUAL TIMING CIRCUIT
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA556 Timing Circuits are very stable controllers for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied, ending the time-out.

The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

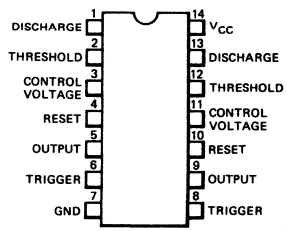
The μA556 Dual Timing Circuit is a pair of 555s for use in sequential timing or applications requiring multiple timers.

- **MICROSECONDS THROUGH HOURS TIMING CONTROL**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT CAPABILITY**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Power Dissipation	600 mW
Operating Temperature Ranges	
μA556 DC/PC	0°C to +70°C
μA556DM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering)	
(10 s) Plastic DIP (9A)	260°C
(60 s) Ceramic DIP (6A)	300°C

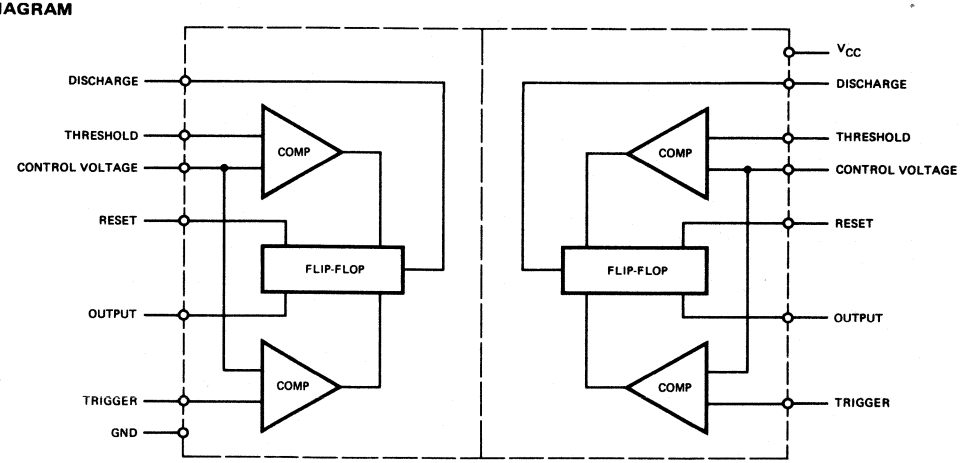
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA556	μA556DC
μA556	μA556DM
μA556	μA556PC

BLOCK DIAGRAM



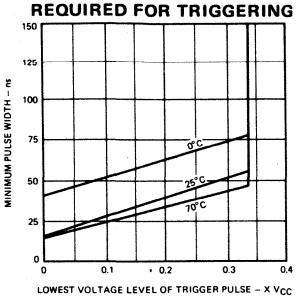
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V to +15 V, unless otherwise specified)

PARAMETER	TEST CONDITIONS	μA556DM			μA556DC/PC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current (Total)	V_{CC} = 5.0 V, R_L = ∞		6.0	10		6.0	12	mA
	V_{CC} = 15 V, R_L = ∞ LOW State (Note 1)		20	22		20	28	mA
Timing Error (Monostable)								
Initial Accuracy	R_A = 2 kΩ to 100 kΩ		0.5	1.5		0.75		%
Drift with Temperature	C = 0.1 μF (Note 2)		30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%V
Timing Error (Astable)								
Initial Accuracy	R_A, R_B = 2 kΩ to 100 kΩ		1.5			2.25		%
Drift with Temperature	C = 0.1 μF (Note 2)		90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%V
Threshold Voltage			2/3			2/3		X V_{CC}
Threshold Current	Note 3		30	100		30	100	nA
Trigger Voltage	V_{CC} = 15 V	4.8	5.0	5.2		5.0		V
	V_{CC} = 5.0 V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	V_{CC} = 15 V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5.0 V	2.9	3.33	3.8	2.6	3.33	4.0	V
Output Voltage (LOW)	V_{CC} = 15 V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2.0	2.25		2.0	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5.0 V							
	I_{SINK} = 8.0 mA		0.1	0.25				V
	I_{SINK} = 5.0 mA					0.25	0.35	V
Output Voltage (HIGH)	I_{SOURCE} = 200 mA							
	V_{CC} = 15 V		12.5			12.5		V
	I_{SOURCE} = 100 mA							
	V_{CC} = 15 V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5.0V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics (Note 4)								
Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%V

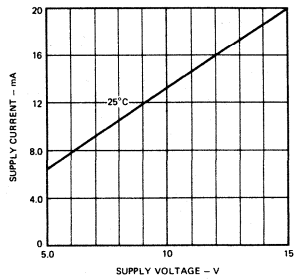
NOTES:
1. Supply current when output is HIGH is typically 1.0 mA less.
2. Tested at V_{CC} = 5 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total R = 20 MΩ.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.

TYPICAL PERFORMANCE CURVES

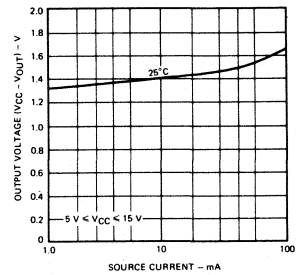
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



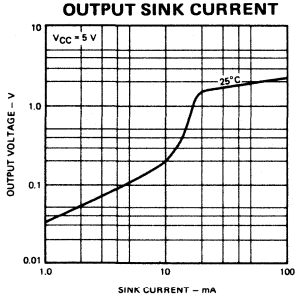
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



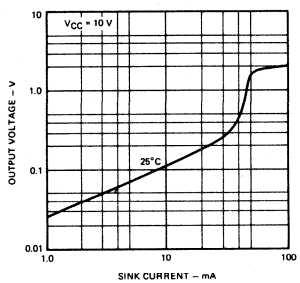
HIGH OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SOURCE CURRENT



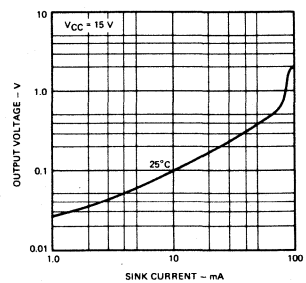
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



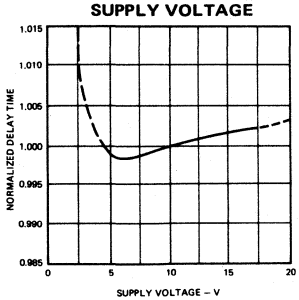
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



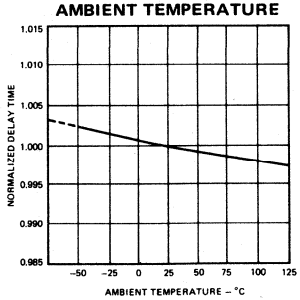
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



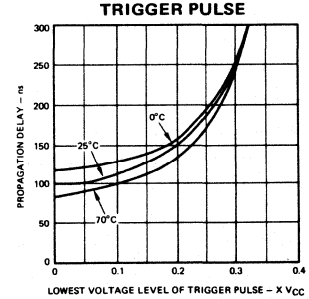
DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE



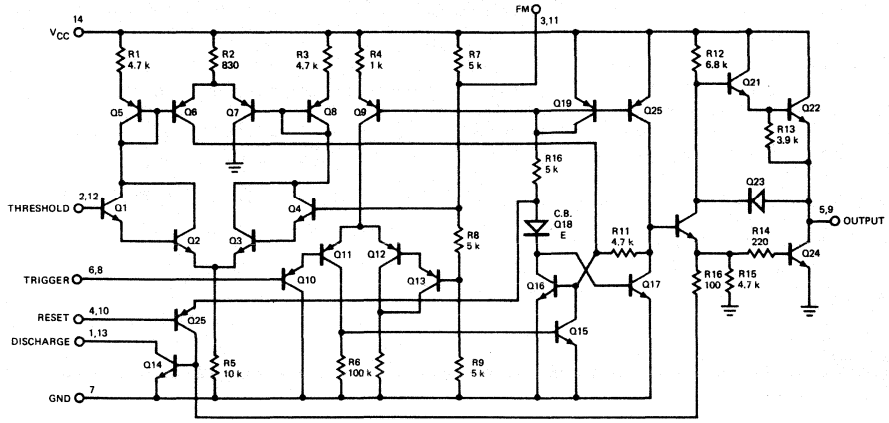
DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE



PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



EQUIVALENT CIRCUIT (One Half of μA556)



TYPICAL APPLICATIONS

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 6, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R1C1$ and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the Trigger terminal (lead 6) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

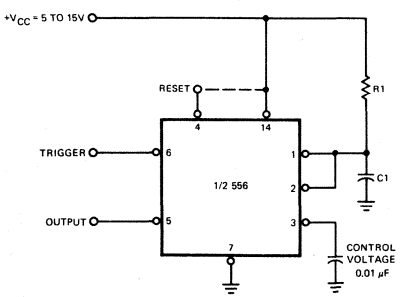


Fig. 1

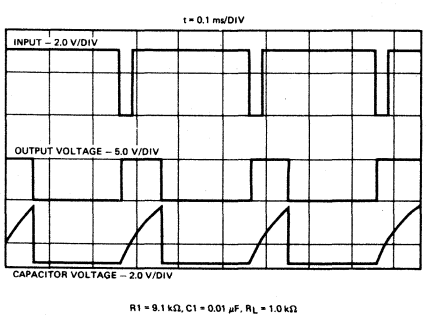


Fig. 2

TIME DELAY AS A FUNCTION OF R1 AND C1

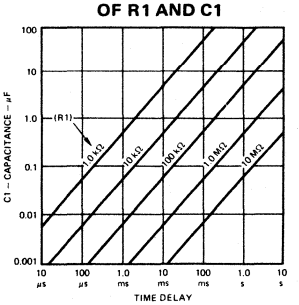


Fig. 3

TYPICAL APPLICATIONS (Cont'd)

ASTABLE OPERATION

When the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

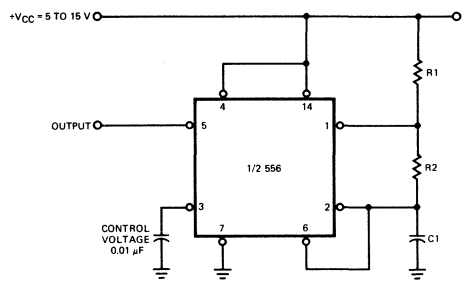
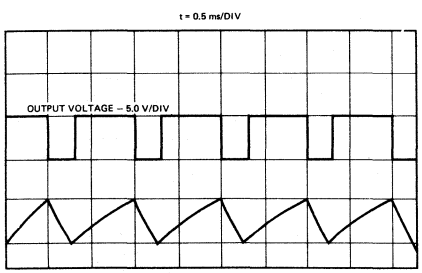


Fig. 4



R1 = R2 = 4.8 kΩ, C1 = 0.1 μF, R_L = 1 kΩ

Fig. 5

FREE RUNNING FREQUENCY AS A FUNCTION OF R1, R2 AND C1

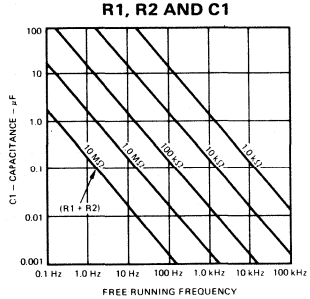
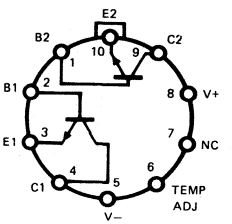


Fig. 6

μA726
TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA726 is a Monolithic Transistor Pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers. It is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

CONNECTION DIAGRAM
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5I
PACKAGE CODE H



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
Military (μA726)	−55°C to +125°C
Commercial (μA726C)	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V
Internal Power Dissipation	500mW

MAXIMUM RATINGS FOR EACH TRANSISTOR

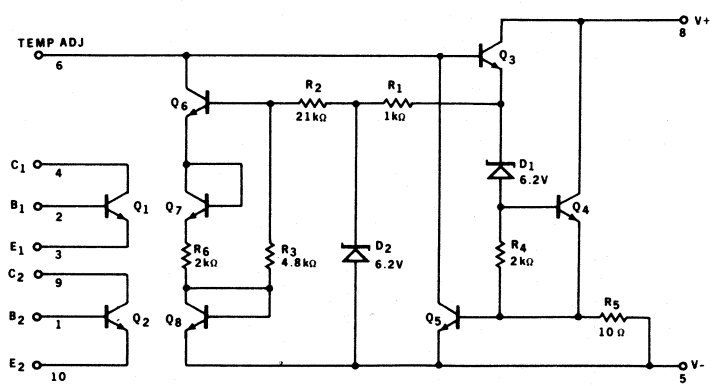
Collector-to-Emitter Voltage, V_{CEO}	30V
Collector-to-Base Voltage, V_{CBO}	40V
Collector-to-Substrate Voltage, V_{CIO}	40V
Emitter-to-Base Voltage, V_{EBO}	5V
Collector Current, I_C	5mA

ORDER INFORMATION

TYPE	PART NO.
μA726	μA726HM
μA726C	μA726HC

13

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA726

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15V$, $R_{adj} = 62k\Omega$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\mu A$, $V_{CE} = 5V$		10	50	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		50	200	nA
Average Input Bias Current	$I_C = 10\mu A$, $V_{CE} = 5V$		50	150	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		250	500	nA
Offset Voltage Change	$I_C = 10\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100k\Omega$		0.3	6.0	mV
	$I_C = 100\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	μV/°C
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	μV/°C
Input Offset Current Drift	$I_C = 10\mu A$, $V_{CE} = 5V$		10		pA/°C
	$I_C = 100\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\mu A$, $R_S \leq 50\Omega$,		25		μV/V
Low Frequency Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		μV p-p
Broadband Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10kHz		10		μV p-p
Long-term Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	$f = 20MHz$, $I_C = 100\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu A$, $I_C = 1mA$		0.5	1.0	V

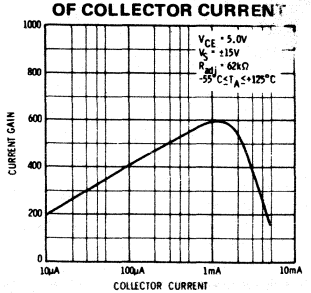
μA726C

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +85°C$, $V_S = \pm 15V$, $R_{adj} = 75k\Omega$ unless otherwise specified)

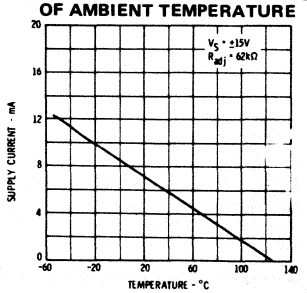
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\mu A$, $V_{CE} = 5V$		10	100	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		50	400	nA
Average Input Bias Current	$I_C = 10\mu A$, $V_{CE} = 5V$		50	300	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		250	1000	nA
Offset Voltage Change	$I_C = 10\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100k\Omega$		0.3	6.0	mV
	$I_C = 100\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		0.2	2.0	μV/°C
Input Offset Current Drift	$I_C = 10\mu A$, $V_{CE} = 5V$		10		pA/°C
	$I_C = 100\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$I_C = 100\mu A$, $R_S = 50\Omega$		25		μV/V
Low Frequency Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		μV p-p
Broadband Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz		10		μV p-p
Long-Term Drift	$I_C = 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	$f = 20MHz$, $I_C = 100\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu A$, $I_C = 1mA$		0.5	1.0	V

TYPICAL PERFORMANCE CURVES FOR μA726

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT

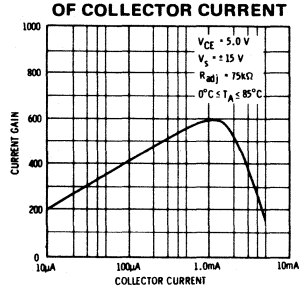


SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

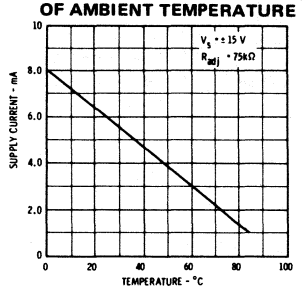


TYPICAL PERFORMANCE CURVES FOR μA726C

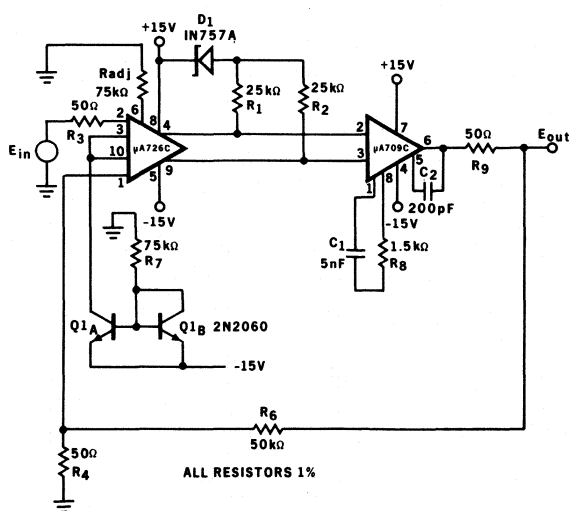
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 AMPLIFIER CIRCUIT



13

μA733

DIFFERENTIAL VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

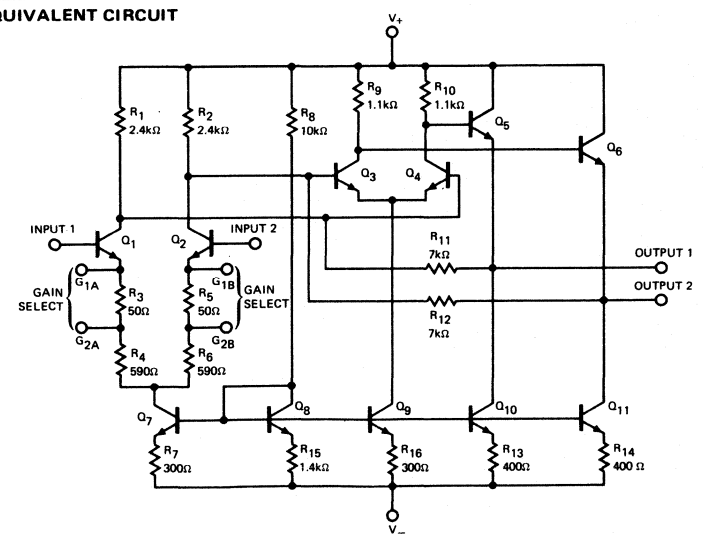
GENERAL DESCRIPTION – The μA733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier constructed using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Flatpak	570 mW
DIP	670 mW
Operating Temperature Range	
Military (μA733)	−55° C to +125° C
Commercial (μA733C)	0° C to +70° C
Storage Temperature Range	−65° C to +150° C
Lead Temperature (Soldering, 60 second time limit)	300° C

EQUIVALENT CIRCUIT



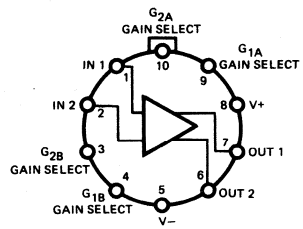
CONNECTION DIAGRAMS

10-LEAD METAL CAN

(TOP VIEW)

PACKAGE OUTLINE 5N

PACKAGE CODE H



Note: Pin 5 connected to case.

ORDER INFORMATION

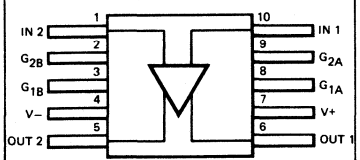
TYPE	PART NO.
μA733	μA733HM
μA733C	μA733HC

10-LEAD FLATPAK

(TOP VIEW)

PACKAGE OUTLINE 3F

PACKAGE CODE F



ORDER INFORMATION

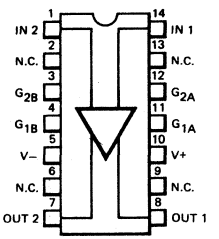
TYPE	PART NO.
μA733	μA733FM

14-LEAD DIP

(TOP VIEW)

PACKAGE OUTLINE 6A

PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA733	μA733DM
μA733C	μA733DC

Notes on following pages.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for −55°C ≤ T_A ≤ +125°C					
Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance					
Gain 2		8.0			kΩ
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage					
Gain 1				1.5	V
Gain 2 and Gain 3				1.2	V
Output Swing		2.5			V_{p-p}
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

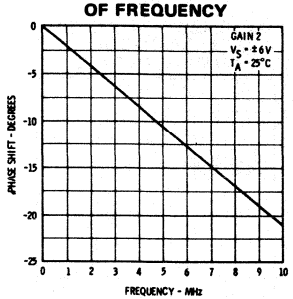
μA733C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

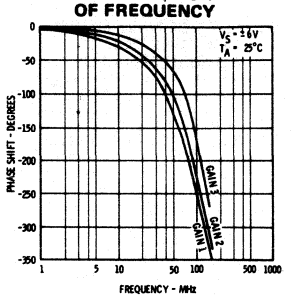
PARAMETER (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μV_{rms}
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for 0°C ≤ T_A ≤ ±70°C					
Differential Voltage Gain					
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	50			dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			V_{p-p}
Output Sink Current		2.5			mA
Power Supply Current				27	mA

TYPICAL PERFORMANCE CURVES FOR μA733 AND μA733C

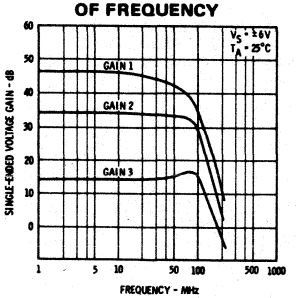
PHASE SHIFT AS A FUNCTION OF FREQUENCY



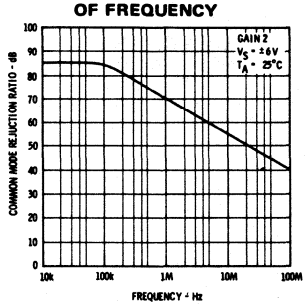
PHASE SHIFT AS A FUNCTION OF FREQUENCY



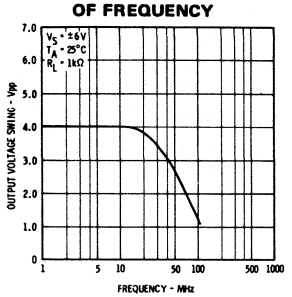
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



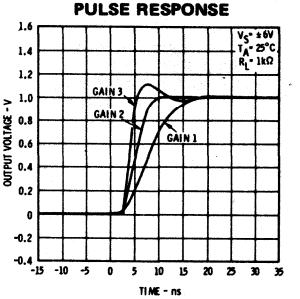
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



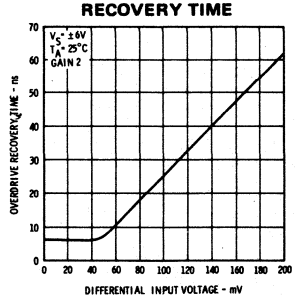
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



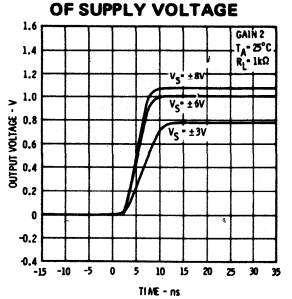
PULSE RESPONSE



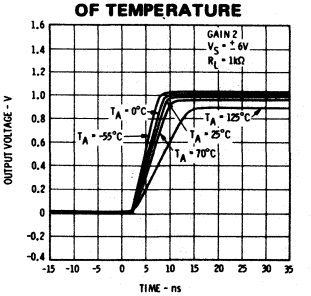
DIFFERENTIAL OVERDRIVE RECOVERY TIME



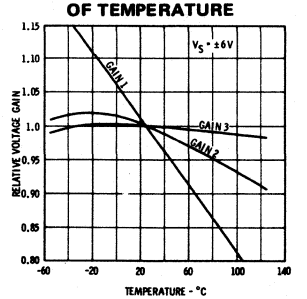
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



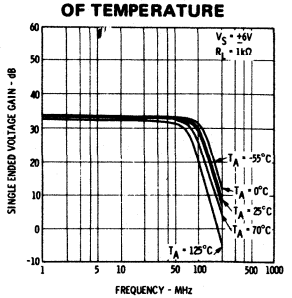
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



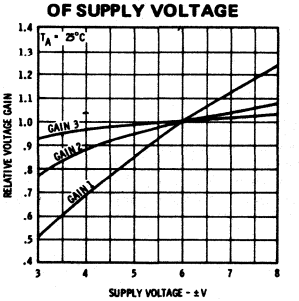
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE



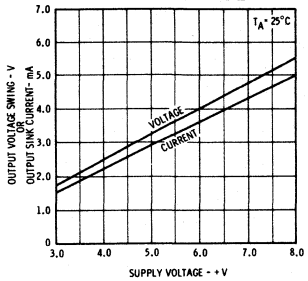
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



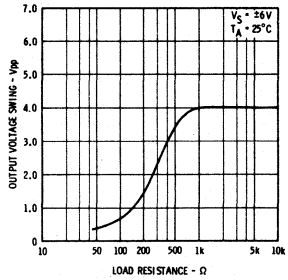
13

TYPICAL PERFORMANCE CURVES FOR μA733 AND μA733C

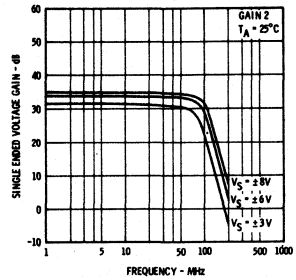
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



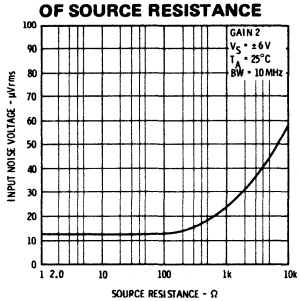
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



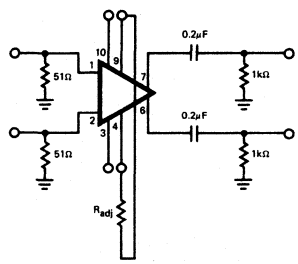
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



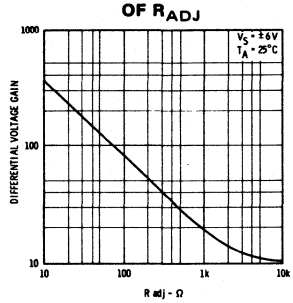
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



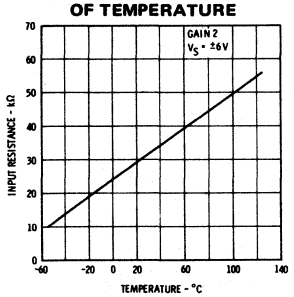
VOLTAGE GAIN ADJUST CIRCUIT



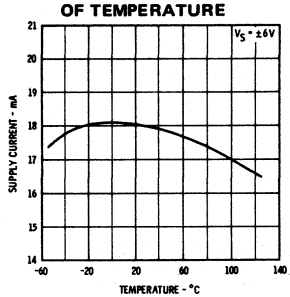
VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



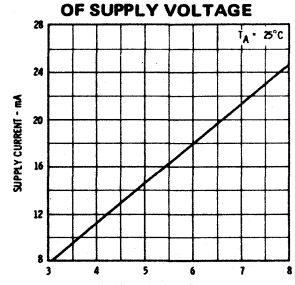
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

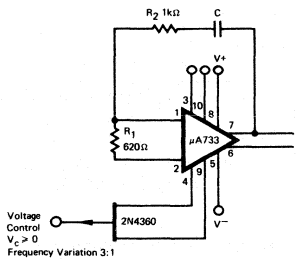


NOTES

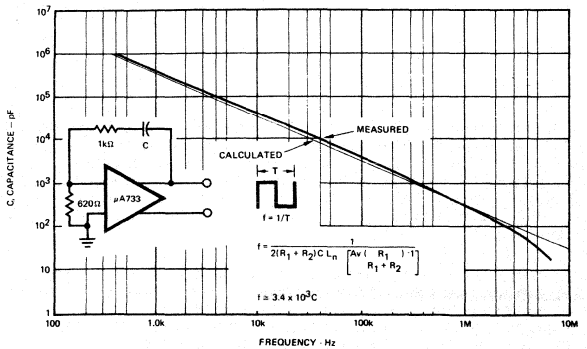
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP and 7.1 mW/°C for the Flatpak.
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

TYPICAL APPLICATIONS

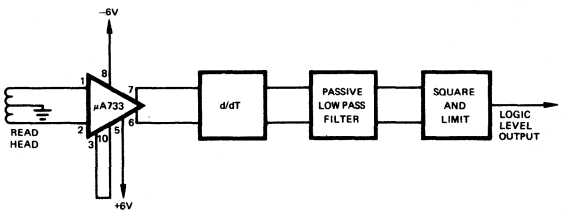
VOLTAGE CONTROLLED OSCILLATOR



OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



PHASE ENCODING PLAYBACK SYSTEM



Phase Linearity:	±4° from 2 to 5 MHz
Input Resistance:	30 kΩ
Input Capacity:	2 pF
Fixed Gain:	100

13

μA742

ZERO CROSSING AC TRIGGER-TRIGAC

FAIRCHILD LINEAR INTEGRATED CIRCUIT

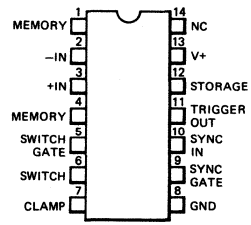
GENERAL DESCRIPTION – The μA742 is a monolithic Zero Crossing AC Trigger (TRIGAC) utilizing the Fairchild Planar* Epitaxial Process. It is intended for use in ac power control circuits for operation directly off the ac line or with a separate ac or dc power supply. The TRIGAC functions as a threshold detector and a driver for triacs and SCR's. As a threshold detector, it senses level changes at the inputs and as a driver it supplies high energy pulses for thyristor triggering. The trigger pulses occur at the zero crossing of the load current and therefore minimize RFI generation for either resistive or inductive loads

- **DESIGNED FOR APPLICATIONS IN 60Hz TO 400 Hz AC POWER CONTROL SYSTEMS HAVING RESISTIVE OR INDUCTIVE LOADS**
- **OPERATES DIRECTLY FROM AN AC LINE OR FROM A DC SUPPLY**
- **INPUT COMPATIBLE WITH A WIDE RANGE OF SENSOR IMPEDANCES**
- **BRIDGE SENSING WITH ADJUSTABLE HYSTERESIS SET POINTS**
- **PROVISIONS FOR TIME PROPORTIONING OPERATION**
- **PROVIDES ZERO CROSSING THYRISTOR TRIGGERING FOR MINIMUM RFI**
- **EVEN NUMBER OF CONSECUTIVE HALF-CYCLE TRIGGERINGS FOR TRIACS AND INVERSE PARALLEL SCR's IN MOST APPLICATIONS**

ABSOLUTE MAXIMUM RATINGS

Peak Current into Supply Terminal (ac Operation)	±30mA
Continuous Current into Supply Terminal (dc Operation)	20mA
RMS Current into Sync Input Terminal	15mA
Current into Switch Terminal	10mA
Power Dissipation	670mW
Voltage at (+) or (–) Input Terminal	(Note 1)
Differential Voltage between (+) and (–) Input Terminals	±7V
Current into Clamp Terminal (Clamp ON)	20mA
Voltage at Clamp Terminal (Clamp OFF)	25V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Trigger Output Short-Circuit Duration (Note 2)	Continuous

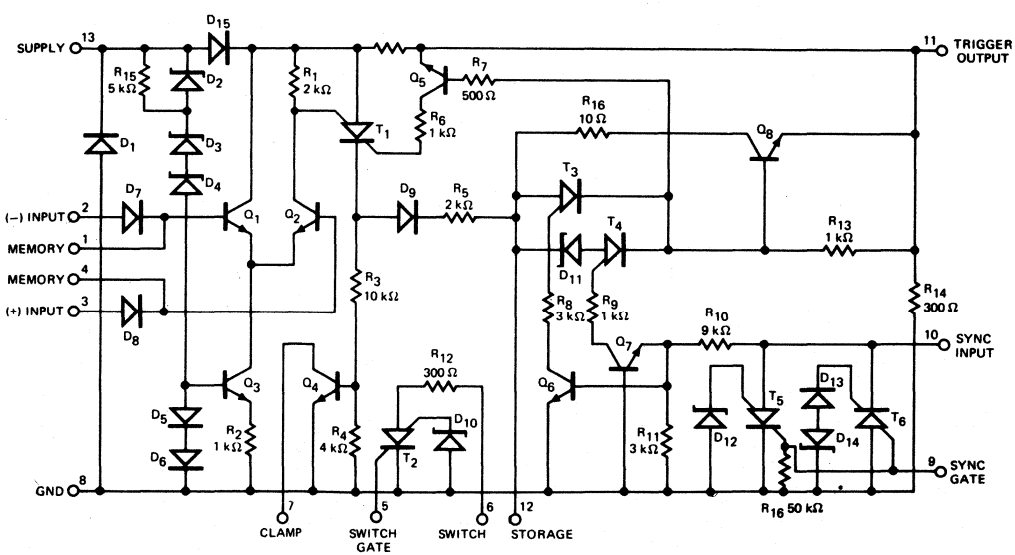
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA742C	μA742PC
μA742C	μA742DC

EQUIVALENT CIRCUIT

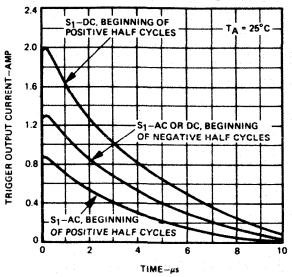


Notes on following pages.

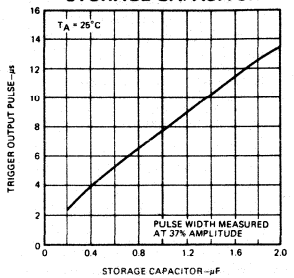
*Planar is a patented Fairchild process.

TYPICAL PERFORMANCE CURVES FOR μA742C
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

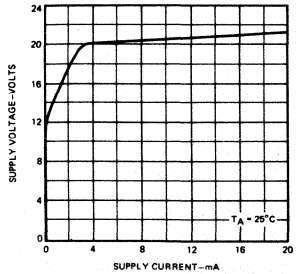
TRIGGER OUTPUT PULSE WAVE FORMS



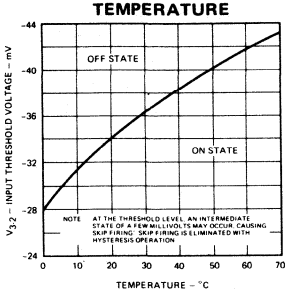
TRIGGER OUTPUT PULSE WIDTH AS A FUNCTION OF STORAGE CAPACITOR



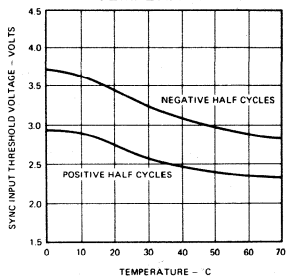
SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



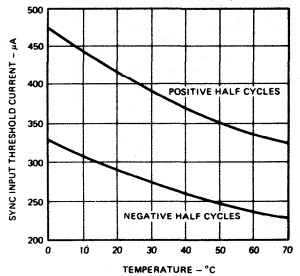
INPUT THRESHOLD VOLTAGE AS A FUNCTION OF TEMPERATURE



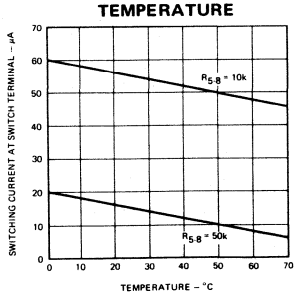
SYNC INPUT THRESHOLD VOLTAGE AS A FUNCTION OF TEMPERATURE



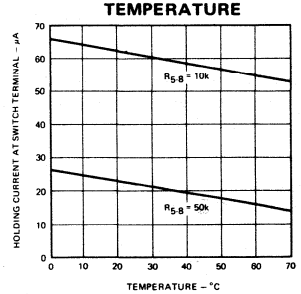
SYNC INPUT THRESHOLD CURRENT AS A FUNCTION OF TEMPERATURE



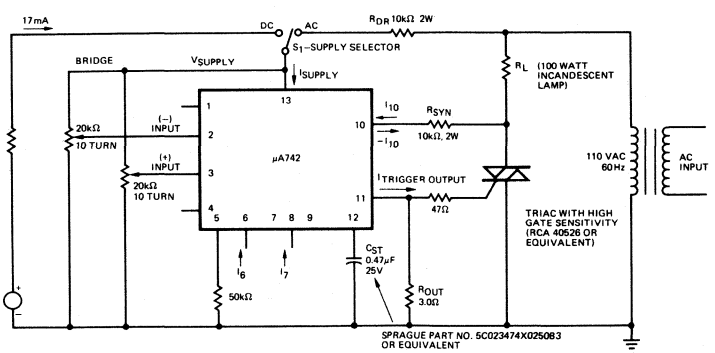
SWITCHING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE



HOLDING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE



TEST CIRCUIT 1



13

μA742C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltage Range at the (+) and (–) Input Terminals: 2.5V to 17V; $V_{(+)\ Input} - V_{(-)\ Input} \geq 50mV$, Test Circuit 1, unless otherwise specified.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Peak Supply Voltage	S_1 in dc position	19	21	26	V
	S_1 in ac position, positive half cycles of ac line	19	21	26	V
	S_1 in ac position, negative half cycle of ac line	-1.6	-0.95	-0.8	V
Peak Trigger Output Pulse	S_1 in ac position, beginning of positive half cycles	0.6	0.9		A
	S_1 in ac or dc position, beginning of negative half cycles	1.0	1.3		A
	S_1 in dc position beginning of positive half cycles	1.6	2.0		A
Bias Current at (+) and (–) Terminals			15	25	μA
Input Threshold Voltage for Output Pulse Enable		-50	-35	50	mV
ON Voltage at Clamp Terminal	I_7 = 1 mA		85	200	mV
ON Voltage at Switch Terminal	I_6 = 5 mA		2.6	3.0	V
Switching Voltage at Switch Terminal		6.0	7.2		V
Switching Current at Switch Terminal			15		μA
Holding Current at Switch Terminal			23	200	μA
ON Voltage at Sync Input Terminal	I_{10} = 10 mA		1.9	2.2	V
	I_{10} = -10 mA	-2.2	-1.9		V
Switching Voltage at Sync Input Terminal	I_{10} = 2 mA, positive half cycles, $V_{(-)\ Input} - V_{(+)\ Input} > 50$ mV	4.5	5.8		V
	I_{10} = -2 mA, negative half cycles, $V_{(-)\ Input} - V_{(+)\ Input} > 50$ mV		-7.0	-4.5	V
Sync Input Threshold Current for Trigger Output	Beginning of positive half cycles	180	410	500	μA
	Beginning of negative half cycles	-500	-280	-180	μA
Sync Input Threshold Voltage for Trigger Output	Beginning of positive half cycles	2.0	2.7	4.0	V
	Beginning of negative half cycles	-4.0	-3.3	-2.0	V

DEFINITIONS

VOLTAGE RANGE: The range of voltage on the (+) or (–) input terminals, which, if exceeded, could cause the TRIGAC to cease functioning.

BIAS CURRENT: The average of the two currents into the (+) and (–) input terminals.

NOTES:

(1) The maximum voltage should not exceed the instantaneous supply voltage of the μA742.

(2) Rating applies for an external storage capacitor having a value of not more than 2μF.

TYPICAL APPLICATIONS FOR μA742C

NOTES

*Recommended Values

AC Supply Voltage 60Hz Volts - RMS	R_{DR}	R_{SYN}	C_{ST}
24	1.0 kΩ	2.2 kΩ	0.47 μF/25V
110	10 kΩ	10 kΩ	0.47 μF/25V
220	22 kΩ	22 kΩ	0.47 μF/25V

FOR SUPPLY VOLTAGE FREQUENCY OF 400Hz REDUCE C_{ST} TO .047μF/25V.

**Necessary with inductive loads.

***The sensor resistance will determine the values of the bridge resistors. For the values of R_{DR} shown, the total current into the bridge should not exceed 5mA at 20V.

ZERO CROSSING CIRCUIT WITH DC SUPPLY

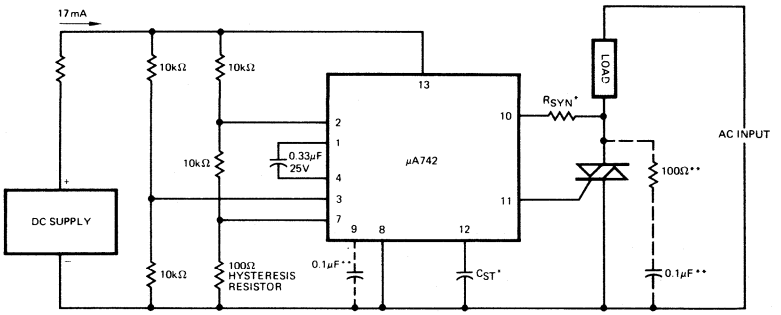


Fig. 1

ZERO CROSSING CIRCUIT

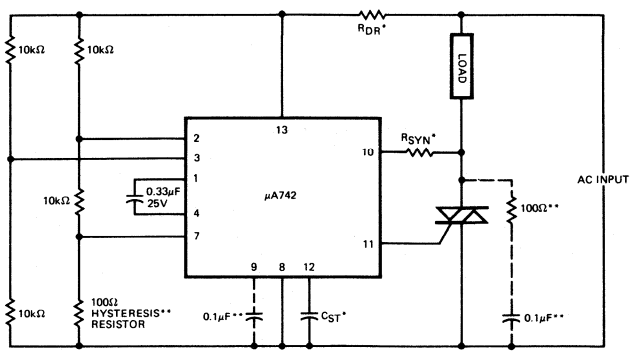


Fig. 2

TYPICAL APPLICATIONS FOR μA742 (Cont'd)

SCR – HALF WAVE

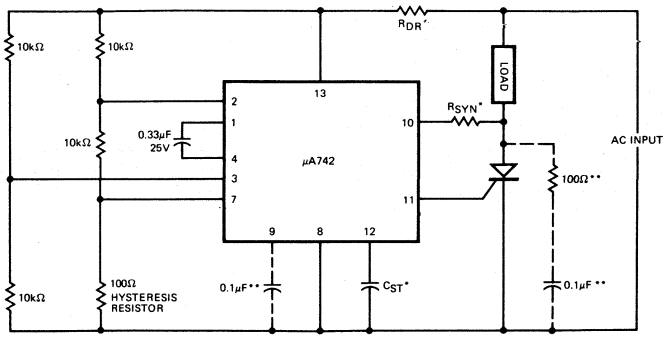


Fig. 3

INVERSE PARALLEL SCR PAIR FIRING WITH A PULSE TRANSFORMER

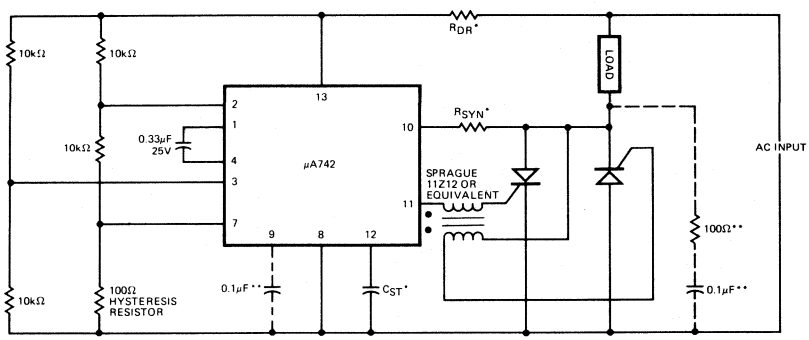


Fig. 4

INVERSE PARALLEL SCR PAIR FIRING WITH A THIRD SCR

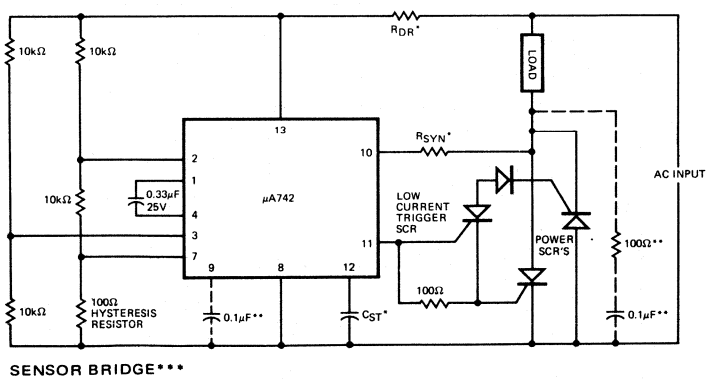


Fig. 5

TYPICAL APPLICATIONS FOR μA742 (Cont'd)

ZERO CROSSING WITH PROPORTIONAL CONTROL

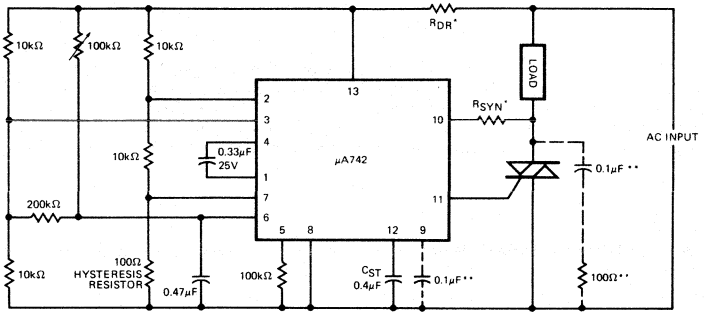


Fig. 6

ZERO CROSSING CONTROL CIRCUIT WITHOUT HYSTERESIS

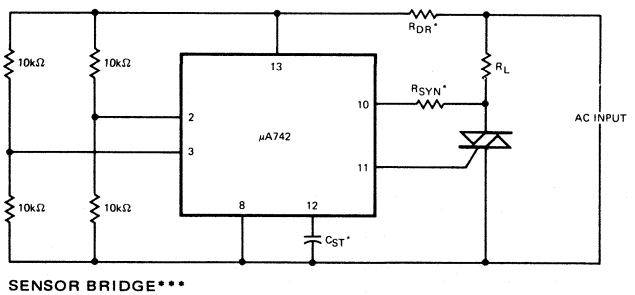


Fig. 7

μA757

GAIN CONTROLLED IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

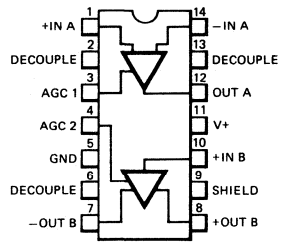
GENERAL DESCRIPTION – The μA757 is a monolithic high performance, Gain Controlled IF Amplifier constructed using the Fairchild Planar* epitaxial process. The amplifier contains two sections which may be operated independently, or in cascade, from audio frequencies to 25 MHz. The μA757 is intended primarily as a gain controlled, intermediate frequency amplifier in AM and FM communications receivers. It also has excellent performance when operated in FM receivers as a limiting amplifier.

- **70 dB GAIN AT 10.7 MHz**
- **70 dB AGC RANGE AT 10.7 MHz**
- **300 mV SIGNAL HANDLING CAPABILITY AT INPUT**
- **CONSTANT INPUT AND OUTPUT IMPEDANCE WITH AGC**
- **STABLE GAIN WITH SUPPLY VOLTAGE AND TEMPERATURE AT ALL LEVELS OF GAIN REDUCTION.**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+15V
Voltage at any Output Terminal	+24V
Voltage at either AGC Terminal (Note 1)	±12V
Differential Voltage at either Input (Pins 1 and 14, Pins 2 and 10)	±5V
Internal Power Dissipation (Note 2)	670 mW
Storage Temperature Range	
Hermetic DIP (μA757, μA757C)	−65°C to +150°C
Operating Temperature Range	
Military (μA757)	−55°C to +125°C
Commercial (μA757C)	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 s) μA757	300°C

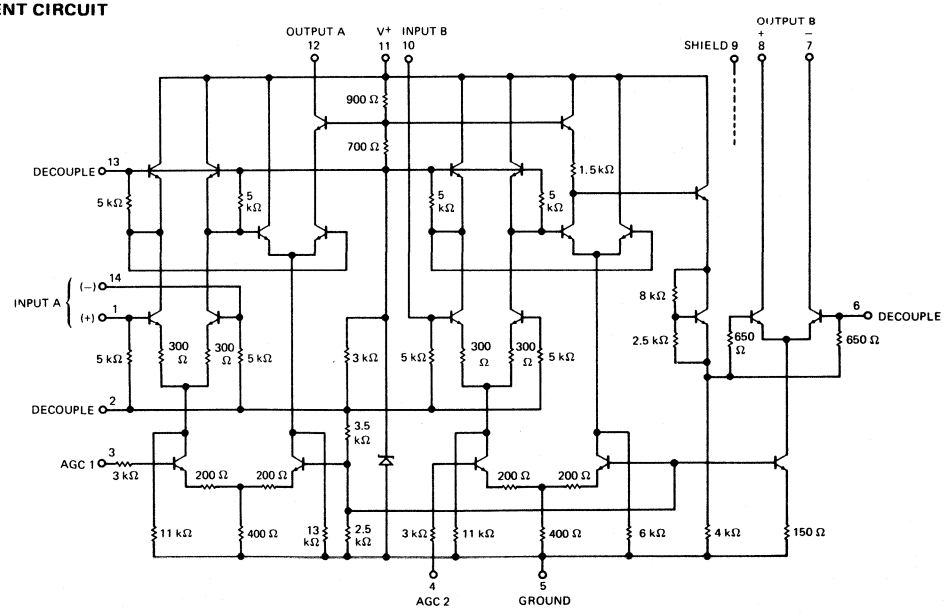
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA757	μA757DM
μA757C	μA757DC

EQUIVALENT CIRCUIT



Notes on following pages.

*Planar is a patented Fairchil process.

μA757

ELECTRICAL CHARACTERISTICS (V_+ = +12 V, T_A = 25°C, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		13	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V	1		170	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2}$ = +1.7 V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal f_1 = 500 kHz, e_1 = 100 mV f_2 = 510 kHz, e_2 = 100 mV I_{OUT} = 1 mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1}$ = +0.8 V, f = 500 kHz			14		mmho
	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.25	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	V
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz			8.0		dB
	R_S = 1.0 kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, f_c = 500 kHz Interfering signal, f_i = 510 kHz I_{OUT} = 0.5 mA p-p, $V_{AGC\ 1}$ = +0.8 V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2}$ = +0.8 V, f = 500 kHz			440		mmho
	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			5.0	6.0	V
Power Supply Sensitivity	V_S = 12 V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

13

μA757

ELECTRICAL CHARACTERISTICS (V_+ = +12 V, T_A = +125°C, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		14	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V	1		170	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2	55	71		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2		62		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		35		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		−1.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.4	V
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.7	2.8	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		3.8	5.6	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			6.0	7.0	V

μA757

ELECTRICAL CHARACTERISTICS (V_+ = +12 V, T_A = −55°C, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		10	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			14	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V	1		120	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			170	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2	55	68		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2		64		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		28		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		−3.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		30	70	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	V
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.0	1.7	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		2.3	3.4	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			4.0	6.0	V

μA757C

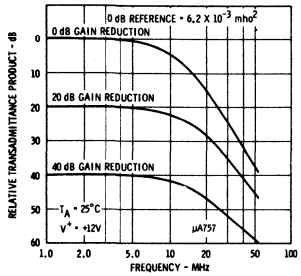
ELECTRICAL CHARACTERISTICS (V_+ = +12 V, T_A = +25°C, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		14	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			18	22	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8V	1		170	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			220	270	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8V , f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2}$ = +1.7 V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal f_1 = 500 kHz, e_1 = 100 mV f_2 = 510 kHz, e_2 = 100 mV I_{OUT} = 1 mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1}$ = +0.8 V, f = 500 kHz			14		mmho
	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.25	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	V
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz			8.0		dB
	R_S = 1.0 kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, f_c = 500 kHz Interfering signal, f_i = 510 kHz I_{OUT} = 0.5 mA p-p, $V_{AGC\ 1}$ = +0.8 V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2}$ = +0.8 V, f = 500 kHz			440		mmho
	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			5.0	6.0	V
Power Supply Sensitivity	V_S = 12 V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

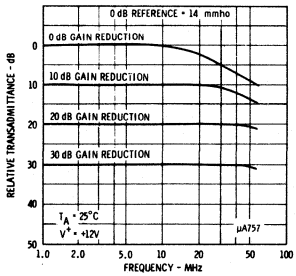
13

TYPICAL PERFORMANCE CURVES FOR μA757 AND μA757C

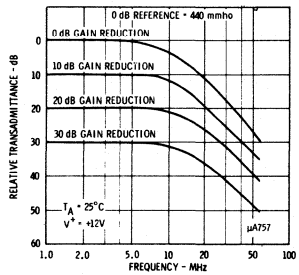
PRODUCT OF SECTIONS 1 AND 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



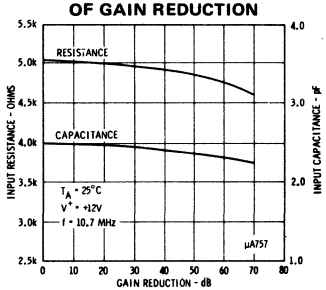
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



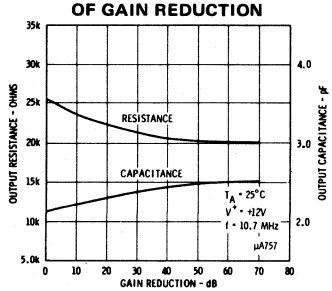
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



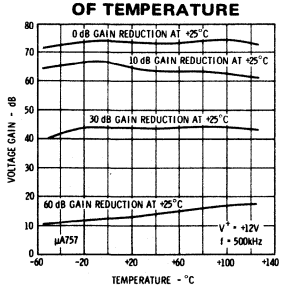
SECTION 1 AND 2 INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



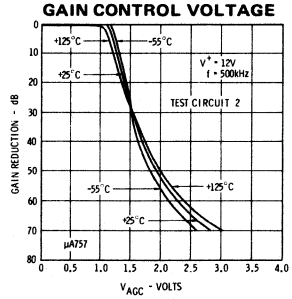
SECTION 2 OUTPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



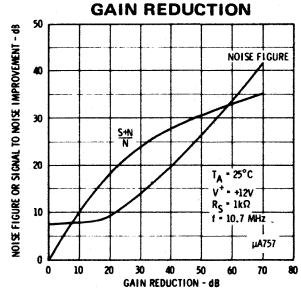
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



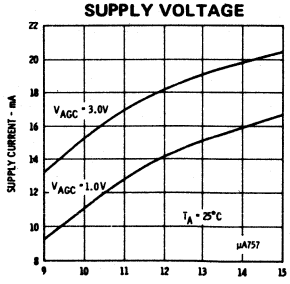
GAIN REDUCTION AS A FUNCTION OF GAIN CONTROL VOLTAGE



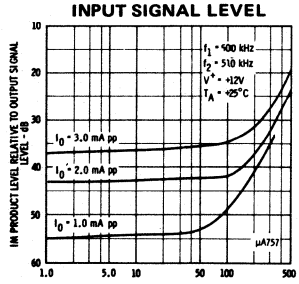
SIGNAL TO NOISE RATIO IMPROVEMENT AND NOISE FIGURE AS A FUNCTION OF GAIN REDUCTION



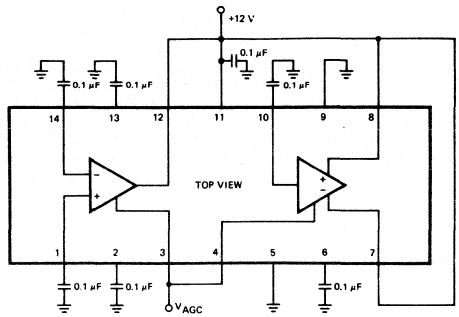
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



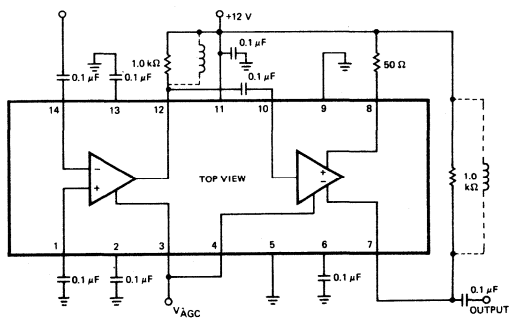
TWO TONE IM DISTORTION PRODUCTS AS A FUNCTION OF INPUT SIGNAL LEVEL



TEST CIRCUIT 1 (NOTE 3)



TEST CIRCUIT 2 (NOTE 2)



NOTES

1. For supply voltages less than +12 V, the absolute maximum voltage at either AGC terminal is equal to the supply voltage.
2. Rating applies to ambient temperatures up to 70° C. Above 70° C ambient derate linearly at 8.3 mW/° C.
3. For 10.7 MHz measurements, interstage capacitance and Section 2 output capacitance are tuned out. Pin 9 should be connected to GND.

13

μA796

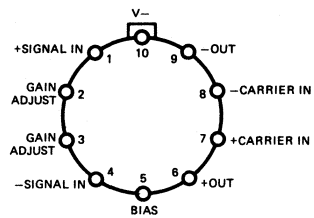
DOUBLE-BALANCED MODULATOR/DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA796 is a monolithic Double-Balanced Modulator/Demodulator using the Fairchild Planar* epitaxial process. This circuit produces an output voltage which is the product of an input voltage (signal) and a switching function (carrier). Communications applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Signal conditioning techniques possible include frequency doubling and halving, linear mixing and chopping, with additional uses as phase detectors in phase locked loops and as differentiators in NRZ and phase encoded digital tape and disk memories.

- **EXCELLENT CARRIER SUPPRESSION**
- **LOW OFFSETS AND DRIFT**
- **FULLY BALANCED INPUTS AND OUTPUT**
- **USEFUL TO 100 MHz**
- **WIDE RANGE OF APPLICATION**

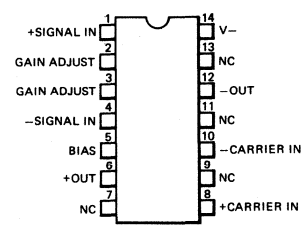
CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA796C	μA796HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



ORDER INFORMATION

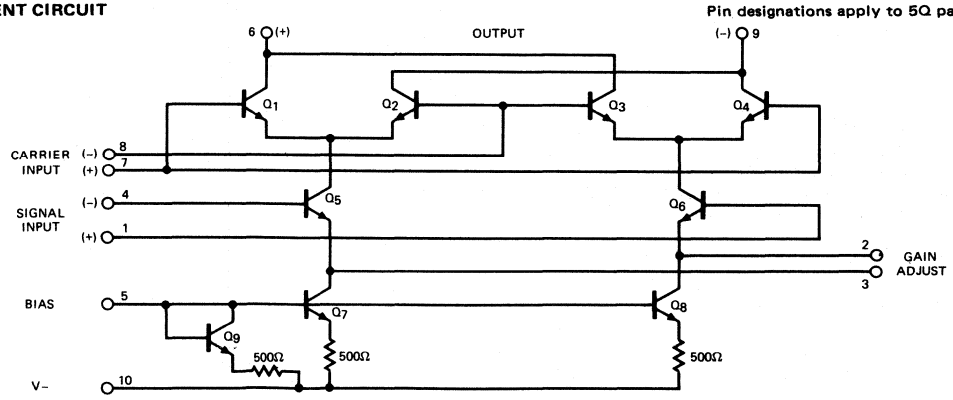
TYPE	PART NO.
μA796C	μA796PC

ABSOLUT MAXIMUM RATINGS

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30 V
Differential Input Signal ($V_7 - V_8$)	±5.0 V
Differential Input Signal ($V_4 - V_1$)	$\pm(5 + I_5R_e)$ V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0 V
Bias Current (I_5)	12 mA
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 s)	300°C

EQUIVALENT CIRCUIT

Pin designations apply to 5Q package only



Notes on following pages.

*Planar is a patented Fairchild process.

μA796C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Figure 1 unless otherwise specified)

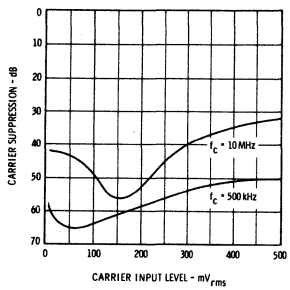
PARAMETER	CONDITIONS (Pin designations apply to metal can package only)	MIN	TYP	MAX	UNITS
Carrier Feedthrough	V_C = 60 mV (rms) sine wave f_C = 1.0 kHz, offset adjusted		40		μV rms
	V_C = 60 mV (rms) sine wave f_C = 10 MHz, offset adjusted		140		μV rms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2	mV rms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset not adjusted		20	150	mV rms
Carrier Suppression	f_S = 10 kHz, 300 mV (rms) f_C = 500 kHz, 60 mV (rms) sine wave offset adjusted	50	65		dB
	f_S = 10 kHz, 300 mV (rms) f_C = 10 MHz, 60 mV (rms) sine wave offset adjusted		50		dB
Transadmittance Bandwidth	R_L = 50Ω Carrier Input Port, V_C = 60 mV (rms) sine wave f_S = 1.0 kHz, 300 mV (rms) sine wave		300		MHz
	Signal Input Port, V_S = 300 mV (rms) sine wave $V_7 - V_8$ = 0.5 V dc		80		MHz
Voltage Gain, Signal Channel	V_S = 100 mV (rms), f = 1.0 kHz $V_7 - V_8$ = 0.5 V dc	2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		2.0		pF
Single Ended Output Resistance	f = 10 MHz		40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	30	μA
	$(I_7 + I_8)/2$		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	$0°C \leq T_A \leq +70°C$		2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$		14	60	μA
Average Temperature Coefficient of Output Offset Current	$0°C < T_A < +70°C$		90		nA/°C
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 V dc		-85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

NOTES
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C.
2. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

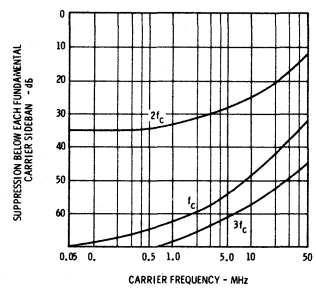
13

TYPICAL PERFORMANCE CURVES FOR μA796C

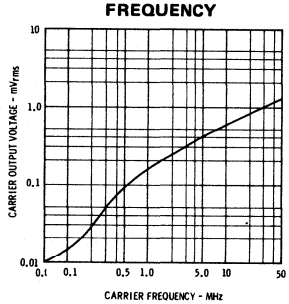
CARRIER SUPPRESSION AS A FUNCTION OF CARRIER INPUT LEVEL



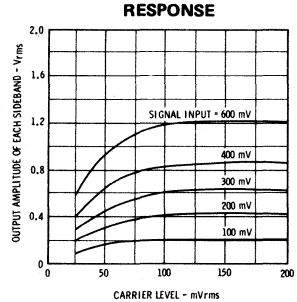
CARRIER SUPPRESSION AS A FUNCTION OF FREQUENCY



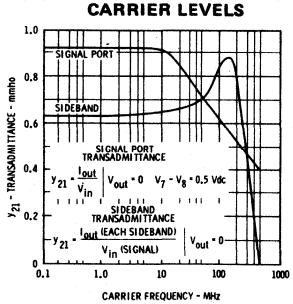
CARRIER FEEDTHROUGH AS A FUNCTION OF FREQUENCY



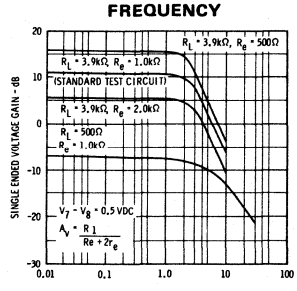
SIGNAL-PORT FREQUENCY RESPONSE



SIDEBAND OUTPUT AS A FUNCTION OF CARRIER LEVELS

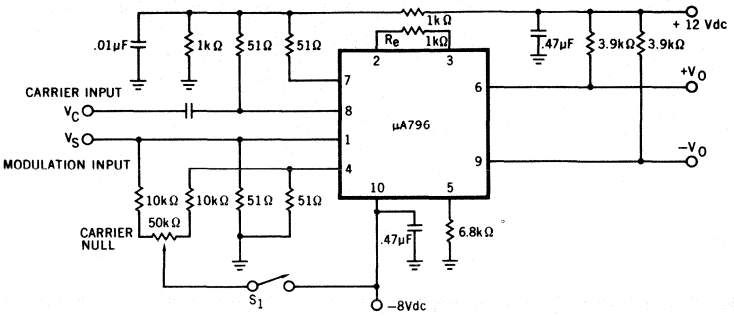


SIDEBAND AND SIGNAL PORT TRANSADMITTANCES AS A FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

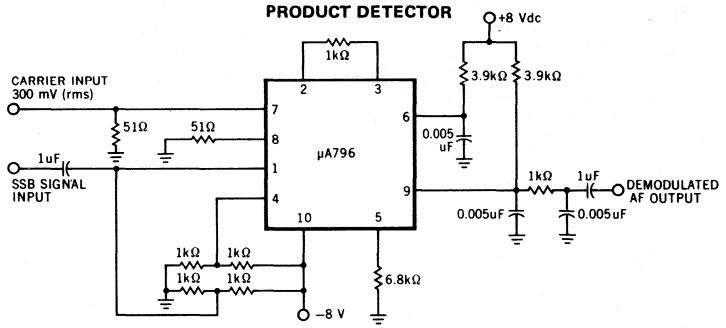
TYPICAL MODULATOR CIRCUIT



Note: S_1 is closed for "adjusted" measurements.

Fig. 1

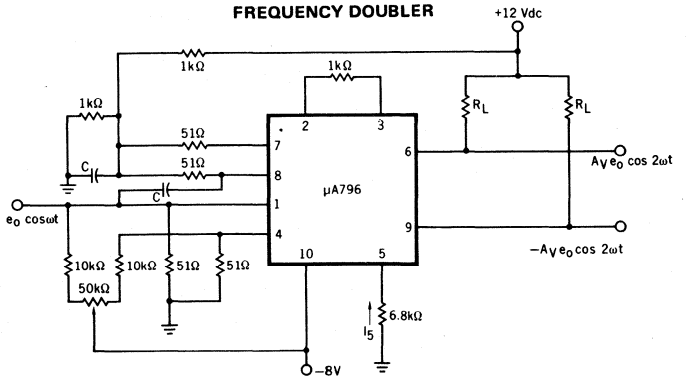
PRODUCT DETECTOR



This figure shows the μA796 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mV(rms) is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mV(rms). All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Fig. 2

FREQUENCY DOUBLER



The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

Fig. 3

μA2240

PROGRAMMABLE TIMER/COUNTER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

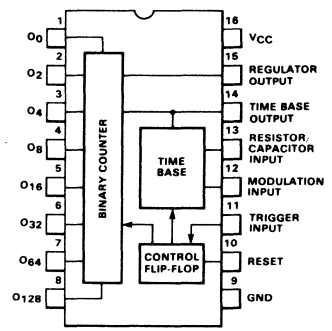
GENERAL DESCRIPTION – The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital system. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **ACCURATE TIMING FROM MICROSECONDS TO DAYS**
- **PROGRAMMABLE DELAYS FROM 1 RC TO 255 RC**
- **TTL, DTL AND CMOS COMPATIBLE OUTPUTS**
- **TIMING DIRECTLY PROPORTIONAL TO RC TIME CONSTANT**
- **HIGH ACCURACY – 0.5%**
- **EXTERNAL SYNC AND MODULATION CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **EXCELLENT SUPPLY VOLTAGE REJECTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5 mA
Maximum Power Dissipation, Note 1	
Package Code D (Ceramic)	750 mW
Code P (Plastic)	650 mW
Operating Temperature Range Package	
Military (μA2240)	−55°C to +125°C
Commercial (μA2240C)	0°C to 70°C

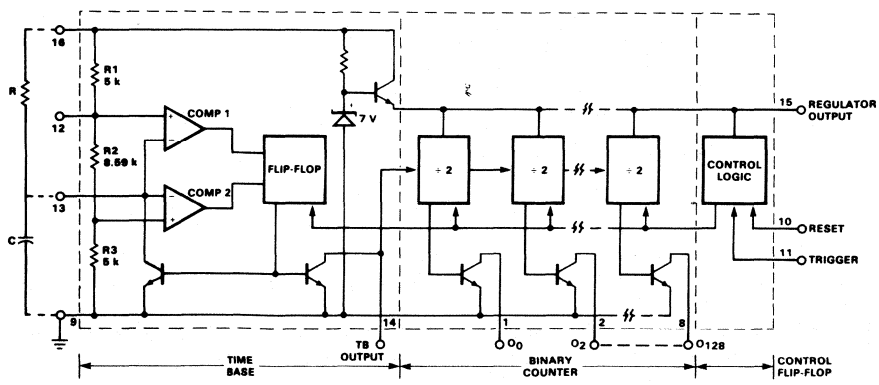
CONNECTION DIAGRAM
16-PIN DIP (TOP VIEW)
PACKAGE OUTLINES 7B, 9B
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA2240	μA2240DM
μA2240C	μA2240DC
μA2240C	μA2240PC

BLOCK DIAGRAM



NOTE 1: Above 25°C ambient derate linearly at 6.2 mW/°C for Package Code D and at 5.3 mW/°C for Package Code P.

ELECTRICAL CHARACTERISTICS: (See Test Circuit Fig. 28, V_{CC} = 5 V, T_A = 25°C, R = 10 kΩ, C = 0.1 μF, unless otherwise noted)

PARAMETER	CONDITIONS	μA2240			μA2240C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GENERAL CHARACTERISTICS								
Supply Voltage	For $V_{CC} \leq$ 4.5 V, Short Pin 15 to Pin 16	4		15	4		15	V
Supply Current								
Total Circuit	V_{CC} = 5 V, V_{TR} = 0, V_{RS} = 5 V		3.5	6		4	7	mA
	V_{CC} = 15 V, V_{TR} = 0, V_{RS} = 5 V		12	16		13	18	mA
Counter Only	See Test Circuit, Figure 29		1			1.5		mA
Regulator Output, V_{REG}	Measured at Pin 15, V_{CC} = 5 V	4.1	4.4		3.9	4.4		V
	V_{CC} = 15 V, See Test Circuit, Figure 30	6.0	6.3	6.6	5.8	6.3	6.8	V
TIME BASE SECTION								
Timing Accuracy (Note 2)	V_{RS} = 0, V_{TR} = 5 V		0.5	2.0		0.5	5	%
Temperature Drift	V_{CC} = 5 V, 0°C $\leq T_J \leq$ 75°C		150	300		200		ppm/°C
	V_{CC} = 15 V		80			80		ppm/°C
Supply Drift	$V_{CC} \geq$ 8 V, See Figure 23		0.05	0.2		0.08	0.3	%/V
Max Frequency	R = 1 kΩ, C = 0.007 μF	100	130			130		kHz
Modulation Voltage Level	Measured at Pin 12 V_{CC} = 5 V	3.00	3.50	4.0	2.80	3.50	4.20	V
	V_{CC} = 15 V		10.5			10.5		V
Recommended Range of Timing Components	See Figure 20							
Timing Resistor, R		0.001		10	0.001		10	MΩ
Timing Capacitor, C		0.007		1000	0.01		1000	μF
TRIGGER/RESET CONTROLS								
Trigger	Measured at Pin 11, V_{RS} = 0							
Trigger Threshold			1.4	2.0		1.4	2.0	V
Trigger Current	V_{RS} = 0, V_{TR} = 2 V		8			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			1			1		μs
Reset	Measured at Pin 10, V_{TR} = 0							
Reset Threshold			1.4	2.0		1.4	2.0	V
Reset Current	V_{TR} = 0, V_{RS} = 2 V		8			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			0.8			0.8		μs
COUNTER SECTION	See Test Circuit, Figure 30							
Max Toggle Rate	V_{RS} = 0, V_{TR} = 5 V Measured at Pin 14	0.8	1.5			1.5		MHz
Input Impedance			20			20		kΩ
Input Threshold		1.0	1.4		1.0	1.4		V
Output:	Measured at Pins 1 through 8							
Rise Time	R_L = 3 kΩ, C_L = 10 pF		180			180		ns
Fall Time			180			180		ns
Sink Current	$V_{OL} \leq$ 0.4 V	3	5		2	4		mA
Leakage Current	V_{OH} = 15 V		0.01	8		0.01	15	μA

NOTES:
2. Timing error solely introduced by μA2240, measured as % of ideal time base period of T = 1.00 RC.
3. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

FUNCTIONAL DESCRIPTION

(Figure 1 and Block Diagram, page 1)

When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive-going trigger pulse to TRIG, pin 11, initiates the timing cycle. The Trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive-going reset pulse is applied to R, pin 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a Reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

In most timing applications, one or more of the counter outputs are connected to the Reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the Reset terminal (switch S1 open), the circuit operates in an astable or free-running mode, following to a trigger input.

Important Operating Information

- Ground connection is pin 9.
- Reset R (pin 10) sets all outputs HIGH.
- Trigger TRIG (pin 11) sets all outputs LOW.
- Time-base TBO (pin 14) can be disabled by bringing the RC input (pin 13) LOW via a 1 k resistor.
- Normal Time-base Output TBO (pin 14) is a negative-going pulse greater than 500 ns.

  Note: Under the conditions of high supply voltages (V_{CC} > 7 V) and low values of timing capacitor (C < 0.1 μF, the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from TBO (pin 14) to ground (pin 9).
- Reset (pin 10) stops the time-base oscillator.
- Outputs $O_0 \ldots O_{128}$ (pins 1-8) sink 2 mA current with $V_{OL} \leqslant 0.4$ V.
- For use with external clock, minimum clock pulse amplitude should be 3 V, with greater than 1 μs pulse duration.

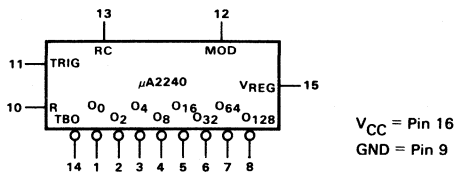


Fig. 1. Logic Diagram

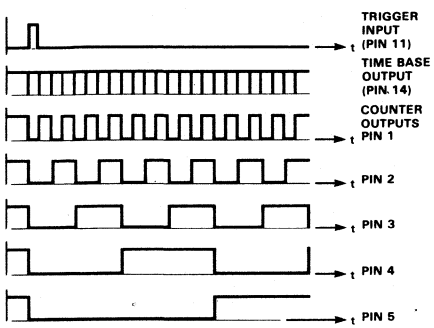


Fig. 2. Timing Diagram of Output Waveforms

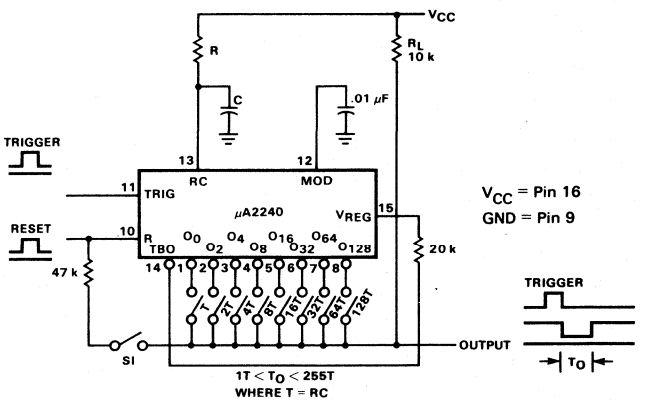


Fig. 3. Basic Circuit Connection for Timing Applications
Monostable: S1 Closed
Astable: S1 Open

CIRCUIT CONTROLS

Counter Outputs (O_0 . . . O_{128}, pins 1 thru 8)

The binary counter outputs are buffered open-collector type stages, as shown in the block diagram on page 1. Each output is capable of sinking 2 mA at 0.4 V V_{OL}. In the Reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the Programming section.

Reset and Trigger Inputs (R and TRIG, pins 10 and 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these controls is approximately two diode drops (≈ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in *Figure 22*. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, pin 12)

The oscillator time-base period, T, can be modulated by applying a dc voltage to MOD, pin 12 (see *Figure 25*). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12, as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

The time base can be synchronized by setting the time-base period T to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m)$$

where

$$m \text{ is an integer, } 1 \leq m \leq 10$$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

RC Terminal (pin 13)

The time-base period T is determined by the external RC network connected to RC, pin 13. When the time base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC.

Time-Base Output (TBO, pin 14)

The time-base output is an open-collector type stage as shown in the block diagram, page, 1, and requires a 20 kΩ pull-up resistor to pin 15 for proper circuit operation. In the Reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary-counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is ≈ +1.4 V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

When using high supply voltages ($V_{CC} > 7$ V) and a small-value timing capacitor ($C < 0.1$ μF), the pulse width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

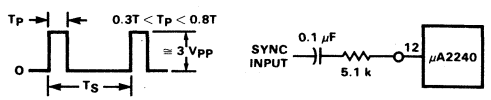


Fig. 4. Operation with External Sync. Signal

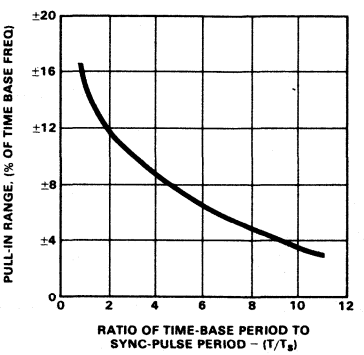


Fig. 5. Typical Pull-in Range for Harmonic Synchronization

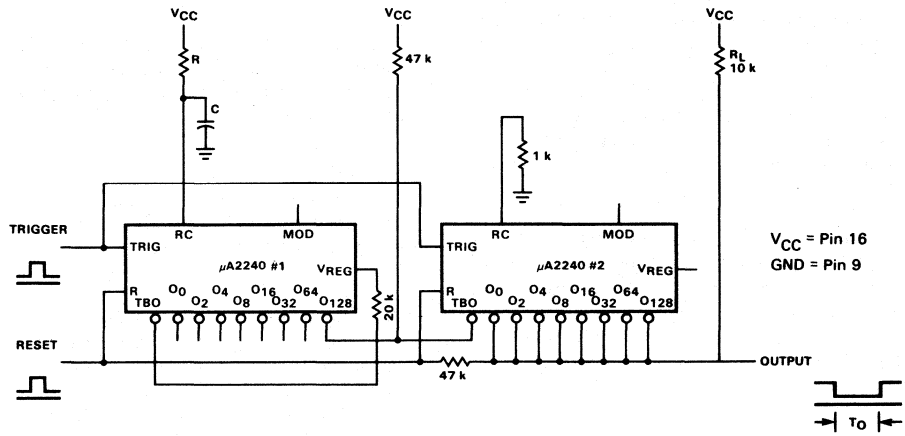


Fig. 6. Cascaded Operation for Long Delays

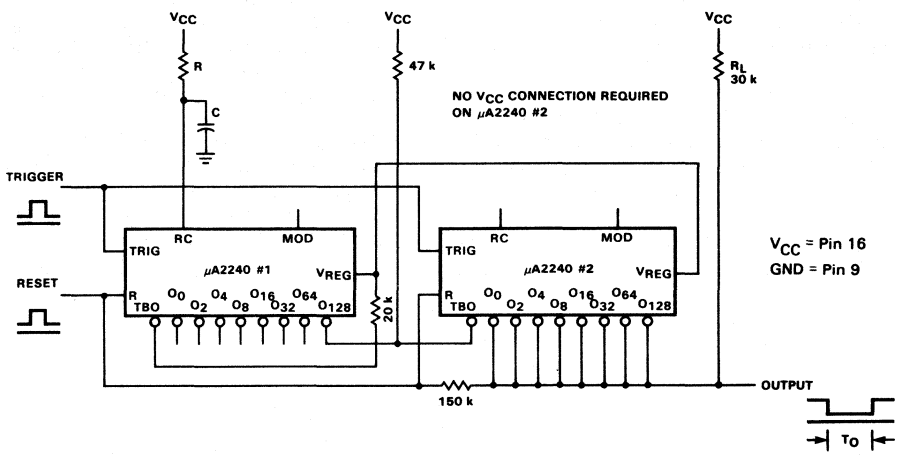


Fig. 7. Low Power Operation of Cascaded Timers

Regulator Output (V_{REG}, pin 15)

The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded (see *Figure 7*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, pin 15 should be shorted to pin 16.

MONOSTABLE OPERATION

Precision Timing

In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3*. The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration, T_O, and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC pin 13 (see *Figure 21*) and N is an integer in the range of $1 \leqslant N \leqslant 255$ as determined by the combination of counter outputs $O_0 \ldots O_{128}$, pins 1 through 8, connected to the output bus.

Counter-Output Programming

The binary-counter outputs, $O_0 \ldots O_{128}$, pins 1 through 8 are open-collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)T = 49$ T. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\ T \leqslant T_O \leqslant 255\ T$.

Ultra Long Time-Delay Application

Two μA2240 units can be cascaded as shown in *Figure 6* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the Reset and the Trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 7*. In this case, the V_{CC} terminal (pin 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (pins 15) of both units together.

ASTABLE OPERATION

The μA2240 can be operated in its astable or free-running mode by disconnecting the Reset terminal (pin 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free-running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its Reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely. in astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Binary Pattern Generation

In astable operation, as shown in *Figure 8*, the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some

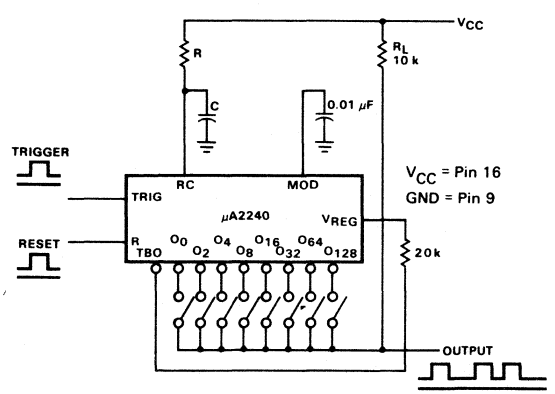


Fig. 8. Operation with External Trigger and Reset Inputs

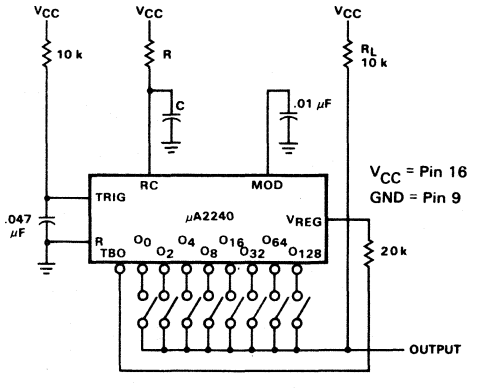


Fig. 9. Free-Running or Continuous Operation

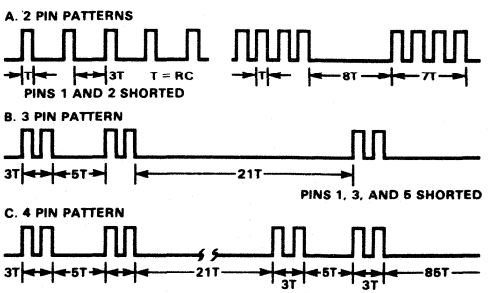


Fig. 10. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

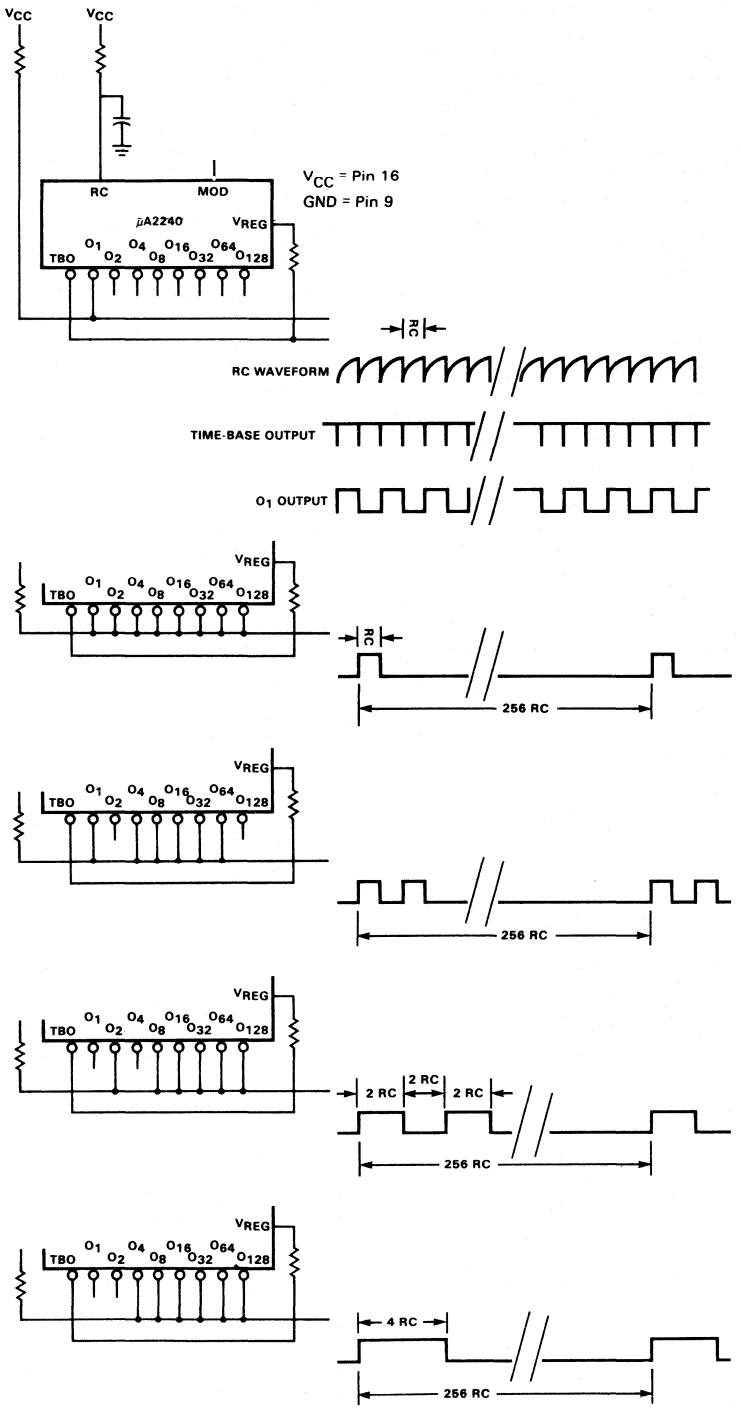


Fig. 11. Continuous Free-run Operation Examples of Output

of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

OPERATION WITH EXTERNAL CLOCK

The μA2240 can be operated with an external clock or time base by disabling the internal time-base oscillator and applying the external clock input to TBO, pin 14. The recommended circuit connection for this application is shown in *Figure 12*. The internal time base is de-activated by connecting a 1 kΩ resistor from RC, pin 13, to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 V is required. Minimum external clock pulse width must be ≥ 1 μs.

For low power operation with supply voltages of 6 V or less, the internal time base section can be powered down by connecting V_{CC} to pin 15 and leaving pin 16 open. In this configuration, the internal time base does not draw any current and the overall current drain is reduced by ≈ 3 mA.

FREQUENCY SYNTHESIZER

The programmable counter section of the μA2240 can be used to generate 255 discrete frequencies from a given time-base output setting using the circuit connection of *Figure 13*. The circuit output is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter. The modulus N is the total count corresponding to the counter outputs connected to the output bus. For example, if pins 1, 3 and 4 are connected together to the output bus, the total count is N = 1 + 4 + 8 = 13; and the period of the output waveform is equal to (N + 1) T or 14 T. In this manner, 255 different frequencies can be synthesized from a given time-base setting.

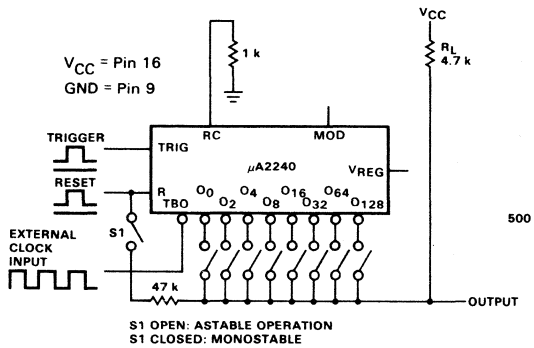


Fig. 12. Operation with External Clock

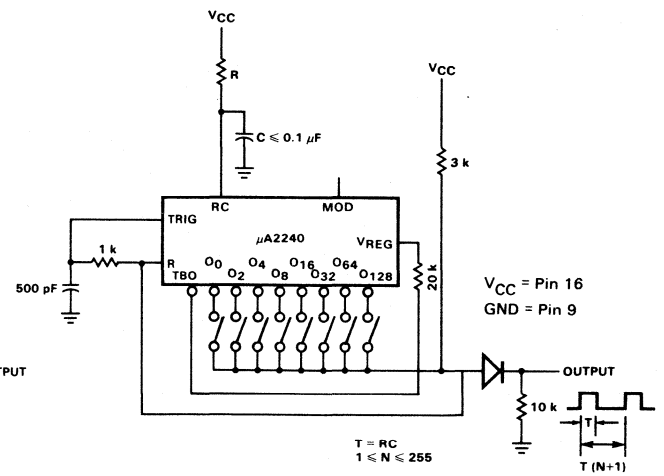


Fig. 13. Frequency Synthesis from Internal Time-Base

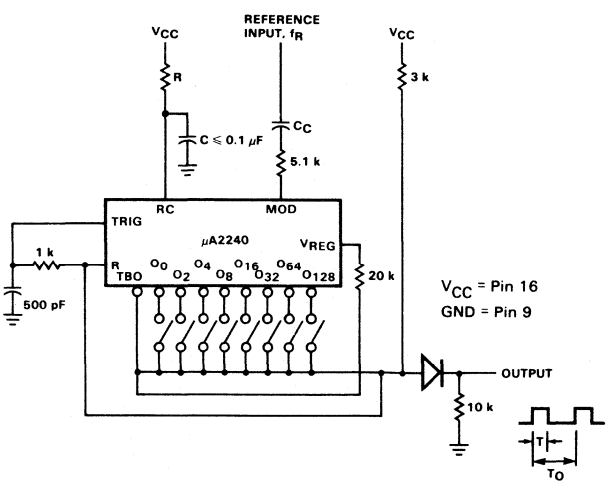


Fig. 14. Frequency Synthesis by Harmonic Locking to an External Reference

SYNTHESIS WITH HARMONIC LOCKING

The harmonic synchronization feature of the μA2240 time base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in *Figure 14* (see *Figures 4* and *5* for external sync waveform and harmonic capture range). If the time base is synchronized to (m)th harmonic of input frequency where $1 \leqslant m \leqslant 10$, the frequency f_O of the output waveform in *Figure 14* is related to the input reference frequency f_R as

$$f_O = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leqslant N \leqslant 255$, the circuit of *Figure 14* can produce 2550 different frequencies from a single fixed reference.

The circuit of *Figure 14* can be used to generate frequencies which are not harmonically related to a reference input. For example, by selecting the external RC to set m = 10 and setting N = 5, a 100 Hz output frequency synchronized to 60 Hz power line frequency can be obtained.

STAIRCASE GENERATOR

The μA2240 timer/counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator as shown in *Figure 15*. Under Reset condition, the output is LOW. When a trigger is applied, the op amp output goes HIGH and generates a negative-going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any level by applying a disable signal to pin 14, through a steering diode, as shown in *Figure 15*. The count is stopped when pin 14 is clamped at a voltage level $\leqslant$ 1.0 V.

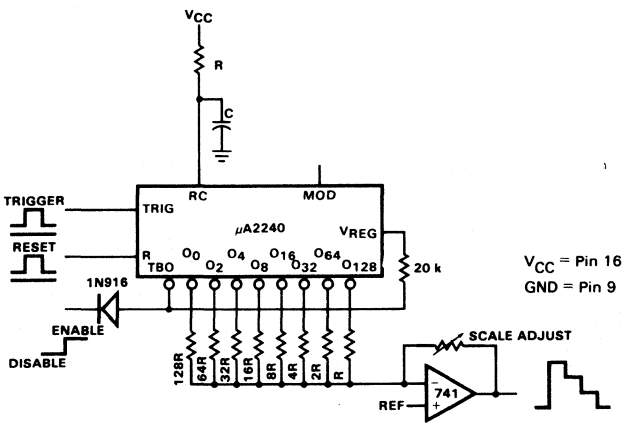


Fig. 15. Staircase Generator

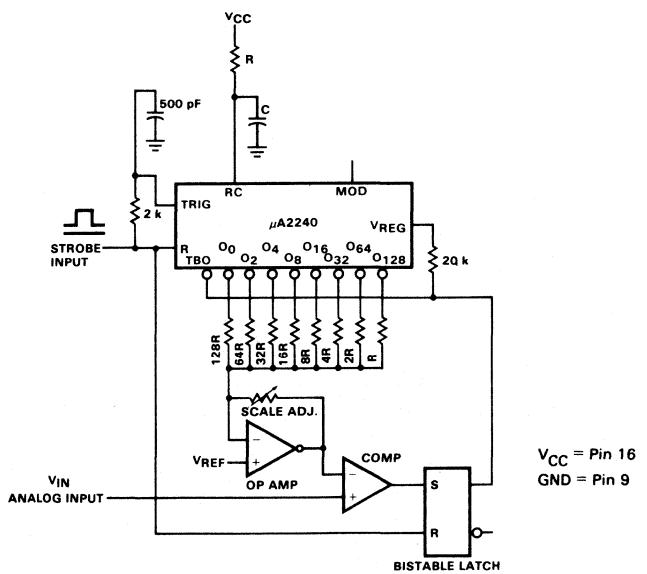


Fig. 16. Digital Sample and Hold Circuit

DIGITAL SAMPLE AND HOLD

Figure 16 shows a digital sample and hold circuit using the μA2240. Circuit operation is similar to the staircase generator described in the previous section. When a strobe input is applied, the RC low-pass network between the Reset and the Trigger inputs resets the timer, then triggers it. This strobe input also sets the output of the bistable latch to a HIGH state and activates the counter.

The circuit generates a staircase voltage at the op amp output. When the level of the staircase reaches that of the analog input to be sampled, the comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op amp output corresponds to the sampled analog input. Once the input is sampled, it is held until the next strobe signal. Minimum recycle time of the system is ≈ 6 ms.

ANALOG-TO-DIGITAL CONVERTER

Figure 17 shows a simple 8-bit A/D converter system using the μA2240. Circuit operation is very similar to that of the digital sample and hold system of *Figure 16*. In the case of A/D conversion, the digital output is obtained in parallel format from the binary-counter outputs with the output at pin 8 corresponding to the most significant bit (MSB). Recycle time is ≈ 6 ms.

DIGITAL TACHOMETER TIME BASE

A digital tachometer requires a time-base generator to supply two pulse outputs at specific intervals, *e.g.*, every second. The first pulse is a command (load) to transfer the accumulated counts in the counter section into latches (memory); the second resets the counter to zero. A simple adjustable time base, accurate to approximately ±0.5%, can be implemented using the circuit in *Figure 18*.

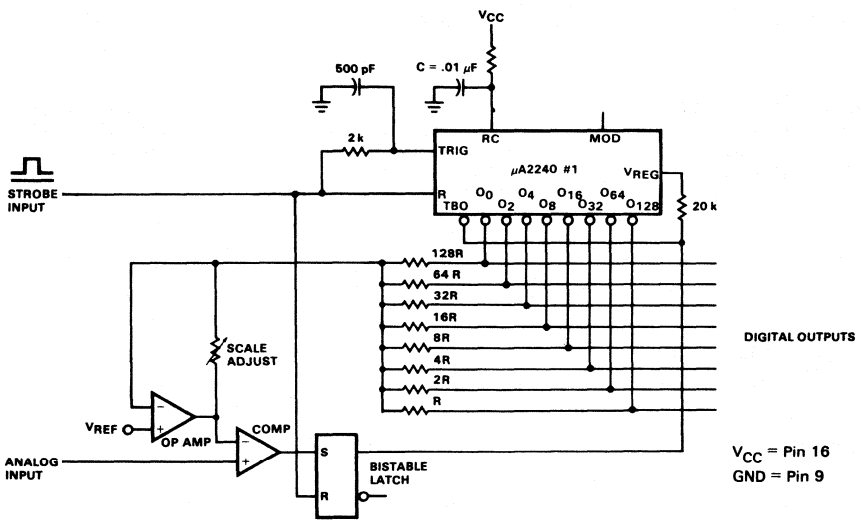


Fig. 17. Analog-to-Digital Converter

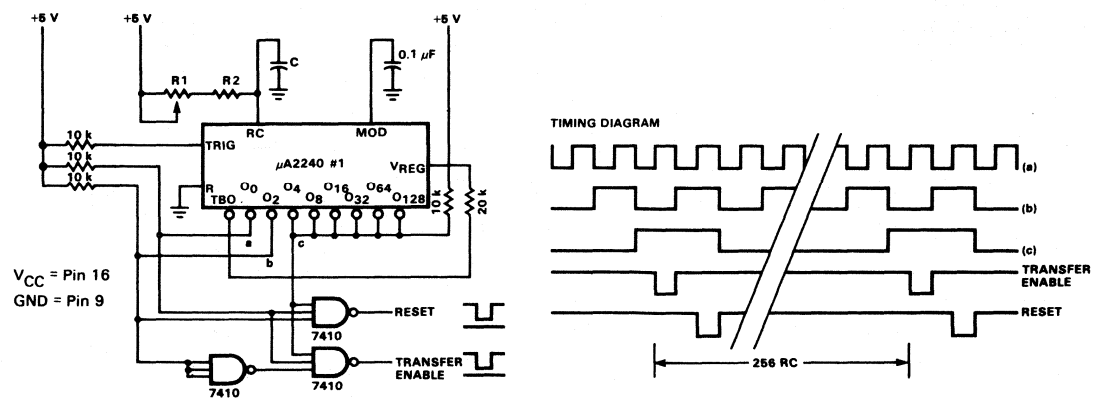


Fig. 18. Simple Time Generator for a Digital Tachometer

TYPICAL ELECTRICAL CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE IN RESET CONDITION

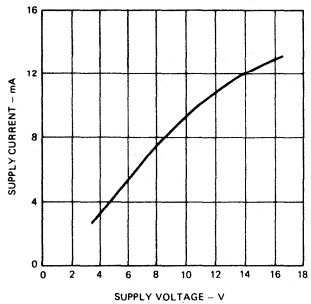


Fig. 19

RECOMMENDED RANGE OF TIMING COMPONENT VALUES

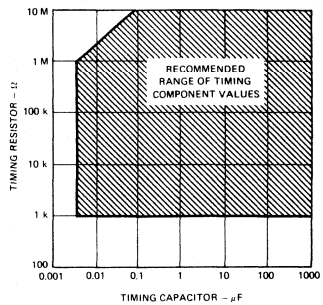


Fig. 20

TIME BASE PERIOD AS A FUNCTION OF EXTERNAL RC

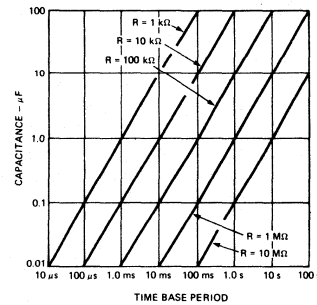


Fig. 21

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AND RESET AMPLITUDE

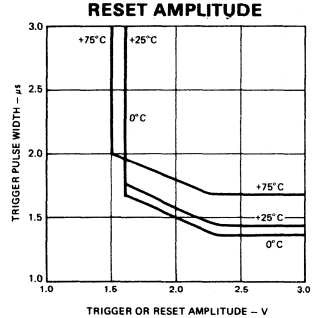


Fig. 22

TIME BASE PERIOD DRIFT AS A FUNCTION OF SUPPLY VOLTAGE

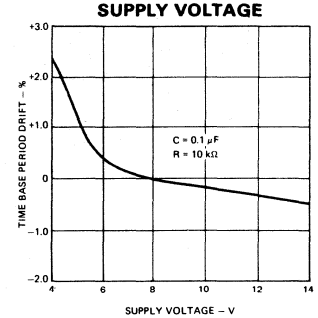


Fig. 23

MINIMUM TRIGGER/RETRIGGER TIMING AS A FUNCTION OF TIMING CAPACITOR

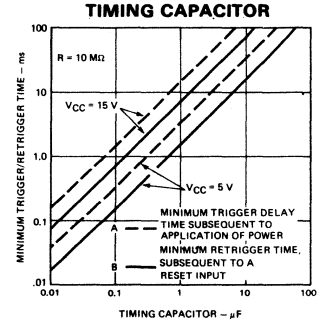


Fig. 24

NORMALIZED CHANGE IN TIME BASE PERIOD AS A FUNCTION OF MODULATION VOLTAGE

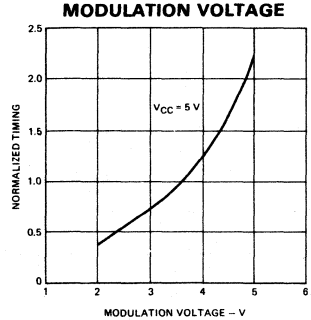


Fig. 25

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

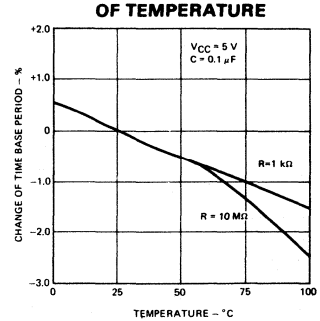


Fig. 26

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

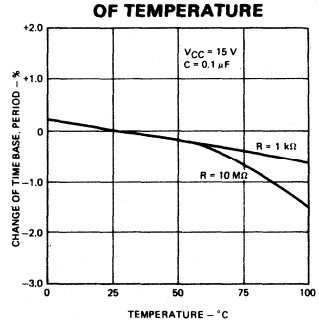


Fig. 27

TEST CIRCUITS

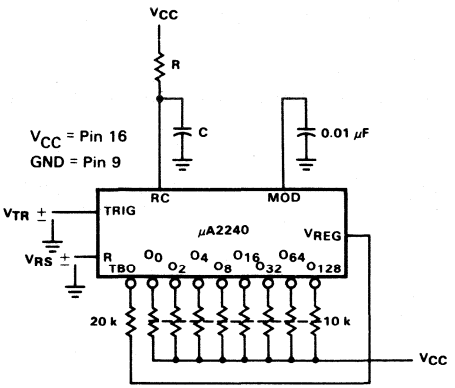


Fig. 28. Generalized Test Circuit

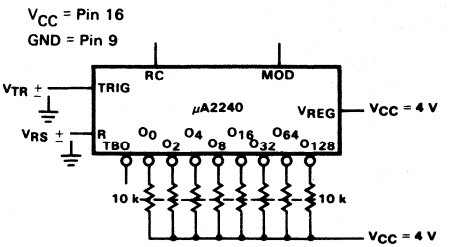


Fig. 29. Test Circuit for Low Power Operation (Time Base Powered Down)

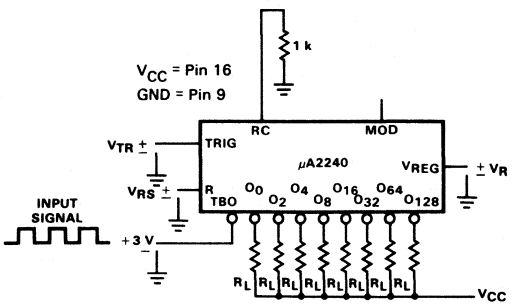


Fig. 30. Test Circuit for Counter Section

μA3018 • μA3018A • μA3019 • μA3026 • μA3036
μA3039 • μA3045 • μA3046 • μA3054 • μA3086

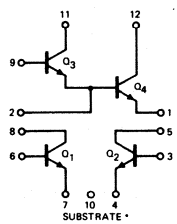
TRANSISTOR AND DIODE ARRAYS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – Fairchild Transistor and Diode Arrays consist of general purpose integrated circuit devices constructed on a single substrate, using the Fairchild Planar* epitaxial process. These arrays are arranged to offer maximum flexibility in circuit design for applications from dc to 120 MHz. Excellent transistor and diode matching and temperature tracking allow circuit techniques unavailable when using discrete devices. Multiple devices in one package permit a greater packing density and cost saving than with individually packaged transistors.

- **PRECISION MONOLITHIC MATCHING**
- **DESIGN FLEXIBILITY**
- **CUSTOM APPLICATIONS**

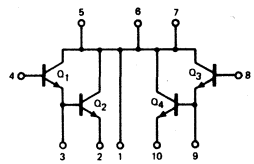
PACAKGE OUTLINE 5D
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3018	μA3018
μA3018A	μA3018AHM

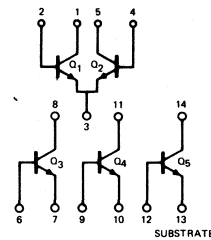
PACKAGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3036	μA3036HM

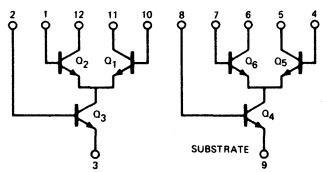
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA3045	μA3045
μA3046	μA3046DC
μA3086	μA3086DM

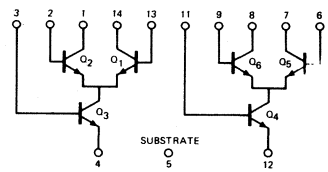
PACKAGE OUTLINE 5D
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3026	μA3026HM

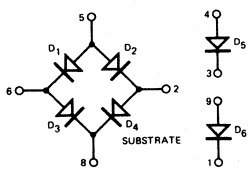
PACAKGE OUTLINE 6A
PACAKGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA3054	μA3054DC

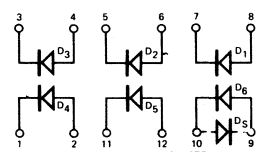
PACAKGE OUTLINE 5Q
PACAKGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3039	μA3039HM

PACAKGE OUTLINE 5D
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3019	μA3019HM

*Planar is a patented Fairchild process.

μA3018/3018A

- **MATCHED MONOLITHIC GENERAL PURPOSE TRANSISTORS**
- **h_{FE} MATCHED ±10%**
- **V_{BE} MATCHED ±2 mV 3018A (±5 mV 3018)**
- **OPERATION FROM DC TO 120 MHz**
- **WIDE OPERATING CURRENT RANGE**
- **3018A PERFORMANCE CHARACTERISTICS CONTROLLED FROM 10 μA TO 10 mA**
- **LOW NOISE FIGURE – 3.2 dB TYPICAL AT 1 kHz**
- **FULL MILITARY TEMPERATURE RANGE CAPABILITY (–55 TO +125°C)**

APPLICATIONS

- General Use in Signal Processing Systems in dc Through VHF Range
- Custom Design Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS

	μA3018	μA3018A
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	450 mW	450 mW
Temperature Range		
Operating Temperature	–55°C to +125°C	–55°C to +125°C
Storage Temperature	–65°C to +200°C	–65°C to +200°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15 V	15 V
Collector-to-Base Voltage, V_{CBO}	20 V	30 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V	40 V
Emitter-to-Base Voltage, V_{EBO}	5 V	5 V
Collector Current, I_C	50 mA	50 mA

13

ELECTRICAL CHARACTERISTICS FOR μA3018 (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CBO}	Collector Cutoff Current	V_{CB} = 10 V, I_E = 0		0.002	100	nA
I_{CEO}	Collector Cutoff Current	V_{CE} = 10 V, I_B = 0		See Curve	5.0	μA
I_{CEOD}	Collector Cutoff Current Darlington Pair	V_{CE} = 10 V, I_B = 0				μA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	15	24		V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5.0	7.0		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	I_C = 10 μA, I_{CI} = 0	20	60		V
V_{CES}	Collector-to-Emitter Saturation Voltage	I_B = 1 mA, I_C = 10 mA		0.23		V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 10 mA I_C = 1 mA I_C = 10 μA	30	100 100 54		
	Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)	V_{CE} = 3 V, I_{C1} = I_{C2} = 1 mA	0.9	0.97		
h_{FED}	Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	V_{CE} = 3 V, I_C = 1 mA I_C = 100 μA	1500	5400		
V_{BE}	Base-to-Emitter Voltage	V_{CE} = 3 V, I_E = 1 mA I_E = 10 mA		0.715 0.800		V
$\lvert V_{BE_1} \rvert$ $\lvert V_{BE_2} \rvert$	Input Offset Voltage	V_{CE} = 3 V, I_E = 1 mA		0.48	5.0	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	V_{CE} = 3 V, I_E = 1 mA		−1.9		mV/°C
V_{BED} ($V_{9\text{-}1}$)	Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{CE} = 3 V, I_E = 10 mA I_E = 1 mA		1.46 1.32		V
$\frac{\Delta V_{BED}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	V_{CE} = 3 V, I_E = 1 mA		4.4		mV/°C
$\frac{V_{BE_1}\text{-}V_{BE_2}}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	V_{CC} = +6 V, V_{EE} = −6 V		10		μV/°C
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source resistance = 1 kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent Circuit Characteristics:					
h_{fe}	Forward Current-Transfer Ratio	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110		
h_{ie}	Short Circuit Input Resistance			3.5		kΩ
h_{oe}	Open Circuit Output Conductance			15.6		μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
	Admittance Characteristics:					
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance			0.3 + j 0.04		mmho
Y_{oe}	Output Admittance			0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance			See Curve		mmho
f_T	Gain-Bandwidth Product	V_{CE} = 3 V, I_C = 3 mA		500		MHz
C_{eb}	Emitter-to-Base Capacitance	V_{EB} = 3 V, I_E = 0		0.6		pF
C_{cb}	Collector-to-Base Capacitance	V_{CB} = 3 V, I_C = 0		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	V_{CI} = 3 V, I_C = 0		2.8		pF

NOTES:

1. Derate at 5 mW/°C for $T_A > 85°C$.
2. Substrate must be connected to the most negative voltage to maintain normal operation.

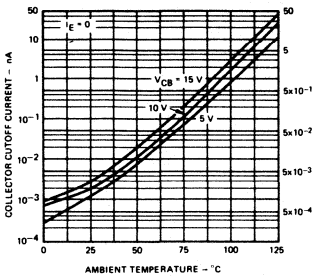
ELECTRICAL CHARACTERISTICS FOR μA3018A (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CBO}	Collector Cutoff Current	V_{CB} = 10 V, I_E = 0		0.002	40	nA
I_{CEO}	Collector Cutoff Current	V_{CE} = 10 V, I_B = 0		See Curve	0.5	μA
I_{CEOD}	Collector Cutoff Current Darlington Pair	V_{CE} = 10 V, I_B = 0			5.0	μA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	15	24		V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	30	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5.0	7.0		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	I_C = 10 μA, I_{CI} = 0	40	60		V
V_{CES}	Collector-to-Emitter Saturation Voltage	I_B = 1 mA, I_C = 10 mA		0.23	0.5	V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 10 mA	50	100		
		V_{CE} = 3 V, I_C = 1 mA	60	100		
		V_{CE} = 3 V, I_C = 10 μA	30	54		
	Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)	V_{CE} = 3 V, I_{C1} = I_{C2} = 1 mA	0.9	0.97		
h_{FED}	Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	V_{CE} = 3 V, I_C = 1 mA	2000	5400		
		V_{CE} = 3 V, I_C = 100 μA	1000	2800		
V_{BE}	Base-to-Emitter Voltage	V_{CE} = 3 V, I_E = 1 mA	0.600	0.715	0.800	V
		V_{CE} = 3 V, I_E = 10 mA		0.800	0.900	
$\lvert V_{BE_1} \rvert$ / $\lvert V_{BE_2} \rvert$	Input Offset Voltage	V_{CE} = 3 V, I_E = 1 mA		0.48	2.0	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	V_{CE} = 3 V, I_E = 1 mA		−1.9		mV/°C
V_{BED} (V_{9-1})	Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{CE} = 3 V, I_E = 10 mA		1.46	1.60	V
		V_{CE} = 3 V, I_E = 1 mA	1.10	1.32	1.50	
$\frac{\Delta V_{BED}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	V_{CE} = 3 V, I_E = 1 mA		4.4		mV/°C
$\frac{V_{BE_1}-V_{BE_2}}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	V_{CC} = +6 V, V_{EE} = −6 V		10		μV/°C
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA, Source resistance = 1 kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent Circuit Characteristics:					
h_{fe}	Forward Current-Transfer Ratio	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110		
h_{ie}	Short Circuit Input Resistance			3.5		kΩ
h_{oe}	Open Circuit Output Conductance			15.6		μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
	Admittance Characteristics:					
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance			0.3 + j 0.04		mmho
Y_{oe}	Output Admittance			0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance			See Curve		mmho
f_T	Gain-Bandwidth Product	V_{CE} = 3 V, I_C = 3 mA		500		MHz
C_{eb}	Emitter-to-Base Capacitance	V_{EB} = 3 V, I_E = 0		0.6		pF
C_{cb}	Collector-to-Base Capacitance	V_{CB} = 3 V, I_C = 0		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	V_{CI} = 3 V, I_C = 0		2.8		pF

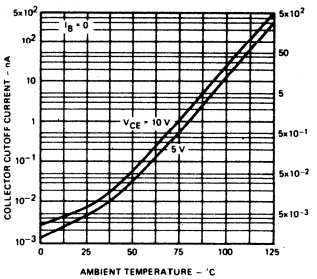
13

TYPICAL PERFORMANCE CURVES FOR μA3018/3018A

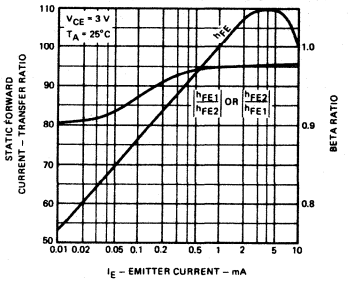
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



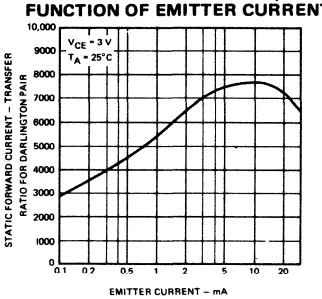
COLLECTOR-TO-EMITTER CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



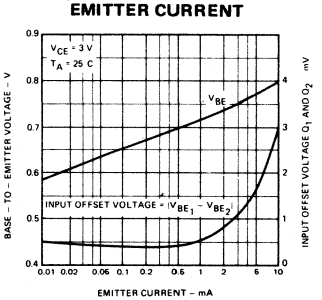
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



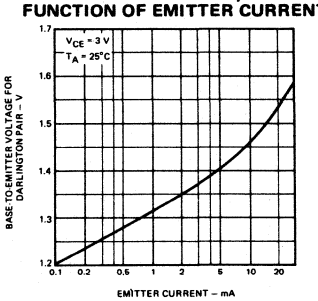
STATIC FORWARD CURRENT-TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q3, Q4 AS A FUNCTION OF EMITTER CURRENT



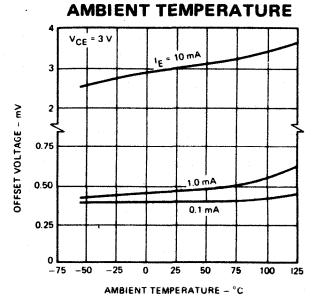
STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



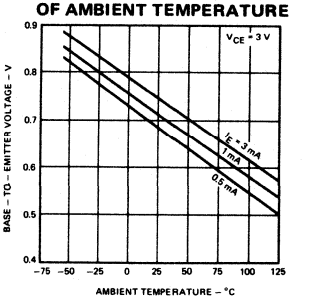
STATIC INPUT VOLTAGE FOR DARLINGTON PAIR Q3, Q4 AS A FUNCTION OF EMITTER CURRENT



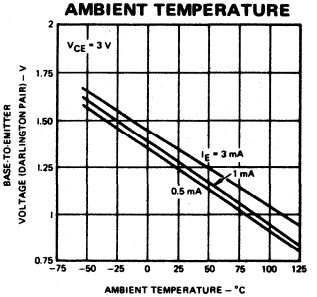
OFFSET VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE



BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE

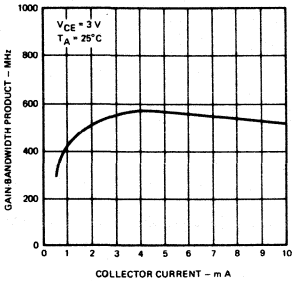


STATIC INPUT VOLTAGE FOR DARLINGTON PAIR (Q_3, Q_4) AS A FUNCTION OF AMBIENT TEMPERATURE

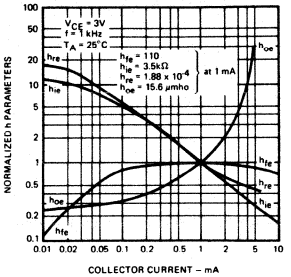


TYPICAL AC CHARACTERISTICS FOR EACH TRANSISTOR

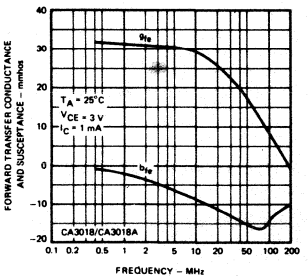
GAIN-BANDWIDTH PRODUCT (f_T) AS A FUNCTION OF COLLECTOR CURRENT



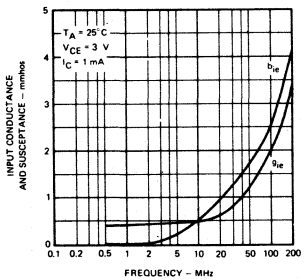
NORMALIZED h PARAMETERS AS A FUNCTION OF COLLECTOR CURRENT



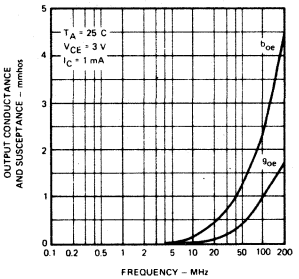
FORWARD TRANSFER ADMITTANCE (Y_{fe}) AS A FUNCTION OF FREQUENCY



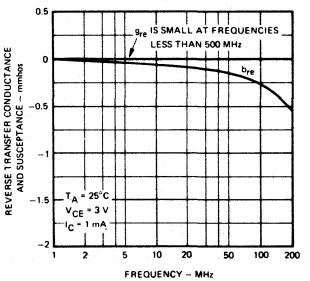
INPUT ADMITTANCE (Y_{ie}) AS A FUNCTION OF FREQUENCY



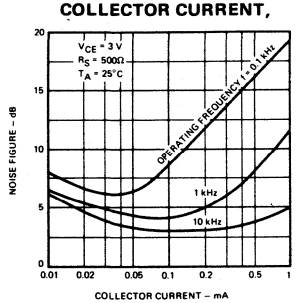
OUTPUT ADMITTANCE (Y_{oe}) AS A FUNCTION OF FREQUENCY



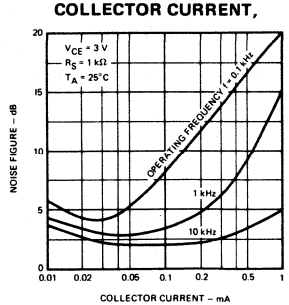
REVERSE TRANSFER ADMITTANCE (Y_{re}) AS A FUNCTION OF FREQUENCY



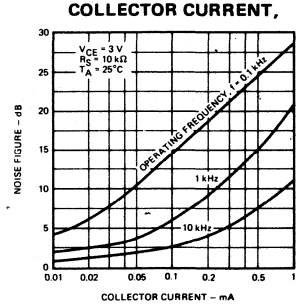
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



μA3019

- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **LOW REVERSE LEAKAGE CURRENT – 5 mA TYP.**

APPLICATIONS

- Modulator
- Mixer
- Balanced Modulator
- Analog Switch
- Diode Gate for Chopper-Modulator Applications

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	
For each Diode	20 mW
Total For Device	120 mW
Temperature Range	
Storage Temperature	−65°C to +200°C
Operating Temperature	−55°C to +125°C
Voltage Between Any Pin and Pin 7 (Note 1)	18 V

ELECTRICAL CHARACTERISTICS FOR μA3019 (For each diode, T_A = 25°C unless otherwise specified)

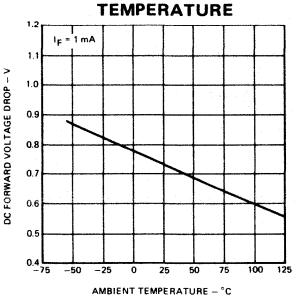
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_F	DC Forward Voltage Drop	DC Forward Current, I_F = 1 mA	–	0.73	0.78	V
BV	DC Reverse Breakdown Voltage (Any Diode)	DC Reverse Current, I_R = −10 μA	4.0	6.0	–	V
BV_S	DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	DC Reverse Current, I_R = −10 μA	25	80	–	V
I_R	DC Reverse (Leakage) Current	DC Reverse Voltage, V_R = −4 V	–	0.0055	10	μA
I_R	DC Reverse (Leakage) Current Between any Diode Unit and Substrate	DC Reverse Voltage, V_R = −4 V	–	0.010	10	μA
$\lvert V_{F_1} - V_{F_2} \rvert$	Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	DC Forward Current, I_F = 1 mA	–	1.0	5.0	mV
C_D	Single Diode Capacitance	Frequency, f = 1 MHz DC Reverse Voltage, V_R = −2 V	–	1.8	–	pF
C_{DQ-I}	Diode Quad-to-Substrate Capacitance	Frequency, f = 1 MHz DC Reverse Voltage, V_R between Pins 2,5,6, or 8 of Diode Quad and Pin 7 (Substrate) = −2 V				
		Pin 2 or 6 to Pin 7	–	4.4	–	pF
		Pin 5 or 8 to Pin 7	–	2.7	–	pF
V_S	Series Gate Switching Pedestal Voltage	See Figure 1	–	10	–	mV

NOTE

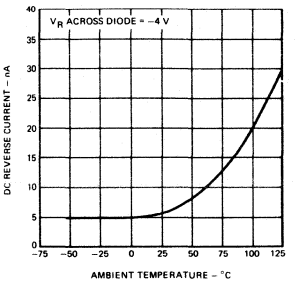
1. Substrate (Pin 7) must be connected to the most negative potential.

TYPICAL PERFORMANCE CURVES FOR μA3019

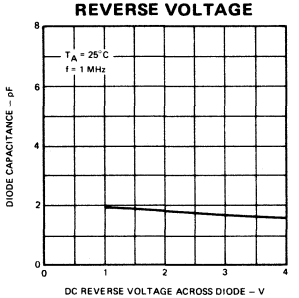
DC FORWARD VOLTAGE DROP (ANY DIODE) AS A FUNCTION OF TEMPERATURE



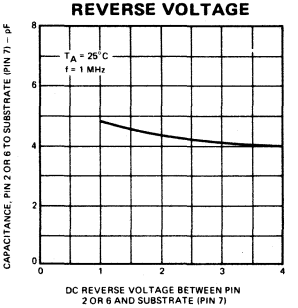
REVERSE (LEAKAGE) CURRENT (ANY DIODE) AS A FUNCTION OF TEMPERATURE



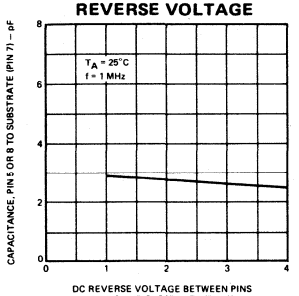
DIODE CAPACITANCE (ANY DIODE) AS A FUNCTION OF REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



SERIES GATE SWITCHING TEST SETUP

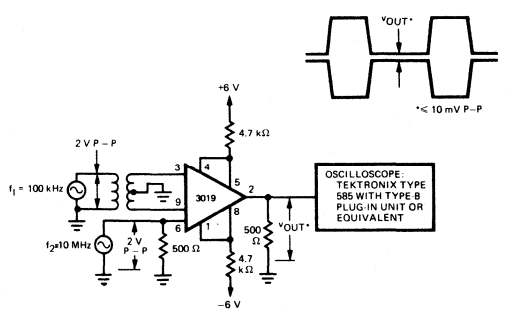


Fig. 1

13

μA3026/3054

- **LOW INPUT OFFSET VOLTAGE – ±5 mV**
- **WIDEBAND OPERATION**
- **INDEPENDENTLY ACCESSIBLE INPUTS AND OUTPUTS**
- **TWO MATCHED DIFFERENTIAL AMPLIFIERS**

APPLICATIONS

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations – RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

	μA3054	μA3026
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	600 mW	750 mW
Temperature Range		
Operating Temperature	−55°C to +125°C	0°C to +85°C
Storage Temperature	−65°C to +200°C	−25°C to +85°C
The following ratings apply for each transistor in the device		
Collector-to-Emitter Voltage, V_{CEO}		15 V
Collector-to-Base Voltage, V_{CBO}		20 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)		20 V
Emitter-to-Base Voltage, V_{EBO}		5 V
Collector Current, I_C		50 mA

ELECTRICAL CHARACTERISTICS FOR μA3026/3054 (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	For Each Differential Amplifier					
V_{IO}	Input Offset Voltage		–	0.45	5	mV
I_{IO}	Input Offset Current	V_{CB} = 3 V	–	0.3	2	μA
I_I	Input Bias Current		–	10	24	μA
$I_{C(Q_1)}$ or $I_{C(Q_5)}$ / $I_{C(Q_2)}$ or $I_{C(Q_6)}$	Quiescent Operating Current Ratio	$I_{E(Q_3)} = I_{E(Q_4)}$ = 2 mA	–	0.98 to 1.02	–	–
$\frac{\Delta\lvert V_{IO}\rvert}{\Delta T}$	Temperature Coefficient Magnitude of Input-Offset Voltage		–	1.1	–	μV/°C
	For Each Transistor					
V_{BE}	DC Forward Base-to-Emitter Voltage	V_{CB} = 3 V, I_C = 50 μA	–	0.630	0.700	V
		1 mA	–	0.715	0.800	
		3 mA	–	0.750	0.850	
		10 mA	–	0.800	0.900	
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient of Base-to-Emitter Voltage	V_{CB} = 3 V, I_C = 1 mA	–	−1.9	–	mV/°C
I_{CBO}	Collector-Cutoff Current	V_{CB} = 10 V, I_E = 0	–	0.002	100	nA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	15	24	–	V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	20	60	–	V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	I_C = 10 μA, I_{CI} = 0	20	60	–	V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5	7	–	V

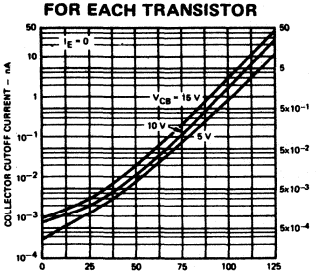
NOTES
1. For $T_A > 55°C$; 3026 derates at 5 mW/°C and 3054 at 6.67 mW/°C
2. The collector of each transistor of the 3026 and 3054 is isolated from the substrate by an integral diode. Substrate must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS FOR μA3026/3054 (T_A = 25°C unless otherwise specified) (Cont'd)

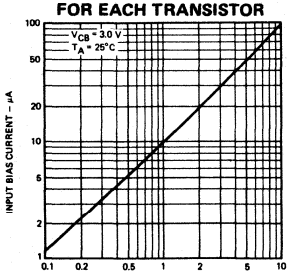
SYMBOL	PARAMETER (See Test Circuits)	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common-Mode Rejection Ratio for Each Amplifier	V_{CC} = 12 V	–	100	–	dB
AGC	AGC Range, One Stage	V_{EE} = −6 V	–	75	–	dB
A_V	Voltage Gain, Single Stage Double-Ended Output	V_X = −3.3 V	–	32	–	dB
AGC	AGC Range, Two Stage	f = 1 kHz	–	105	–	dB
A_V	Voltage Gain, Two Stage Double-Ended Output		–	60	–	dB
	Low-Frequency, Small-Signal Equivalent-Circuit Characteristics (for Single Transistor):					
h_{fe}	Forward Current-Transfer Ratio		–	110	–	–
h_{ie}	Short Circuit Input Resistance	f = 1 kHz, V_{CE} = 3 V,	–	3.5	–	kΩ
h_{oe}	Open Circuit Output Conductance	I_C = 1 mA	–	15.6	–	μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio		–	1.8×10^{-4}	–	–
NF	1 Noise Figure (for Single Transistor)	f = 1 kHz, V_{CE} = 3 V	–	3.25	–	dB
f_T	Gain-Bandwidth Product (for Single Transistor)	V_{CE} = 3 V, I_C = 3 mA	–	550	–	MHz
	Admittance Characteristics; Differential Circuit Configuration (for Each Amplifier):					
y_{21}	Forward Transfer Admittance	V_{CB} = 3 V	–	−20+j 0	–	mmho
y_{11}	Input Admittance	Each Collector	–	0.22+j 0.1	–	mmho
y_{22}	Output Admittance	$I_C \approx$ 1.25 mA	–	0.01+j 0	–	mmho
y_{12}	Reverse Transfer Admittance	f = 1 MHz	–	−0.003+j 0	–	mmho
	Admittance Characteristics; Cascode Circuit Configuration (for Each Amplifier):					
y_{21}	Forward Transfer Admittance	V_{CB} = 3 V	–	68-j 0	–	mmho
y_{11}	Input Admittance	Total Stage	–	0.55+j 0	–	mmho
y_{22}	Output Admittance	$I_C \approx$ 2.5 mA	–	0+j 0.02	–	mmho
y_{12}	Reverse Transfer Admittance	f = 1 MHz	–	0.004-j 0.005	–	μmho
NF	Noise Figure	f = 100 MHz	–	8	–	dB

TYPICAL PERFORMANCE CURVES FOR μA3026/3054

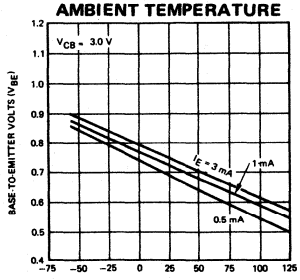
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



INPUT BIAS CURRENT CHARACTERISTIC AS A FUNCTION OF COLLECTOR CURRENT FOR EACH TRANSISTOR



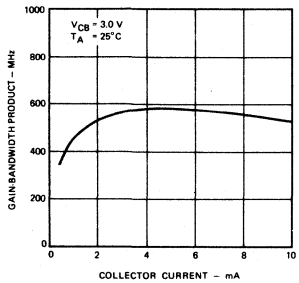
BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE



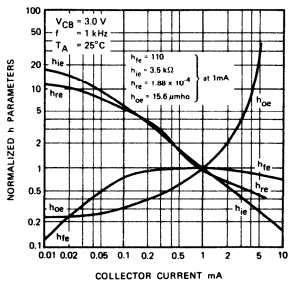
13

TYPICAL AC CHARACTERISTICS FOR EACH TRANSISTOR FOR μA3026/3054

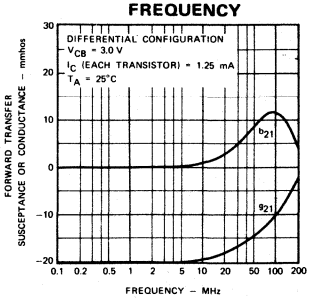
GAIN BANDWIDTH PRODUCT (f_T) AS A FUNCTION OF COLLECTOR CURRENT



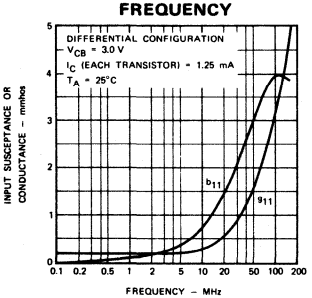
NORMALIZED h PARAMETER AS A FUNCTION OF COLLECTOR CURRENT FOR EACH TRANSISTOR



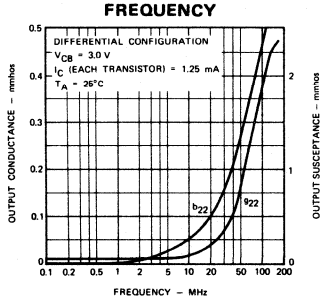
FORWARD TRANSFER ADMITTANCE (Y_{21}) AS A FUNCTION OF FREQUENCY



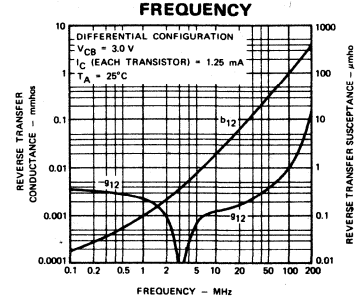
INPUT ADMITTANCE (Y_{11}) AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) AS A FUNCTION OF FREQUENCY

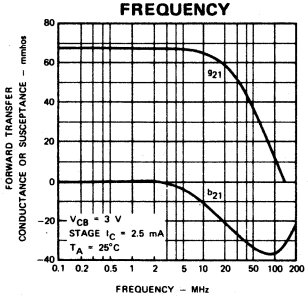


REVERSE TRANSFER ADMITTANCE (Y_{12}) AS A FUNCTION OF FREQUENCY

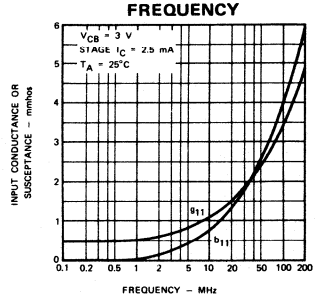


TYPICAL AC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER FOR μA3026/3054

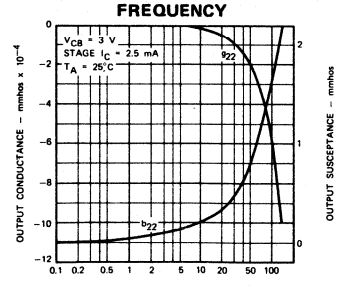
FORWARD TRANSFER ADMITTANCE (Y_{21}) AS A FUNCTION OF FREQUENCY



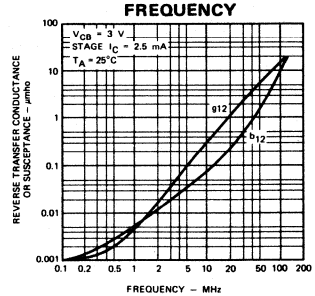
INPUT ADMITTANCE (Y_{11}) AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) AS A FUNCTION OF FREQUENCY

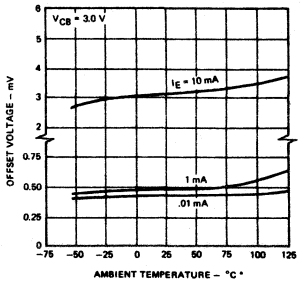


REVERSE TRANSFER ADMITTANCE (Y_{12}) AS A FUNCTION OF FREQUENCY

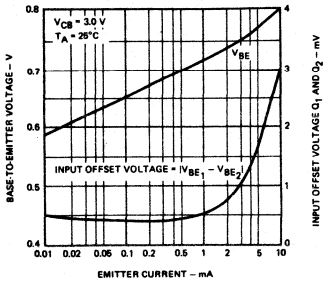


TYPICAL PERFORMANCE CURVES FOR μA3026/3054 (Cont'd)

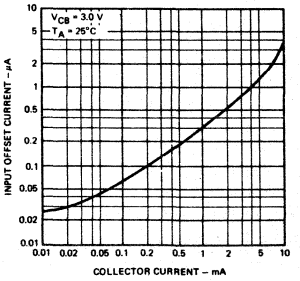
OFFSET VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE FOR DIFFERENTIAL PAIRS



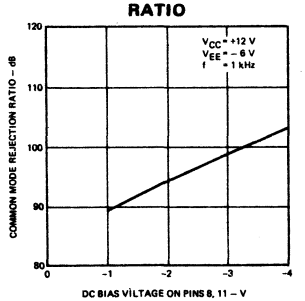
STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS AS A FUNCTION OF EMITTER CURRENT



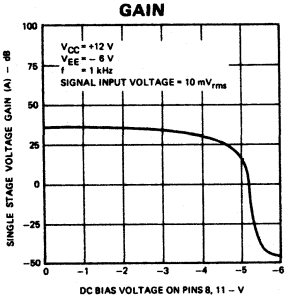
INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS AS A FUNCTION OF COLLECTOR CURRENT



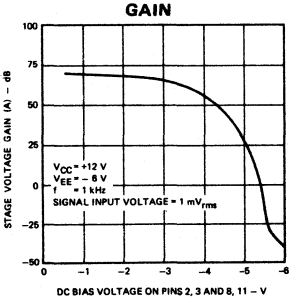
COMMON MODE REJECTION RATIO

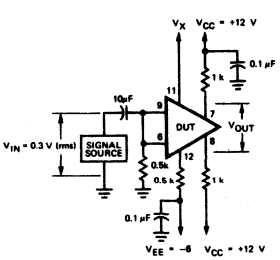


SINGLE STAGE VOLTAGE GAIN

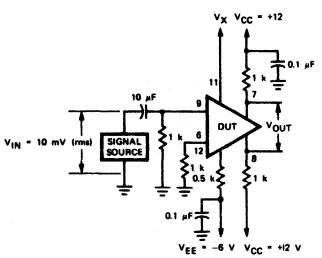


TWO-STAGE VOLTAGE GAIN

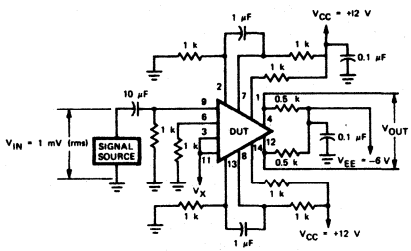




Test setup



Test setup



Test setup

Pin numbers are shown for 3054 (DIP) only.

μA3036

- **MATCHED TRANSISTOR PERFORMANCE**
- **LOW NOISE PERFORMANCE**
- **200 MHz GAIN BANDWIDTH PRODUCT**

APPLICATIONS

- Stereo Phonograph Preamplifiers
- Low level Stereo and Single Channel Amplifier Stages
- Low noise, Emitter-follower Differential Amplifiers
- Operational Amplifier Drivers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

Power Dissipation	
Any One Transistor	300 mW
Total For Array	300 mW
Temperature Range	
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +200°C
The following ratings apply for each transistor in the array	
Collector-to-Emitter Voltage, V_{CEO}	15 V
Collector-to-Base Voltage, V_{CBO}	30 V
Emitter-to-Base Voltage, V_{EBO}	5 V
Collector Current, I_C	50 mA

ELECTRICAL CHARACTERISTICS FOR μA3036 (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	For Each Transistor (Q_1, Q_2, Q_3, Q_4)					
I_{CBO}	Collector Cutoff Current	V_{CB} = 5 V, I_E = 0	–	–	0.5	μA
I_{CEO}	Collector Cutoff Current	V_{CE} = 15 V, I_B = 0	–	–	5.0	μA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	15	20	–	V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	30	44	–	V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5.0	6.0	–	V
	For Either Input Transistor (Q_1 or Q_3)					
h_{FE}	Static Forward Current-Transfer Ratio	I_{C1} or I_{C3} = 1 mA	30	82	–	–
	For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)					
$V_{(BR)EBO(D)}$	Emitter-to-Base Breakdown Voltage	I_{E2} or I_{E4} = 10 μA	10	12.6	–	V
$h_{FE(D)}$	Static Forward Current-Transfer Ratio	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	1000	4540	–	–
	For Each Input Transistor (Q_1 or Q_3)					
h_{fe}	Short Circuit Forward Current-Transfer Ratio		–	82	–	–
h_{ie}	Short Circuit Input Resistance	f = 1 kHz	–	2.6	–	kΩ
h_{oe}	Open Circuit Output Conductance	I_{C1} or I_{C3} = 1 mA	–	7.0	–	μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio		–	9.8×10^{-5}	–	–
	For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)					
$h_{fe(D)}$	Short Circuit Forward Current-Transfer Ratio	f = 1 kHz	–	1300	–	–
$h_{ie(D)}$	Short Circuit Input Resistance	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	–	82	–	kΩ
$h_{oe(D)}$	Open Circuit Output Conductance		–	108	–	μmho
$h_{re(D)}$	Open Circuit Reverse Voltage-Transfer Ratio		–	2.7×10^{-3}	–	–
E_N	Noise Voltage	f = 100 Hz	–	0.2	3.0	$\frac{\mu V\ (rms)}{\sqrt{f(Hz)}}$
		f = 1 kHz	–	0.05	0.3	
		f = 10 kHz	–	0.012	0.1	
	For Either Input Transistor (Q_1 or Q_3)					
Y_{fe}	Forward Transfer Admittance	f = 50 MHz, I_{C1} or I_{C3} = 2 mA	–	0.68 + j 7.9	–	mmho
Y_{ie}	Input Admittance (Output Short Circuited)		–	4.4 + j 5.95	–	mmho
Y_{oe}	Output Admittance (Input Short Circuited)		–	1.94 + j 2.64	–	mmho
Y_{re}	Reverse Transfer Admittance (Input Short-Circuited)		–	Negligible	–	mmho
	For Either Darlington Pair (Q_1, Q_2, or Q_3, Q_4)					
$Y_{ie(D)}$	Input Admittance (Output Short Circuited)	f = 50 MHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 2 mA	–	1.71 + j 2.8	–	mmho
$Y_{oe(D)}$	Output Admittance (Input Short Circuited)		–	3.96 + j 2.6	–	mmho
$f_{T(D)}$	Gain-Bandwidth Product		150	200	–	MHz

μA3039

- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **REVERSE RECOVERY TIME – 1 ns TYP.**
- **LOW DIODE CAPACITANCE – 0.65 pF @ V_R = –2 V**

APPLICATIONS
- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (See note)	
Any One Diode Unit	100 mW
Total for Device	600 mW
Temperature Range	
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +200°C
Voltages and Currents	
Peak Inverse Voltage, PIV for: D_1 - D_5	5 V
D_6	0.5 V
Peak Diode-to-Substrate Voltage, V_{DI} for D_1 - D_5 (term. 1,4,5,8 or 12 to term. 10)	+20,–1 V
DC Forward Current, I_F	25 mA
Peak Recurrent Forward Current, I_f	100 mA
Peak Forward Surge Current, I_f (surge)	100 mA

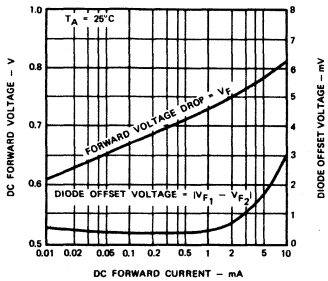
ELECTRICAL CHARACTERISTICS FOR μA3039 (For each diode unit, T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_F	DC Forward Voltage Drop	I_F = 50 μA	–	0.65	0.69	V
		1 mA	–	0.73	0.78	V
		3 mA	–	0.76	0.80	V
		10 mA	–	0.81	0.90	V
BV	DC Reverse Breakdown Voltage	I_R = –10 μA	5.0	7.0	–	V
BV_S	DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	I_R = –10 μA	20	–	–	V
I_R	DC Reverse (Leakage) Current	V_R = –4 V	–	0.016	100	nA
I_R	DC Reverse (Leakage) Current Between any Diode Unit and Substrate	V_R = –10 V	–	0.022	100	nA
$\lvert V_{F_1} - V_{F_2} \rvert$	Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	I_F = 1 mA	–	0.5	5.0	mV
$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	1.0	–	μV/°C
$\frac{\Delta V_F}{\Delta T}$	Temperature Coefficient of Forward Drop	I_F = 1 mA	–	–1.9	–	mV/°C
V_F	DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	I_F = 1 mA	–	0.65	–	V
t_{rr}	Reverse Recovery Time	I_F = 10 mA, I_R = 10 mA	–	1.0	–	ns
R_D	Diode Resistance	f = 1 kHz, I_F = 1 mA	25	30	45	Ω
C_D	Diode Capacitance	V_R = –2 V, I_F = 0	–	0.65	–	pF
C_{DI}	Diode-to-Substrate Capacitance	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF

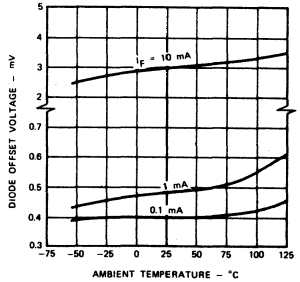
NOTE: Derate at 5.7 mW/°C for T_A > 55°C.

TYPICAL PERFORMANCE CURVES FOR μA3039

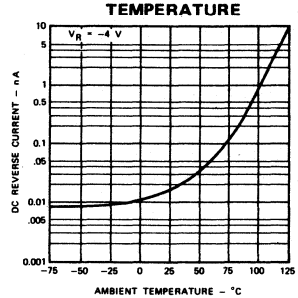
DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE AS A FUNCTION OF DC FORWARD CURRENT



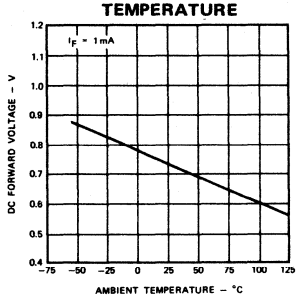
DIODE OFFSET VOLTAGE (ANY DIODE) AS A FUNCTION OF TEMPERATURE



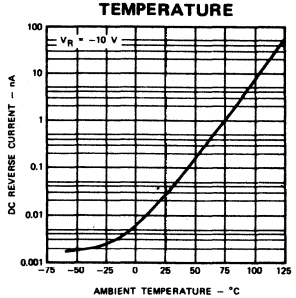
DC REVERSE (LEAKAGE) CURRENT (DIODES 1, 2, 3, 4, 5) AS A FUNCTION OF TEMPERATURE



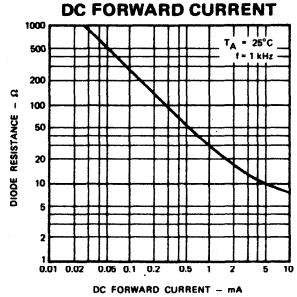
DC FORWARD VOLTAGE DROP (ANY DIODE) AS A FUNCTION OF TEMPERATURE



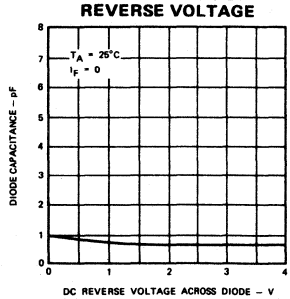
DC REVERSE (LEAKAGE) CURRENT BETWEEN DIODES (1, 2, 3, 4, 5) AND SUBSTRATE AS A FUNCTION OF TEMPERATURE



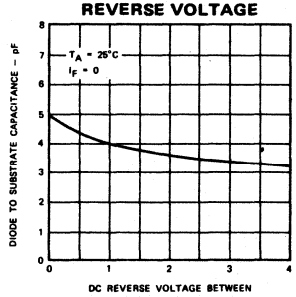
DIODE RESISTANCE (ANY DIODE) AS A FUNCTION OF DC FORWARD CURRENT



DIODE CAPACITANCE (DIODES 1, 2, 3, 4, 5) AS A FUNCTION OF REVERSE VOLTAGE



DIODE-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



μA3045/3046/3086

- **LOW INPUT OFFSET VOLTAGE**
- **WIDEBAND OPERATION**
- **LOW NOISE**

APPLICATIONS

- General Use in all Types of Signal Processing Systems Operating Anywhere in the Frequency Range From DC to VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)		μA3045	μA3046/3086	
Power Dissipation (Note 1)	**Each Transistor**	**Total Package**	**Each Transistor**	**Total Package**
At T_A = 25°C	300 mW	750 mW	300 mW	750 mW
At T_A = 25°C to 55°C			300 mW	750 mW
At T_A = 25°C to 75°C	300 mW	750 mW		
Voltages and Currents				
Collector-to-Emitter Voltage, V_{CEO}	15 V	–	15 V	–
Collector-to-Base Voltage, V_{CBO}	20 V	–	20 V	–
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V	–	20 V	–
Emitter-to-Base Voltage, V_{EBO}	5 V	–	5 V	–
Collector Current, I_C	50 mA	–	50 mA	–
Temperature Range				
Operating Temperature	−55°C to +125°C		(3046) 0°C to +85°C (3086) −40°C to +85°C	
Storage Temperature	−65°C to +200°C		−55°C to +125°C	

13

ELECTRICAL CHARACTERISTICS FOR μA3045/3046 (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	20	60		V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	15	24		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	I_C = 10 μA, I_C = 0	20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5.0	7.0		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 10 V, I_E = 0		0.002	40	nA
I_{CEO}	Collector Cutoff Current	V_{CE} = 10 V, I_B = 0		See Curve	0.5	μA
h_{FE}	Static Forward Current-Transfer Ratio (Static Beta)	V_{CE} = 3 V, I_C = 10 mA	40	100		
		V_{CE} = 3 V, I_C = 1 mA		100		
		V_{CE} = 3 V, I_C = 10 μA		54		
	Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO1} - I_{IO2} \rvert$	V_{CE} = 3 V, I_C = 1 mA		0.3	2.0	μA
V_{BE}	Base-to-Emitter Voltage	V_{CE} = 3 V, I_E = 1 mA		0.715		V
		V_{CE} = 3 V, I_E = 10 mA		0.800		
	Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE} = 3 V, I_C = 1 mA		0.45	5.0	mV
	Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$	V_{CE} = 3 V, I_C = 1 mA		0.45	5.0	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient of Base-to-Emitter Voltage	V_{CE} = 3 V, I_C = 1 mA		−1.9		mV/°C
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	I_B = 1 mA, I_C = 10 mA		0.23		V
$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	V_{CE} = 3 V, I_C = 1 mA		1.1		μV/°C
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent-Circuit Characteristics:					
h_{fe}	Forward Current-Transfer Ratio	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110		
h_{ie}	Short-Circuit Input Resistance			3.5		kΩ
h_{oe}	Open-Circuit Output Conductance			15.6		μmbo
h_{re}	Open-Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
	Admittance Characteristics:					
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31-j 1.5		
Y_{ie}	Input Admittance			0.3+j0.04		
Y_{oe}	Output Admittance			0.001+j0.03		
Y_{re}	Reverse Transfer Admittance			See Curve		
f_T	Gain-Bandwidth Product	V_{CE} = 3 V, I_C = 3 mA	300	550		MHz
C_{EB}	Emitter-to-Base Capacitance	V_{EB} = 3 V, I_E = 0		0.6		pF
C_{CB}	Collector-to-Base Capacitance	V_{CB} = 3 V, I_C = 0		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	V_{CS} = 3 V, I_C = 0		2.8		pF

NOTES:
1. μA3046 and μA3086 derate at 6.67 mW/°C for $T_A > 55°C$, μA3045 at 8 mW/°C for $T_A > 75°C$.
2. Substrate (Pin 13) must be connected to the most negative voltage to maintain normal operation.

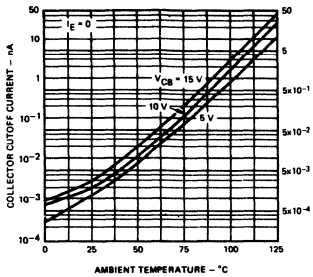
ELECTRICAL CHARACTERISTICS FOR μA3086 (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	20	60		V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	15	24		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	I_C = 10 μA, I_C = 0	20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5.0	7.0		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 10 V, I_E = 0		0.002	100	nA
I_{CEO}	Collector Cutoff Current	V_{CE} = 10 V, I_B = 0		See Curve	5.0	μA
h_{FE}	Static Forward Current-Transfer Ratio (Static Beta)	V_{CE} = 3 V, I_C = 10 mA I_C = 1 mA I_C = 10 μA	40	100 100 54		
	Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO1} - I_{IO2} \rvert$	V_{CE} = 3 V, I_C = 1 mA				μA
V_{BE}	Base-to-Emitter Voltage	V_{CE} = 3 V, I_E = 1 mA I_E = 10 mA		0.715 0.800		V
	Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE} = 3 V, I_C = 1 mA				mV
	Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$	V_{CE} = 3 V, I_C = 1 mA				mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient of Base-to-Emitter Voltage	V_{CE} = 3 V, I_C = 1 mA		−1.9		mV/°C
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	I_B = 1 mA, I_C = 10 mA		0.23		V
$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	V_{CE} = 3 V, I_C = 1 mA				μV/°C
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA R_S = 1 kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent-Circuit Characteristics:					
h_{fe}	Forward Current-Transfer Ratio	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110		
h_{ie}	Short-Circuit Input Resistance			3.5		kΩ
h_{oe}	Open-Circuit Output Conductance			15.6		μmbo
h_{re}	Open-Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
	Admittance Characteristics:					
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31-j 1.5		
Y_{ie}	Input Admittance			0.3+j0.04		
Y_{oe}	Output Admittance			0.001+j0.03		
Y_{re}	Reverse Transfer Admittance			See Curve		
f_T	Gain-Bandwidth Product	V_{CE} = 3 V, I_C = 3 mA	300	550		MHz
C_{EB}	Emitter-to-Base Capacitance	V_{EB} = 3 V, I_E = 0		0.6		pF
C_{CB}	Collector-to-Base Capacitance	V_{CB} = 3 V, I_C = 0		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	V_{CS} = 3 V, I_C = 0		2.8		pF

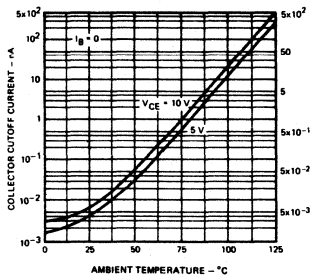
13

TYPICAL PERFORMANCE CURVES FOR μA3045/3046/3086

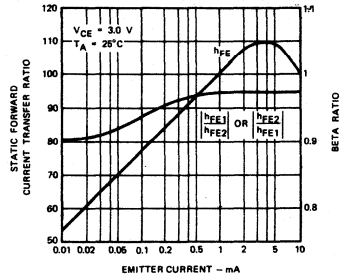
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



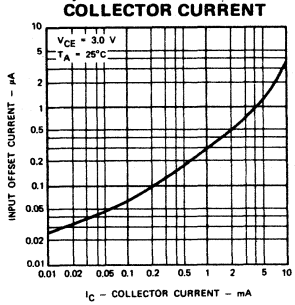
COLLECTOR-TO-EMITTER CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



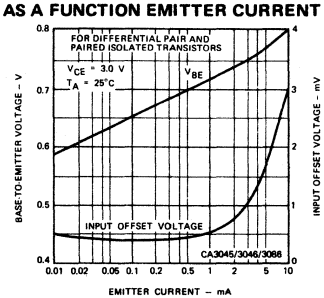
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



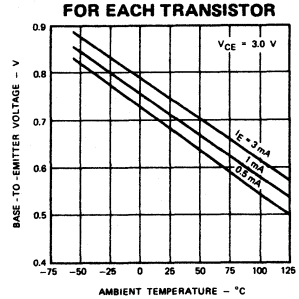
INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q1, Q2 AS A FUNCTION OF COLLECTOR CURRENT



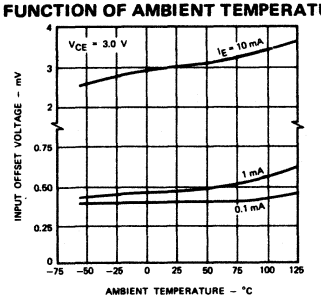
STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE AS A FUNCTION EMITTER CURRENT



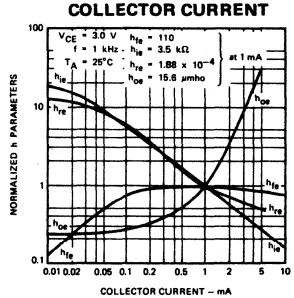
BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



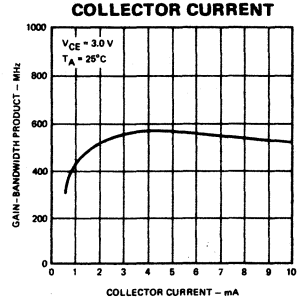
INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS AS A FUNCTION OF AMBIENT TEMPERATURE



NORMALIZED h PARAMETERS AS A FUNCTION OF COLLECTOR CURRENT

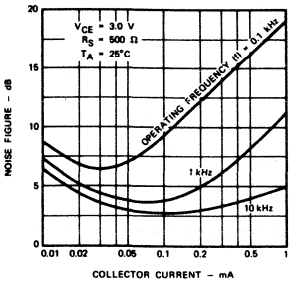


GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF COLLECTOR CURRENT

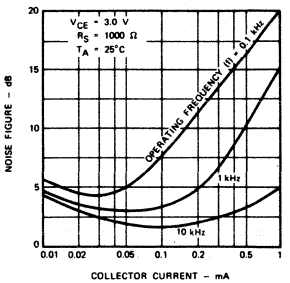


TYPICAL PERFORMANCE CURVES FOR μA3045/3046/3086 (Cont'd)

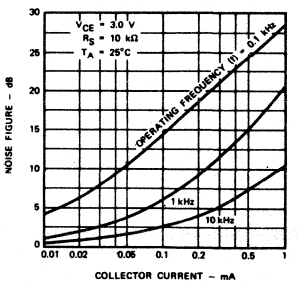
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



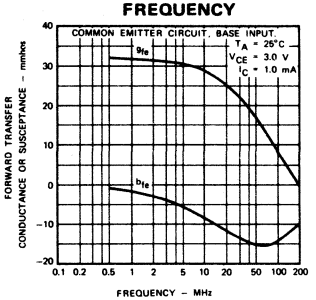
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



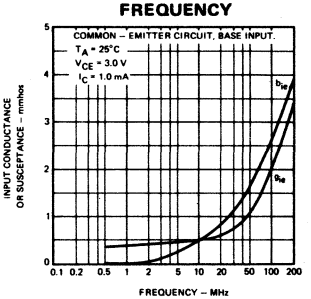
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



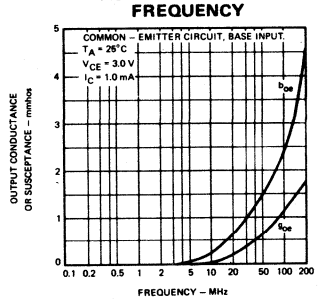
FORWARD TRANSFER ADMITTANCE AS A FUNCTION OF FREQUENCY



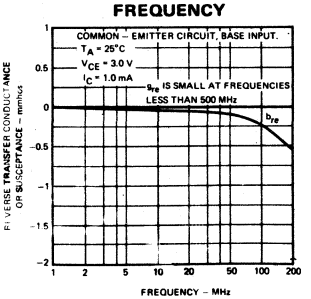
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



REVERSE TRANSFER ADMITTANCE AS A FUNCTION OF FREQUENCY



13

F4016/34016
QUAD BILATERAL SWITCHES

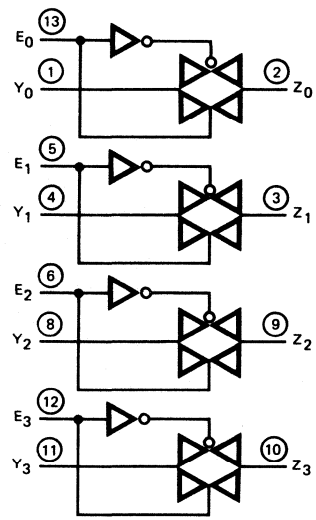
DESCRIPTION – The F4016 has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch and establishes a high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

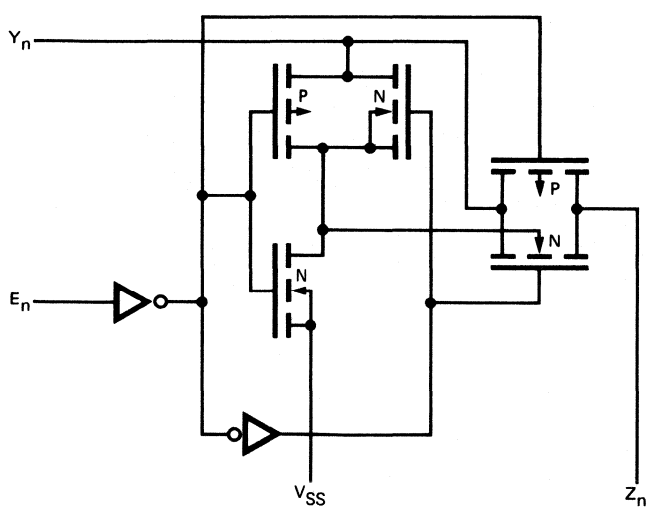
E_0 - E_3	Enable Inputs
Y_0 - Y_3	Input/Output Terminals
Z_0 - Z_3	Input/Output Terminals

LOGIC SYMBOL

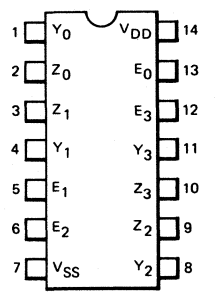


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A F4016)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

CMOS • F4016/34016

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS	
R_{ON}	ON Resistance	XC						610 660 840			370 400 520	Ω	MIN 25°C MAX	$V_{is} = V_{DD}$	R_L = 10 kΩ $E_n = V_{DD}$
								610 660 840			370 400 520	Ω	MIN 25°C MAX	$V_{is} = V_{SS}$ +0.25 V	
					1900 2000 2380							Ω	MIN 25°C MAX	V_{is} = 2.5 V	
								1750 1800 2360				Ω	MIN 25°C MAX	V_{is} = 5.6 V	
											775 800 1020	Ω	MIN 25°C MAX	V_{IN} = 9.3 V	
		XM						600 660 960			360 400 600	Ω	MIN 25°C MAX	$V_{is} = V_{DD}$	R_L = 10 kΩ $E_n = V_{DD}$
								600 660 960			360 400 600	Ω	MIN 25°C MAX	$V_{is} = V_{SS}$ +0.25 V	
					1870 2000 2600							Ω	MIN 25°C MAX	V_{is} = 2.5 V	
								1700 1800 2000				Ω	MIN 25°C MAX	V_{is} = 5.6 V	
											750 800 1200	Ω	MIN 25°C MAX	V_{is} = 9.3 V	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Switches						15			10		Ω	25°C	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{DD}$ R_L = 10 kΩ	
I_Z	OFF State Leakage Current, Any Y to Z							125			200	nA	25°C	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{SS}$	
I_{DD}	Quiescent Power Supply Current	XC			0.25 7			0.5 8		0.1 1.6		μA	MIN, 25°C MAX	All inputs common and at V_{DD} or V_{SS}	
		XM			0.25 25			0.5 30		0.1 6		μA	MIN, 25°C MAX		

Notes on following page.

13

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		4 3			1.5 1.5			1 1		ns ns	R_L = 10 kΩ, E_n = V_{DD} C_L = 15 pF Input Transition Times ≤ 20 ns V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		26 26			14 14			10 10		ns ns	E_n = V_{DD} (square wave) R_L = 10 kΩ, C_L = 15 pF Input Transition Times ≤ 20 ns V_{is} = V_{DD}
t_{PLZ} t_{PHZ}	Output Disable Time		160 160			170 170			182 182		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8			3 4			2 2.5		ns ns	R_L = 10 kΩ, E_n = V_{DD} C_L = 50 pF Input Transition Times ≤ 20 ns V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32			16 16			13 13		ns ns	R_L = 10 kΩ, C_L = 50 pF Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{is} = V_{DD}
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns ns	
	Distortion, Sine Wave Response		0.31			0.31			0.31		%	R_L = 10 kΩ, C_L = 15 pF Input Frequency = 1 kHz E_n = V_{DD} V_{is} = V_{DD}/2 (sine wave)
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ, E_A = V_{DD}, E_B = V_{SS} V_{is} = V_{DD}/2 sine wave at − 50 dB, 20 Log_{10} [V_{os} (B)/V_{is} (A)] = −50 dB
	Crosstalk, Enable Input to Output					50					mV	$R_{L(OUT)}$ = 10 kΩ, $R_{L(IN)}$ = 1 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ E_n = V_{SS}, V_{is} = V_{DD}/2 sine wave 20 Log_{10} (V_{os}/V_{is}) = −50 dB
	ON State Frequency Response					90					MHz	R_L = 1 kΩ, V_{is} = V_{DD}/2 sine wave E_n = V_{DD}, 20 Log_{10} (V_{os}/V_{is}) = −3 dB
f_{MAX}	Enable Input Frequency (Note 4)					10					MHz	R_L = 1 kΩ, C_L = 15 pF Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{is} = V_{DD}

NOTES:
1. Additional DC Characteristics for the Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
3. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.

F4051/34051

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The F4051 is an 8-Channel Analog Multiplexer/Demultiplexer with three Address Inputs (A_0-A_2), an active LOW Enable Input ($\overline{E}$), eight Independent Inputs/Outputs (Y_0-Y_7) and a Common Input/Output (Z).

The F4051 contains eight bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0-Y_7) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the eight switches is selected (low impedance, ON state) by the three Address Inputs (A_0-A_2). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0-A_2, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0-Y_7, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

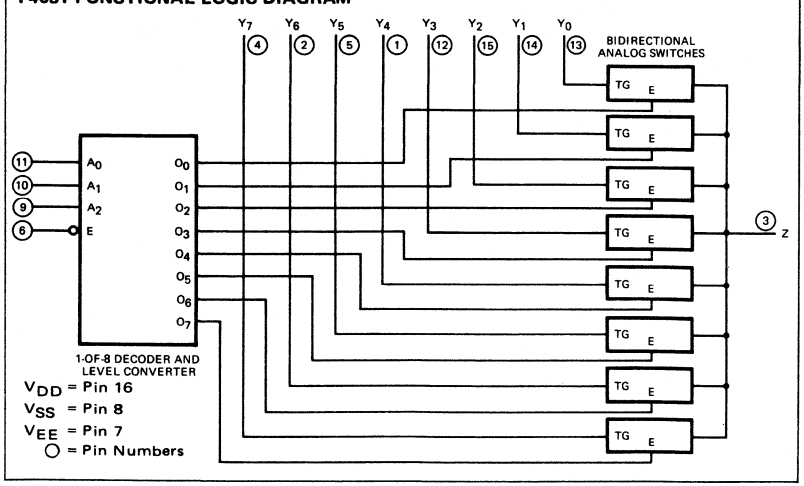
Y_0-Y_7	Independent Inputs/Outputs
A_0-A_2	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Common Input/Output

TRUTH TABLE

INPUTS				CHANNELS							
$\overline{E}$	A_2	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z	Y_4–Z	Y_5–Z	Y_6–Z	Y_7–Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

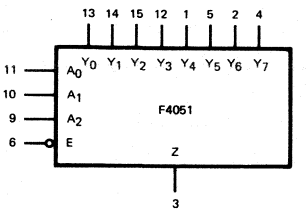
L = LOW Level
H = HIGH Level
X = Don't Care

F4051 FUNCTIONAL LOGIC DIAGRAM



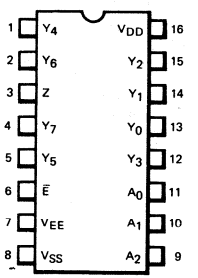
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

13

CMOS • F4051/34051

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95			55			35		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				95			55			35		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				1600			110			55		Ω	MIN	
				1000			125			60			25°C	Note 3
				850			200			95			MAX	
		XM		90			50			30		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				90			50			30		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				1750			100			50		Ω	MIN	
				1000			125			60			25°C	Note 3
				700			220			100			MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels						10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\bar{E} = V_{DD}$, $V_{SS} = V_{DD}/2$, $V_{is} = V_{DD}$ or V_{EE}
		XM						80						
	Any Channel OFF	XC						100						$\bar{E} = V_{SS} = V_{DD}/2$, $V_{is} = V_{DD}$ or V_{EE}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40		8		μA	MIN,25°C	$V_{SS} = V_{EE}$, All inputs common and at V_{DD} or V_{EE}
					700			1400		280			MAX	
		XM			2			4		0.8		μA	MIN,25°C	
					70			140		28			MAX	

Notes on following page.

CMOS • F4051/34051

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 4)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		20 8			7 4			4 3		ns ns	C_L = 15 pF, $\overline{E}$ = V_{SS} = V_{EE}, A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		160 200			90 120			75 90		ns ns	
t_{PZL} t_{PZH}	Output Enable Time		180 200			90 100			70 80		ns ns	C_L = 15 pF, $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1000 1000			900 900			860 850		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		25 10			10 6			6 4		ns ns	C_L = 50 pF $\overline{E}$ = V_{SS} = V_{EE},
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		170 210			95 125			80 95		ns ns	A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PZL} t_{PZH}	Output Enable Time		185 205			95 105			75 85		ns ns	C_L = 50 pF, $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1250 1240			1130 1120			1080 1070		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	C_L = 15 pF R_L = 10 kΩ, V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ, $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) at −40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = −40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (sine wave) 20 Log_{10} (V_{os}/V_{is}) = −40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) V_{SS} = $V_{DD}/2$ 20 Log_{10}(V_{os}/V_{is}) = −3 dB

NOTES:
1. Additional DC Characteristics for the Address and Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or $V_{DD/2}$.
3. V_{is} = 8.6 V for V_{DD} = 15 V.
   V_{is} = 5.1 V for V_{DD} = 10 V
   V_{is} = 1.9 V for V_{DD} = 5 V
4. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
5. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
6. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns, R_L = 10 kΩ.

13

F4052/34052

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The F4052 is a Dual 4-Channel Analog Multiplexer/Demultiplexer with common channel select logic. Each Multiplexer/Demultiplexer has four Independent Inputs/Outputs (Y_0–Y_3) and a Common Input/Output (Z). The common channel select logic includes two Address Inputs (A_0, A_1) and an active LOW Enable Input ($\overline{E}$).

Both multiplexer/demultiplexers contain four bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0–Y_3) and the other side connected to a Common Input/Output (Z). With the Enable Input LOW, one of the four switches is selected (low impedance, ON state) by the two Address Inputs. With the Enable Input HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0, A_1, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0–Y_3, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **DIGITAL OR ANALOG MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

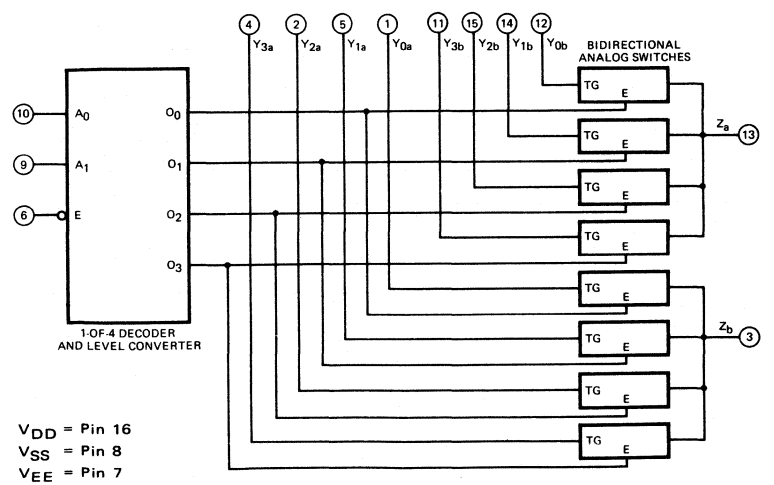
Y_{0a}–Y_{3a}	Independent Inputs/Outputs
Y_{0b}–Y_{3b}	Independent Inputs/Outputs
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a, Z_b	Common Input/Output

TRUTH TABLE

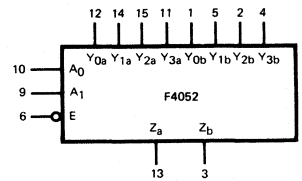
INPUTS			CHANNELS			
$\overline{E}$	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

L = LOW Level, H = HIGH Level, X = Don't care.

F4052 FUNCTIONAL LOGIC DIAGRAM

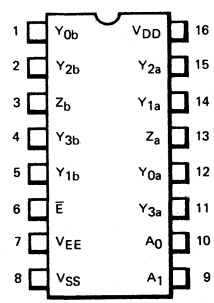


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

CMOS • F4052/34052

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95			55			35		Ω	MIN 25°C MAX	$V_{is} = V_{DD}$ Note 2
				100			65			40				
				125			100			65				
				95			55			35		Ω	MIN 25°C MAX	$V_{is} = V_{EE}$ Note 2
				100			65			40				
				125			100			65				
				1600			110			55		Ω	MIN 25°C MAX	Note 3
				1000			125			60				
				850			200			95				
		XM		90			50			30		Ω	MIN 25°C MAX	$V_{is} = V_{DD}$ Note 2
				100			65			40				
				150			110			70				
				90			50			30		Ω	MIN 25°C MAX	$V_{is} = V_{EE}$ Note 2
				100			65			40				
				150			110			70				
				1750			100			50		Ω	MIN 25°C MAX	Note 3
				1000			125			60				
				700			220			100				
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels						10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\bar{E} = V_{DD}$, $V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						80						
	Any Channel OFF	XC						100						$\bar{E} = V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40		8		μA	MIN,25°C MAX	$V_{SS} = V_{EE}$ All Inputs Common and at 0 V or V_{DD}
					700			1400		280				
		XM			2			4		0.8		μA	MIN,25°C MAX	
					70			140		28				

Notes on following page.

13

CMOS • F4052/34052

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 4)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		20 8			7 4			4 3		ns ns	C_L = 15 pF, $\overline{E}$ = V_{SS} = V_{EE}, A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		160 200			90 120			75 90		ns ns	
t_{PZL} t_{PZH}	Output Enable Time		180 200			90 100			70 80		ns ns	C_L = 15 pF $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1000 1000			900 900			860 850		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		25 10			10 6			6 4		ns ns	C_L = 50 pF $\overline{E}$ = V_{SS} = V_{EE},
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		170 210			95 125			80 95		ns ns	A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PZL} t_{PZH}	Output Enable Time		185 205			95 105			75 85		ns ns	C_L = 50 pF $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1250 1240			1130 1120			1080 1070		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	C_L = 15 pF R_L = 10 kΩ V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ, $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) at −40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = −40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (sine wave) 20 Log_{10} (V_{os}/V_{is}) = −40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) V_{SS} = $V_{DD}/2$ 20 Log_{10} (V_{os}/V_{is}) = −3 dB

NOTES:
1. Additional DC Characteristics for the Address and Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or $V_{DD}/2$.
3. V_{is} = 8.6V for V_{DD} = 15V
   V_{is} = 5.1V for V_{DD} = 10V
   V_{is} = 1.9V for V_{DD} = 5V
4. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
5. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
6. V_{IN} = V_{DD} (Square Wave), Input Transition Times ≤20 ns and R_L = 10 kΩ.

F4066/34066
QUAD BILATERAL SWITCHES

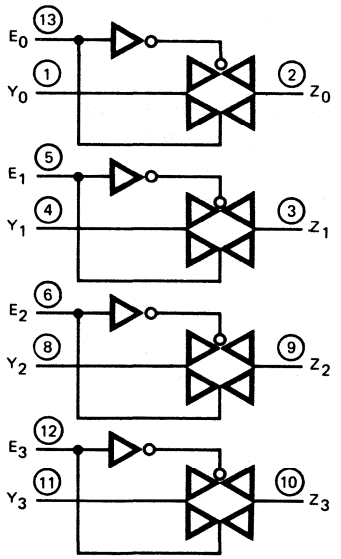
DESCRIPTION – The F4066 has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch; high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

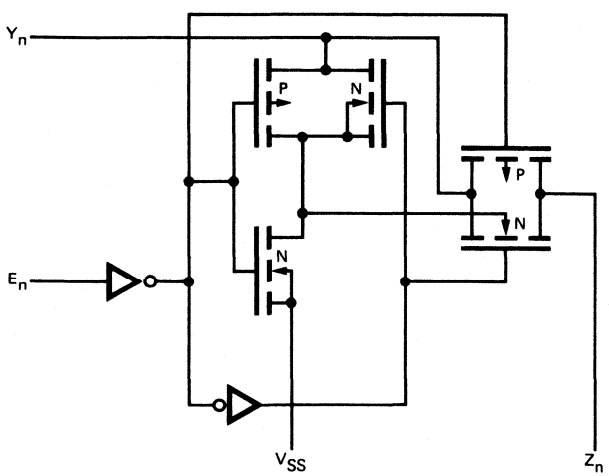
E_0 - E_3	Enable Inputs
Y_0 - Y_3	Input/Output Terminals
Z_0 - Z_3	Input/Output Terminals

LOGIC SYMBOL

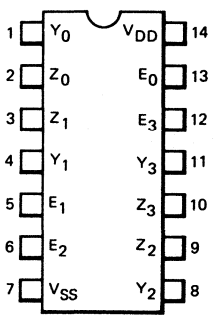


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A F4066)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

13

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		190	900		100	450		80	250	Ω	MIN	R_L = 10 kΩ
				270	1000		120	500		80	280		25°C	E_n = V_{DD},
				330	1090		170	520		130	300		MAX	V_{is} = V_{DD} to V_{SS}
		XM		160	850		85	400		60	220	Ω	MIN	R_L = 10 kΩ
				270	1000		120	500		80	280		25°C	E_n = V_{DD},
				360	1150		190	550		145	320		MAX	V_{is} = V_{DD} to V_{SS}
ΔR_{ON}	"Δ" ON Resistance Between Any Two Switches						10			5		Ω	25°C	V_{is} = V_{DD} to V_{SS}, E_n = V_{DD} R_L = 10 kΩ
I_Z	OFF State Leakage Current, Any Y to Z							100			100	nA	25°C	V_{is} = V_{DD} or V_{SS}, E_n = V_{SS}
I_{DD}	Quiescent Power Supply Current	XC			0.25			0.5		0.1		μA	MIN, 25°C	All inputs common and at V_{DD} or V_{SS}
					25			30		6			MAX	
		XM			0.25			0.5		0.1		μA	MIN, 25°C	
					25			30		6			MAX	

Notes on following page.

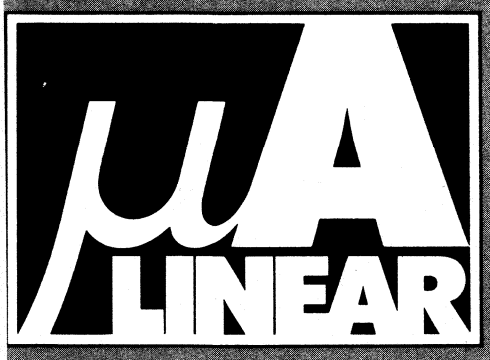
CMOS • F4066/34066

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C(See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		4 3			1.5 1.5			1 1		ns	C_L = 15 pF, R_L = 10 kΩ Input Transition Times ≤ 20 ns $E_n = V_{DD}$ $V_{is} = V_{DD}$ (square wave)
t_{PZL} t_{PZH}	Output Enable Time		24 24			14 14			10 10		ns ns	C_L = 15 pF, R_L = 300Ω $E_n = V_{DD}$ (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		160 160			170 170			182 182		ns ns	Input Transition Times ≤ 20 ns $V_{is} = V_{DD}$
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8			3 4			2 2.5		ns ns	C_L = 50 pF, R_L = 10 kΩ Input Transition Times ≤ 20 ns $E_n = V_{DD}$ $V_{is} = V_{DD}$ (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32			16 16			13 13		ns ns	C_L = 50 pF, R_L = 300Ω $E_n = V_{DD}$ (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns ns	Input Transition Times ≤ 20 ns $V_{is} = V_{DD}$
	Distortion, Sine Wave Response		0.31			0.31			0.31		%	C_L = 15 pF, R_L = 10 kΩ Input Frequency = 1 kHz $E_n = V_{DD}$ $V_{is} = V_{DD}/2$ (sine wave)
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ $E_A = V_{DD}$, $E_B = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) at -50 dB, 20 Log_{10} $[V_{os}(B)/V_{is}(A)] = -50$ dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ≤ 20 ns $R_{L(OUT)}$ = 10 kΩ, $R_{L(IN)}$ = 1 kΩ $E_n = V_{DD}$ (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ $E_n = V_{SS}$, $V_{is} = V_{DD}/2$(sine wave) 20 Log_{10} (V_{os}/V_{is}) = -50 dB
	ON State Frequency Response					90					MHz	R_L = 1 kΩ $V_{is} = V_{DD}/2$ (sine wave) $E_n = V_{DD}$, 20 Log_{10} (V_{os}/V_{is}) = -3 dB
f_{MAX}	Enable Input Frequency (Note 3)					10					MHz	C_L = 15 pF, R_L = 1 kΩ Input Transition Times ≤ 20 ns $E_n = V_{DD}$ (square wave) $V_{is} = V_{DD}$

NOTES:
1. Additional DC Characteristics for the Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).

13



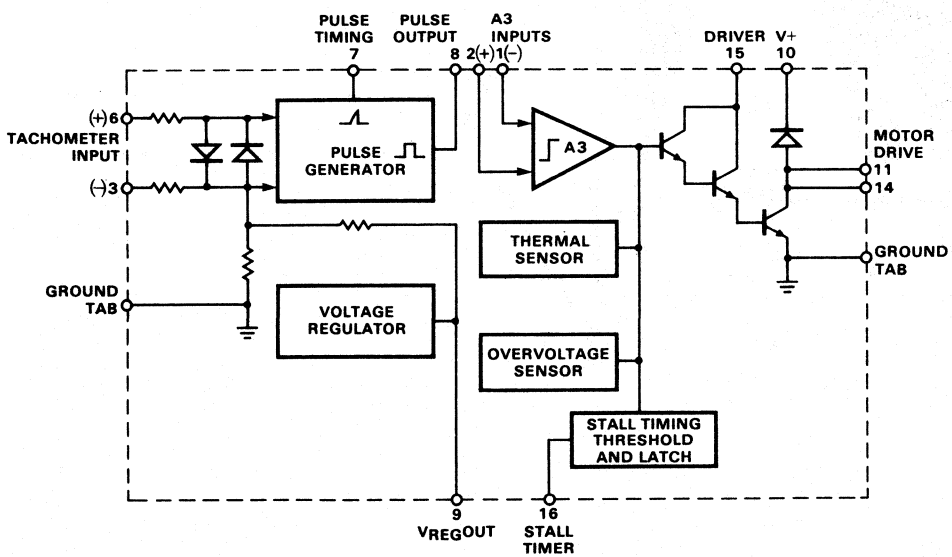
SPECIAL FUNCTIONS –
NEW PRODUCTS TO BE ANNOUNCED

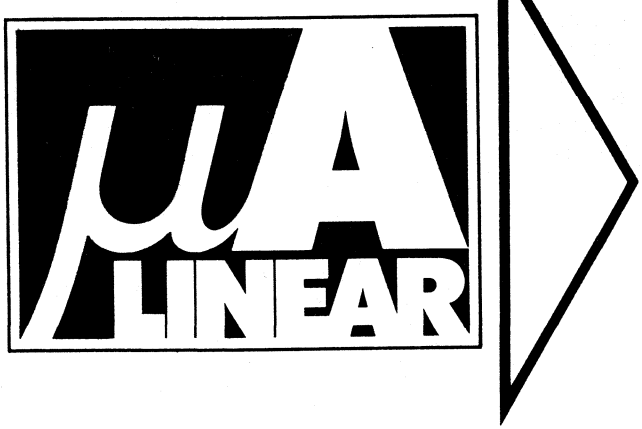
μA7391

MOTOR SPEED CONTROL SYSTEM

This monolithic IC provides all of the functional electronic blocks required for realization of a precision closed loop motor speed control system within a single power Dual In-Line Package. The μA7391 is particularly well suited for speed regulation of capstan drive motors found in automotive and portable tape players, and for application in a variety of industrial controls.

- 1% MOTOR SPEED ACCURACY OVER T_A = −30 TO +85°C, 10 TO 16 V SUPPLY RANGE
- POWER OUTPUT OF 3 AMP STARTING SURGE CURRENT AND A 2 AMP RUNNING CURRENT TO A DC MOTOR
- DRIVEN BY ANY TACHOMETER SIGNAL WAVESHAPE WITH AN AMPLITUDE OF 100 mV pk-pk OR GREATER
- SYSTEM PERFORMANCE PARAMETERS CONTROLLED BY A FEW PASSIVE EXTERNAL COMPONENTS
- SYSTEM PROTECTION FOR BOTH THE μA7391 AND MOTOR





INDEX

INDEX

μA104 • μA304
NEGATIVE VOLTAGE REGULATORS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

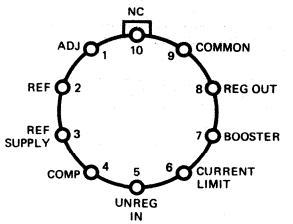
GENERAL DESCRIPTION – The 104 family of Precision Negative Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. This device can be programmed by a single external resistor to supply any voltage from 0 V to 30 V from a single unregulated supply. When used with a separate floating bias supply, the 104/304 can provide 0.01% regulation with the output voltage limited only by the breakdown of external pass transistors. The 104 and 304 provide complementary operation with the 105 positive regulator family. Although primarily designed as a linear series regulator, the 104 family can be used as a current regulator, switching regulator, or in control applications. Without external pass elements, the device can supply currents up to 25 mA; with external pass transistors, the output current is limited only by the capacity of the pass transistors. External resistors establish the output voltage and either constant or fold-back current limiting.

- **1 mV REGULATION WITH FULL LOAD**
- **0.01%/V LINE REGULATION**
- **0.2 mV/V RIPPLE REJECTION**
- **0.3% TEMPERATURE STABILITY OVER FULL TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
μA104	50 V
μA304	40 V
Input/Output Voltage Differential	
μA104	50 V
μA304	40 V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Military grade (μA104)	–55°C to +125°C
Commercial grade (μA304)	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 s)	300°C

CONNECTION DIAGRAM
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F
PACKAGE CODE H

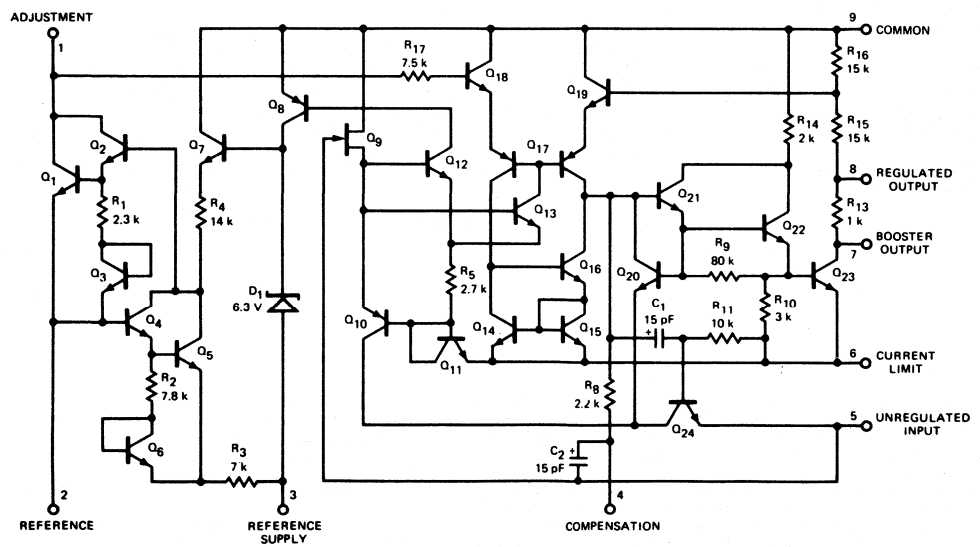


Note: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA104	μA104HM
μA304	μA304HC

EQUIVALENT CIRCUIT



Notes on following pages.

*Planar is a patented Fairchild process.

μA104

ELECTRICAL CHARACTERISTICS (V_{IN} = –50 V to –8.0 V, T_A = –55°C to 125°C, unless otherwise specified), Note 2.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			–50		–8.0	V
Output Voltage Range			–40		–0.015	V
Output/Input Voltage Differential (Note 3)	I_L = 20 mA		2.0		50	V
	I_L = 5 mA		0.5		50	V
Load Regulation (Note 4)	$0 \leq I_L \leq 20$ mA, R_{SC} = 15 Ω			1.0	5.0	mV
Line Regulation (Note 5)	$V_O \leq -5$ V, ΔV_{IN} = 0.1 V_{IN}			0.056	0.1	%
Ripple Rejection	C2 = 10 μF, f = 120 Hz,	$V_{IN} \geq -15$ V		0.2	0.5	mV/V
		-7 V $\geq V_{IN} \geq -15$ V		0.5	1.0	mV/V
Output Voltage Scale Factor V_O/R2	R1 = 2.4 kΩ		1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_O \leq -1$ V, $-55°C \leq T_A \leq 125°C$			0.3	1.0	%
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, $V_O \leq -5$ V,	C2 = 0		0.007		%
		C2 = 10 μF		15		μV
Standby Current Drain	I_L = 5 mA	V_O = 0		1.7	2.5	mA
		V_O = –40 V		3.6	5.0	mA
Long Term Stability	$V_O \leq -1$ V			0.1	1.0	%

μA304

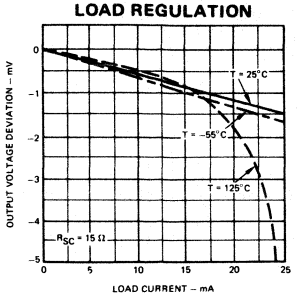
ELECTRICAL CHARACTERISTICS (V_{IN} = –40 V to –8.0 V, T_A = 0°C to 70°C, unless otherwise specified), Note 2.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			–40		–8.0	V
Output Voltage Range			–30		–0.035	V
Output/Input Voltage Differential (Note 3)	I_L = 20 mA		2.0		40	V
	I_L = 5 mA		0.5		40	V
Load Regulation (Note 4)	$0 \leq I_L \leq 20$ mA, R_{SC} = 15 Ω			1.0	5.0	mV
Line Regulation (Note 5)	$V_O \leq -5$ V, ΔV_{IN} = 0.1 V_{IN}			0.056	0.1	%
Ripple Rejection	C2 = 10 μF, f = 120 Hz,	$V_{IN} < -15$ V		0.2	0.5	mV/V
		-7 V $\geq V_{IN} \geq -15$ V		0.5	1.0	mV/V
Output Voltage Scale Factor V_O/R2	R1 = 2.4 kΩ		1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_O \leq -1$ V, $0°C \leq T_A \leq 70°C$			0.3	1.0	%
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, $V_O \leq -5$ V,	C2 = 0		0.007		%
		C2 = 10 μF		15		μV
Standby Current Drain	I_L = 5 mA	V_O = 0		1.7	2.5	mA
		V_O = –30 V		3.6	5.0	mA
Long Term Stability	$V_O \leq -1$ V			0.1	1.0	%

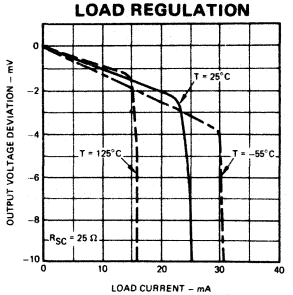
NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation. See Basic Regulator Circuit.
3. When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1 V.
4. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
5. With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0 V and –5 V, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

TYPICAL PERFORMANCE CURVES FOR μA104

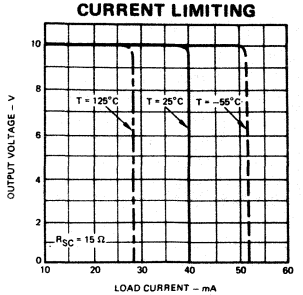
LOAD REGULATION



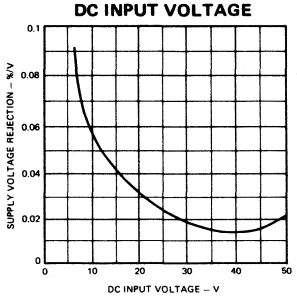
LOAD REGULATION



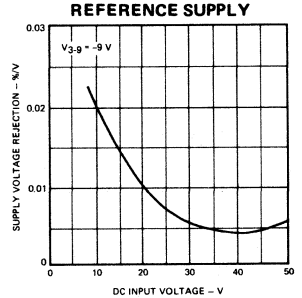
CURRENT LIMITING



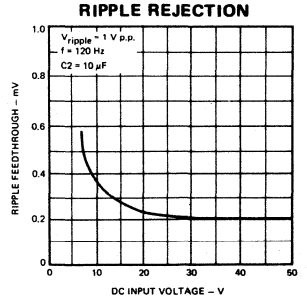
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF DC INPUT VOLTAGE



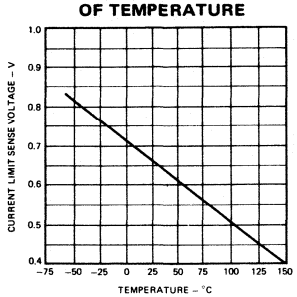
SUPPLY VOLTAGE REJECTION WITH PREREGULATED REFERENCE SUPPLY



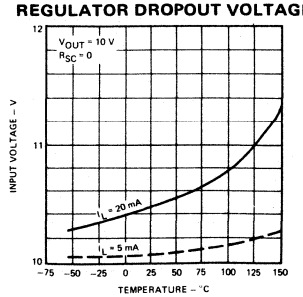
RIPPLE REJECTION



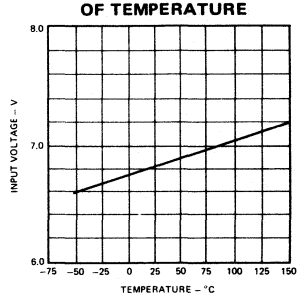
CURRENT LIMIT SENSE VOLTAGE AS A FUNCTION OF TEMPERATURE



REGULATOR DROPOUT VOLTAGE



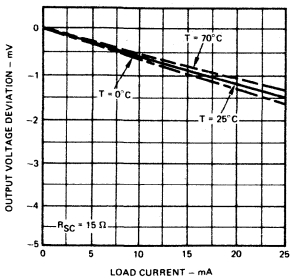
MINIMUM INPUT VOLTAGE AS A FUNCTION OF TEMPERATURE



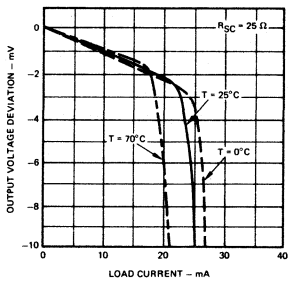
14

TYPICAL PERFORMANCE CURVES FOR μA304

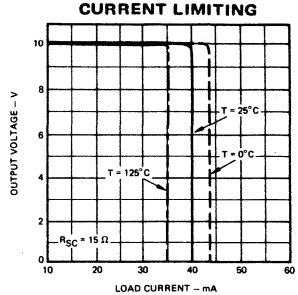
LOAD REGULATION



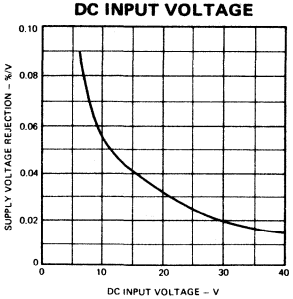
LOAD REGULATION



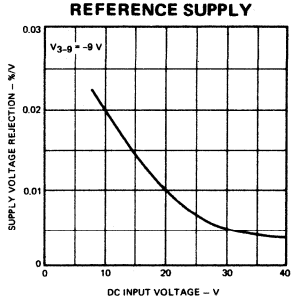
CURRENT LIMITING



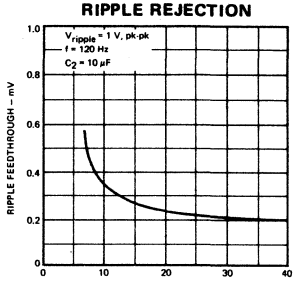
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF DC INPUT VOLTAGE



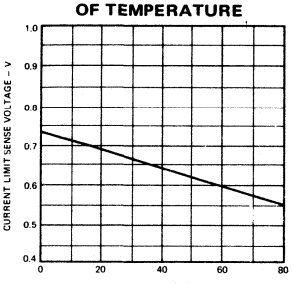
SUPPLY VOLTAGE REJECTION WITH PREREGULATED REFERENCE SUPPLY



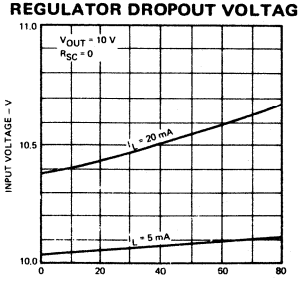
RIPPLE REJECTION



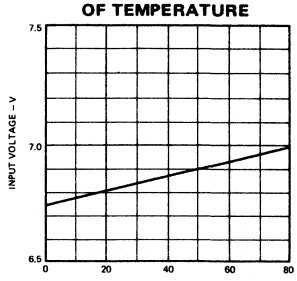
CURRENT LIMIT SENSE VOLTAGE AS A FUNCTION OF TEMPERATURE



REGULATOR DROPOUT VOLTAGE

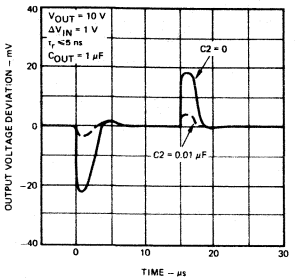


MINIMUM INPUT VOLTAGE AS A FUNCTION OF TEMPERATURE

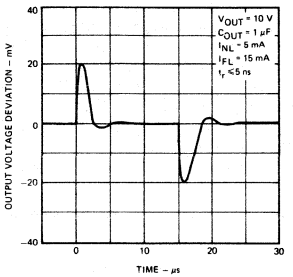


TYPICAL PERFORMANCE CURVES FOR μA104 AND μA304

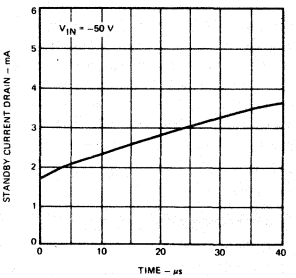
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE

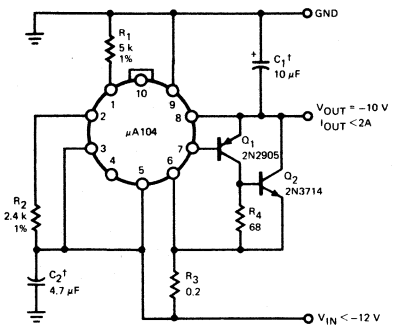


STANDBY CURRENT DRAIN AS A FUNCTION OF TIME



TYPICAL APPLICATIONS

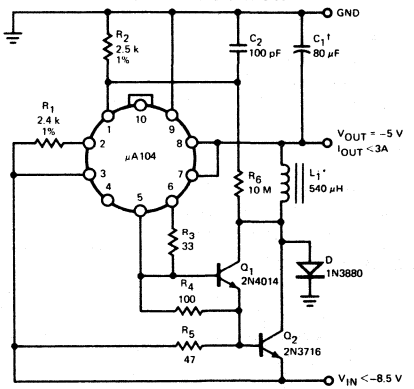
HIGH CURRENT REGULATOR



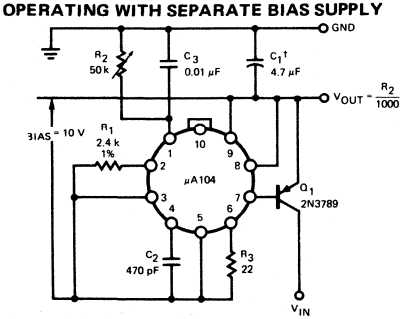
†Solid Tantalum

†Solid Tantalum
*60 Turns #20 on Arnold Engineering A930157-2 Molybdenum Permalloy Core.

SWITCHING REGULATOR

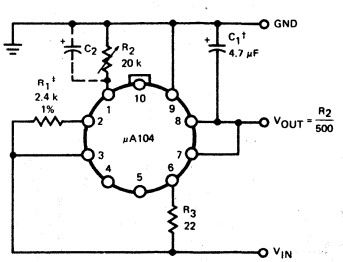


OPERATING WITH SEPARATE BIAS SUPPLY



†Solid Tantalum

BASIC REGULATOR CIRCUIT



†Solid Tantalum
‡Trim R_1 for exact scale factor

NOTE:

A 0.01 μF capacitor may be required across the input if long leads are used from the unregulated power source. Line transient response, noise and ripple rejection can be improved by shunting R2 with a 10 μF capacitor C2.

14

μA105 • μA305 • μA305A • μA376

VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

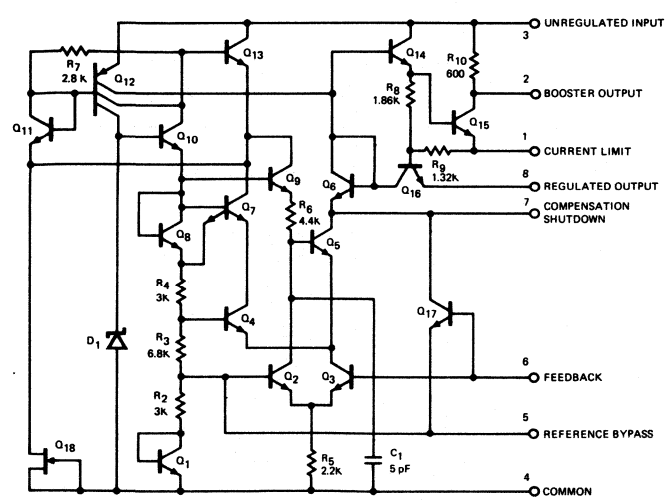
GENERAL DESCRIPTION – The 105/305/305A/376 are monolithic Positive Voltage Regulators constructed using the Fairchild Planar* epitaxial process. Applications for these devices include both linear and switching regulator circuits with output voltages greater than 4.5 V. These devices will not oscillate when confronted with varying resistive and reactive loads and will start reliably regardless of the load within the ratings of the circuit. They also feature fast response to both load and line transients. Used independently, the 105/305 will supply 12 mA, the 305A, 45 mA and 376, 25 mA. The 105 is specified for the military temperature range (−55°C to +125°C) and the 305/376/305A are specified for 0°C to +70°C operation. The 105/305/305A are in an 8-lead TO-5 package and the 376 is available in the space and cost saving mini DIP.

- **LOW STANDBY CURRENT DRAIN**
- **ADJUSTABLE OUTPUT VOLTAGE FROM 4.5 V TO 40 V**
- **HIGH OUTPUT CURRENTS EXCEEDING 10A WITH EXTERNAL COMPONENTS**
- **LOAD REGULATION BETTER THAN 0.1%, FULL LOAD WITH CURRENT LIMITING**
- **DC LINE REGULATION GUARANTEED AT 0.03%/V**
- **RIPPLE REJECTION OF 0.01%/V**

ABSOLUTE MAXIMUM RATINGS

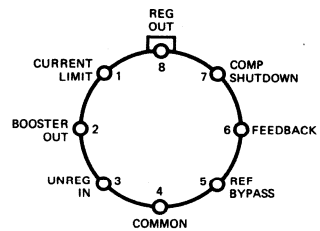
Input Voltage	
μA105, μA305A	50 V
μA305, μA376	40 V
Input/Output Voltage Differential	40 V
Internal Power Dissipation (Note 1)	
μA105, μA305, μA305A	500 mW
μA376	450 mW
Operating Temperature Range	
Military (μA105)	−55°C to +125°C
Commercial (μA305, μA305A, μA376)	0°C to +70°C
Storage Temperature Range	
Metal Can	−65°C to +150°C
Mini DIP	−55°C to +125°C
Lead Temperature	
Metal Can (Soldering, 60 s)	300°C
Mini DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



PIN CONNECTIONS SHOWN ARE FOR METAL CAN

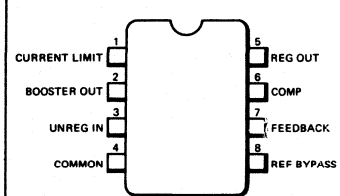
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA105	μA105HM
μA305	μA305HC
μA305A	μA305AHC

8-LEAD MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE TC



ORDER INFORMATION

TYPE	PART NO.
μA376	μA376TC

Notes on following pages.

*Planar is a patented Fairchild process.

μA105

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			8.5		50	V
Output Voltage Range			4.5		40	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 12$ mA	R_{SC} = 10Ω, T_A = 25°C		0.02	0.05	%
		R_{SC} = 10Ω, T_A = 125°C		0.03	0.1	%
		R_{SC} = 10Ω, T_A = −55°C		0.03	0.1	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	C_{REF} = 10 μF, f = 120 Hz			0.003	0.01	%/V
Temperature Stability (Note 5)	−55°C ≤ T_A ≤ 125°C			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	C_{REF} = 0		0.005		%
		$C_{REF} > 0.1$ μF		0.002		%
Current Limit Sense Voltage (Note 4)	R_{SC} = 10Ω, T_A = 25°C V_O = 0 V		225	300	375	mV
Standby Current Drain	V_{IN} = 50 V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

μA305

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			8.5		40	V
Output Voltage Range			4.5		30	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 12$ mA	R_{SC} = 10Ω, T_A = 25°C		0.02	0.05	%
		R_{SC} = 15Ω, T_A = 70°C		0.03	0.1	%
		R_{SC} = 10Ω, T_A = 0°C		0.03	0.1	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	C_{REF} = 10 μF, f = 120 Hz			0.003	0.01	%/V
Temperature Stability (Note 5)	0°C ≤ T_A ≤ 70°C			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	C_{REF} = 0		0.005		%
		$C_{REF} > 0.1$ μF		0.002		%
Current Limit Sense Voltage (Note 4)	R_{SC} = 10Ω, T_A = 25°C V_O = 0 V		225	300	375	mV
Standby Current Drain	V_{IN} = 40 V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.25 mW/°C for the metal can and 5.6 mW/°C for the mini Dip.
2. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.
5. Temperature Stability is defined as the percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

μA305A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			8.5		50	V
Output Voltage Range			4.5		40	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 45$ mA	R_{SC} = 0Ω, T_A = 25°C		0.02	0.2	%
		R_{SC} = 0Ω, T_A = 70°C		0.03	0.4	%
		R_{SC} = 0Ω T_A = 0°C		0.03	0.4	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	C_{REF} = 10 μF, f = 120 Hz			0.003		%/V
Temperature Stability (Note 5)	0°C ≤ T_A ≤ 70°C			0.3	1.0	%
Feedback Sense Voltage			1.55	1.7	1.85	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	C_{REF} = 0		0.005		%
		$C_{REF} > 0.1$ μF		0.002		%
Current Limit Sense Voltage (Note 4)	R_{SC} = 10Ω, T_A = 25°C, V_O = 0 V		225	300	375	mV
Standby Current Drain	V_{IN} = 50 V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

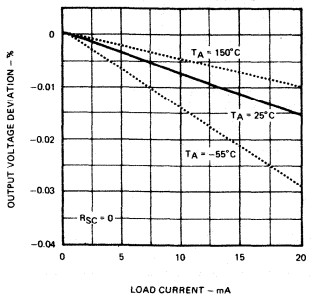
μA376

ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ 70°C

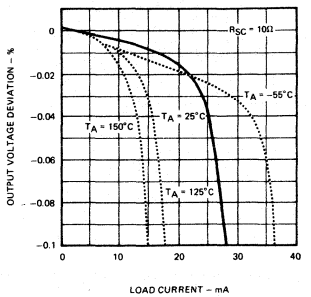
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			9.0		40	V
Output Voltage Range			5.0		37	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation	$0 \leq I_L \leq 25$ mA	R_{SC} = 0Ω, T_A = 25°C			0.2	%
		R_{SC} = 0Ω, T_A = 70°C			0.5	%
		R_{SC} = 0Ω, T_A = 0°C			0.5	%
Line Regulation					0.03	%/V
					0.1	%/V
Ripple Rejection	f = 120 Hz, T_A = 25°C				0.1	%/V
Standby Current Drain	V_{IN} = 30 V, T_A = 25°C				2.5	mA
Reference Voltage			1.60	1.72	1.80	V
Current Limit Sense Voltage				360		mV

TYPICAL PERFORMANCE CURVES FOR μA105/μA305/μA305A

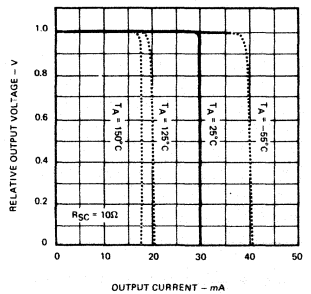
LOAD REGULATION



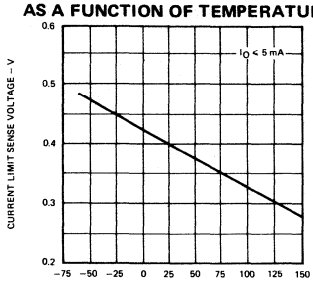
LOAD REGULATION



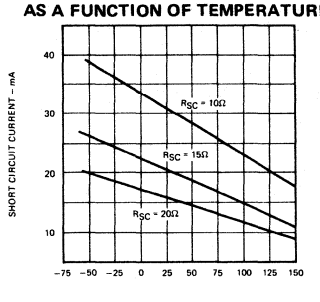
CURRENT LIMITING CHARACTERISTICS



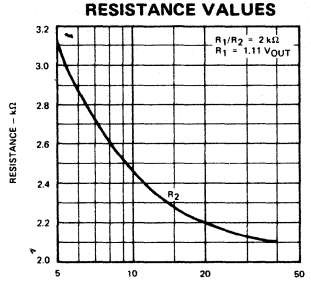
CURRENT LIMIT SENSE VOLTAGE AS A FUNCTION OF TEMPERATURE



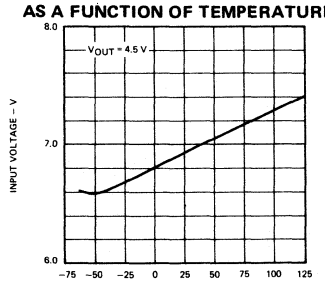
SHORT CIRCUIT CURRENT AS A FUNCTION OF TEMPERATURE



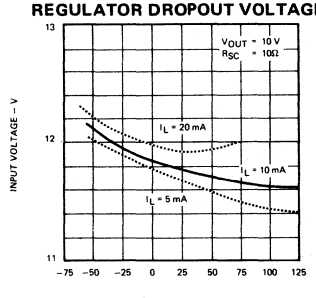
OPTIMUM DIVIDER RESISTANCE VALUES



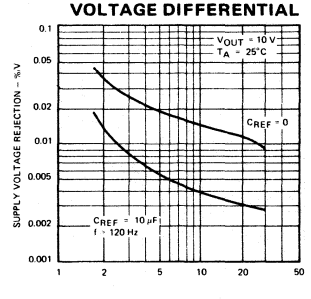
MINIMUM INPUT VOLTAGE AS A FUNCTION OF TEMPERATURE



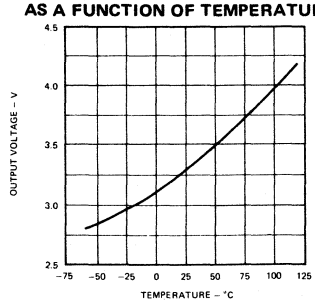
REGULATOR DROPOUT VOLTAGE



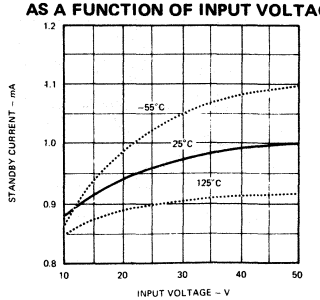
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



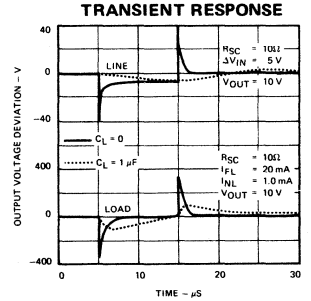
MINIMUM OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE



STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



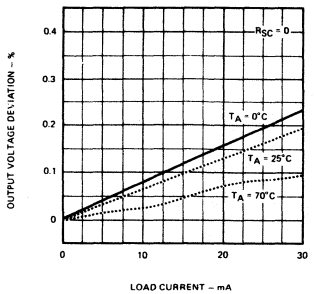
TRANSIENT RESPONSE



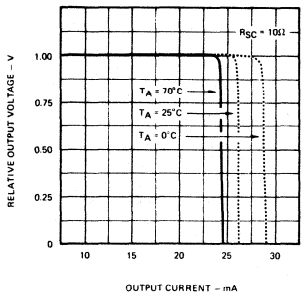
14

TYPICAL PERFORMANCE CURVES FOR μA376

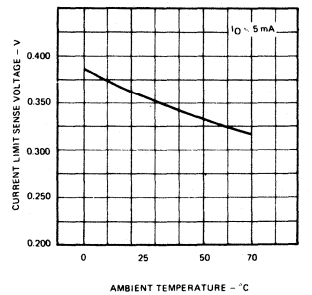
LOAD REGULATION



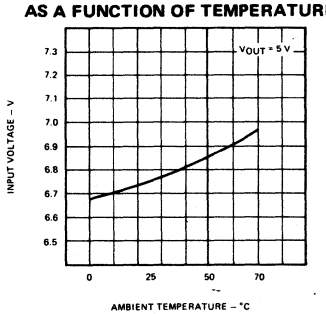
CURRENT LIMITING CHARACTERISTICS



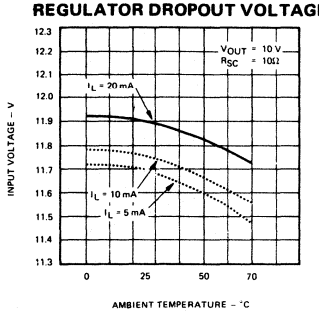
CURRENT LIMIT SENSE VOLTAGE AS A FUNCTION OF TEMPERATURE



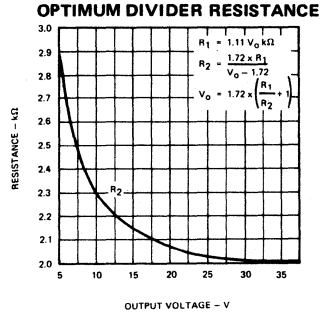
MINIMUM INPUT VOLTAGE AS A FUNCTION OF TEMPERATURE



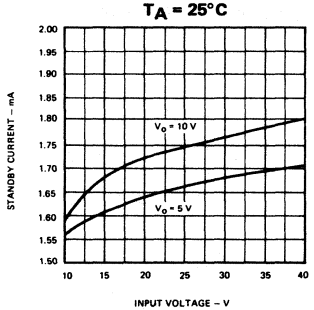
REGULATOR DROPOUT VOLTAGE



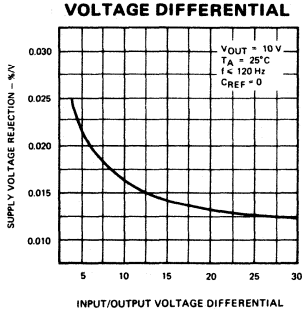
OPTIMUM DIVIDER RESISTANCE



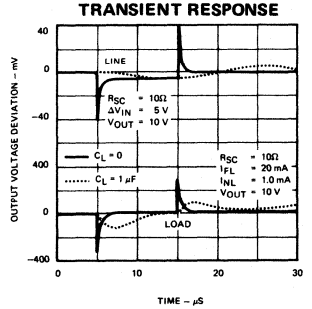
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE T_A = 25°C



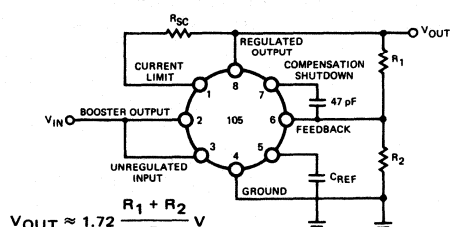
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



TRANSIENT RESPONSE



BASIC POSITIVE REGULATOR WITH CURRENT LIMITING

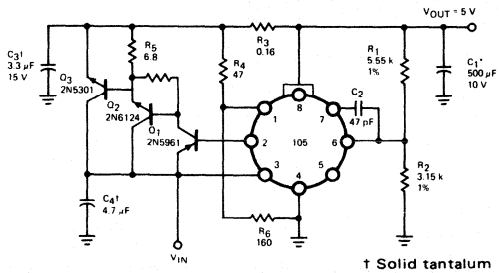


$$V_{OUT} \approx 1.72 \frac{R_1 + R_2}{R_2} V$$

$$I_{SC} \approx \frac{V_{SENSE}}{R_{SC}} mA$$

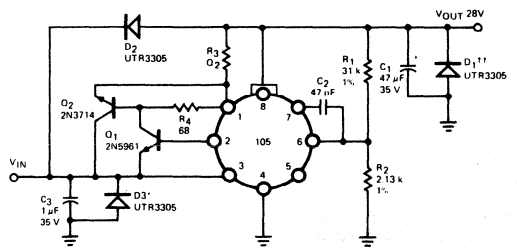
TYPICAL APPLICATIONS

10A REGULATOR WITH FOLDBACK CURRENT LIMITING



† Solid tantalum
* Electrolytic

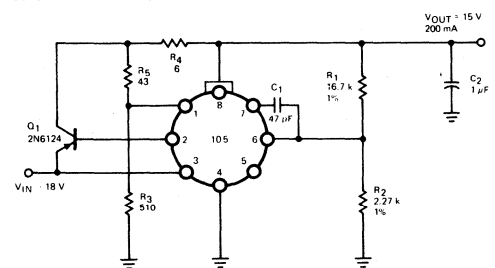
1.0A REGULATOR WITH PROTECTIVE DIODES



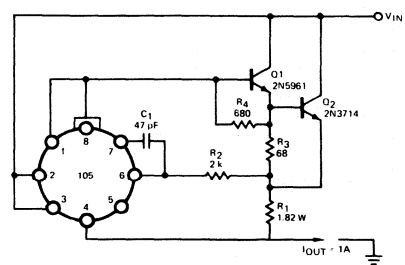
* Protects against input voltage reversal
†† Protects against output voltage reversal

† Protects against shorted input or inductive loads on unregulated supply

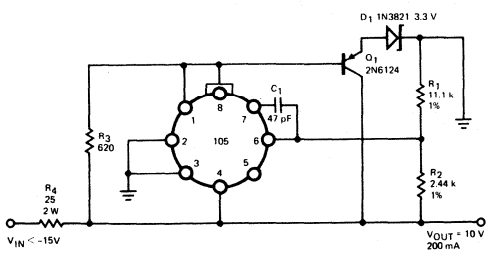
LINEAR REGULATOR WITH FOLDBACK CURRENT LIMITING



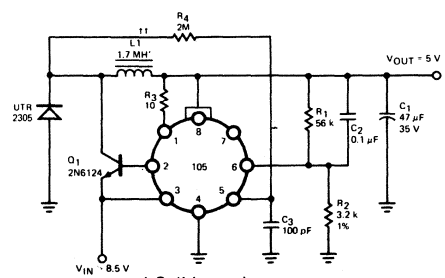
CURRENT REGULATOR



SHUNT REGULATOR



SWITCHING REGULATOR



† Solid tantalum
†† 125 turns #22 on Arnold Engineering A262123-2 molybdenum permalloy core.

14

μA109 • μA209

5 VOLT REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

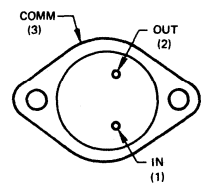
GENERAL DESCRIPTION – The 109 and 209 are complete Five Volt Regulators constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. They are intended for use as local regulators, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, they can provide over 1A output current. The 109 and 209 are intended primarily for use with TTL and DTL logic and are completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 V regulator, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- **OUTPUT CURRENT IN EXCESS OF 1 AMP**
- **SPECIFIED TO MATCH WORST CASE TTL AND DTL REQUIREMENTS**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	
Military Grade (μA109)	−55°C to +150°C
Industrial Grade (μA209)	−25°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

CONNECTION DIAGRAM
TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K

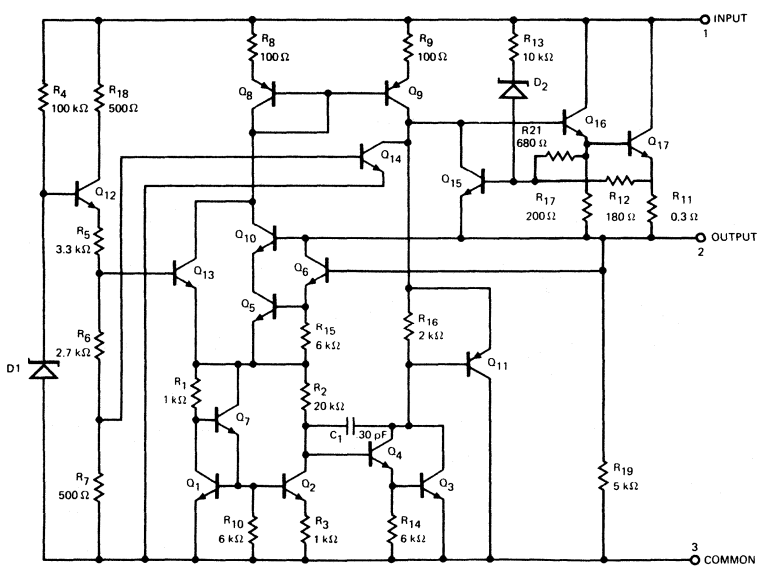


Case is connected to ground.

ORDER INFORMATION

TYPE	PART NO.
μA109	μA109KM
μA209	μA209KM

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

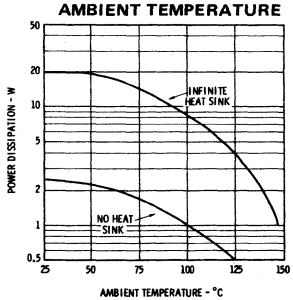
ELECTRICAL CHARACTERISTICS (T_J = −55°C to +150°C for 109, −25°C to +150°C for 209, V_{IN} = 10 V, I_{OUT} = 0.5 A, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		4.7	5.05	5.3	V
Line Regulation		T_J = 25°C, 7 V ≤V_{IN} ≤25 V			4	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤I_{OUT} ≤1.5 A			15	100	mV
Output Voltage		8 V ≤V_{IN} ≤20 V, 5 mA ≤I_{OUT} ≤1 A, P≤15 W		4.6		5.4	V
Quiescent Current		7 V ≤V_{IN} ≤25 V				10	mA
			T_J = 25°C		4.2		mA
Quiescent Current Change	with Line	8V ≤V_{IN} ≤25 V				0.8	mA
	with Load	5 mA ≤I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤f≤100 kHz			40		μV
Long Term Stability						10	mV
Thermal Resistance Junction to Case (Note 1)					3.0		°C/W

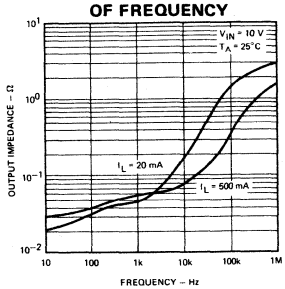
NOTE1: Without a heat sink, the thermal resistance is $\theta_{JA(max)}$ 45°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

TYPICAL PERFORMANCE CURVES FOR μA109 AND μA209

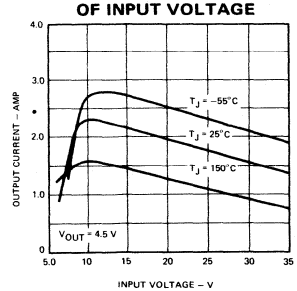
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



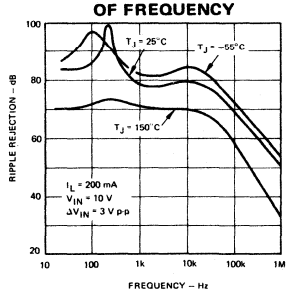
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



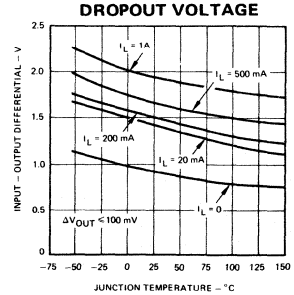
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

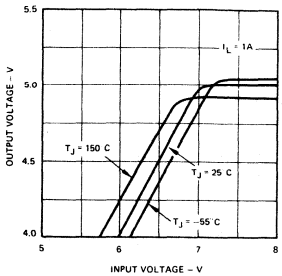


DROPOUT VOLTAGE

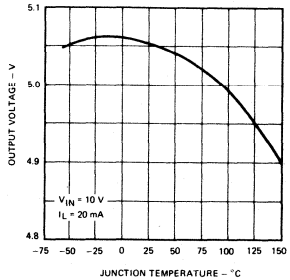


TYPICAL PERFORMANCE CURVES FOR μA109 AND μA209 (Cont'd)

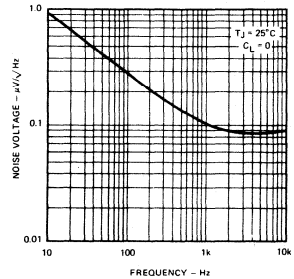
DROPOUT CHARACTERISTIC



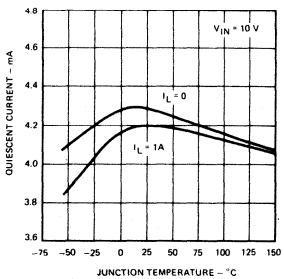
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



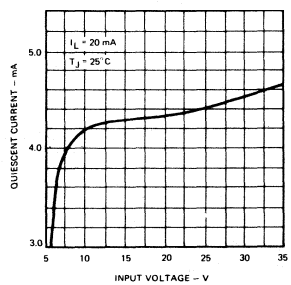
OUTPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

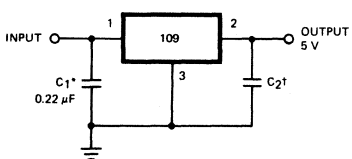


QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



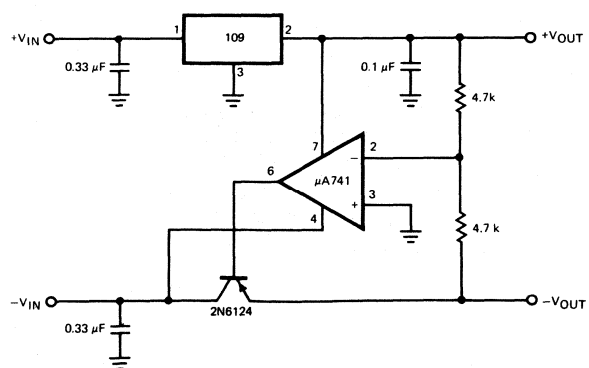
APPLICATIONS

FIXED 5 V REGULATOR



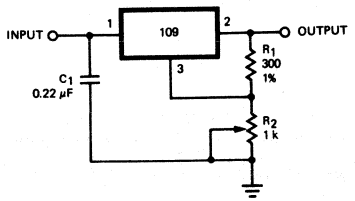
NOTES:
*Required if regulator is located an appreciable distance from power supply filter.
†Although no output capacitor is needed for stability, it does improve transient response.

TRACKING VOLTAGE REGULATOR

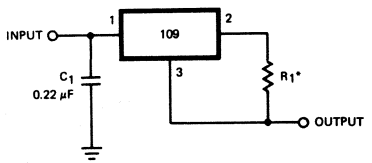


APPLICATIONS (Cont'd)

ADJUSTABLE OUTPUT REGULATOR

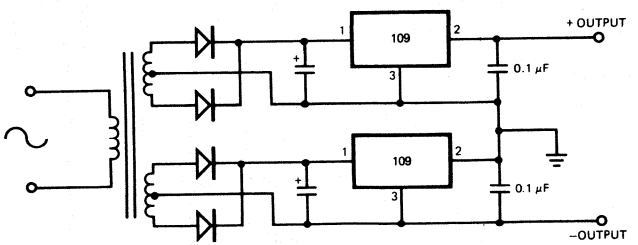


CURRENT REGULATOR



NOTE: *Determines output current.

POSITIVE AND NEGATIVE REGULATOR



14

μA309

5 VOLT REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

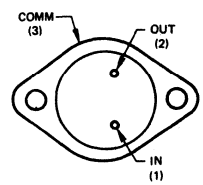
GENERAL DESCRIPTION – The 309 is a monolithic 5 Volt Regulator constructed using the Fairchild Planar* epitaxial process. This regulator employs internal current limiting, thermal shutdown and safe-area compensation making it essentially indestructable. The 309 is intended for use as a local regulator, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, it can provide over 1A output current. The 309 is intended primarily for use with TTL and DTL logic and is completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 volt regulator, this device can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- **OUTPUT CURRENT IN EXCESS OF 1 AMP**
- **SPECIFIED TO MATCH WORST CASE TTL AND DTL REQUIREMENTS**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **INTERNAL SHORT CIRCUIT LIMITING**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	0°C to +125°C
Lead Temperature (Soldering, 60 s time limit)	300°C

CONNECTION DIAGRAM
TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K

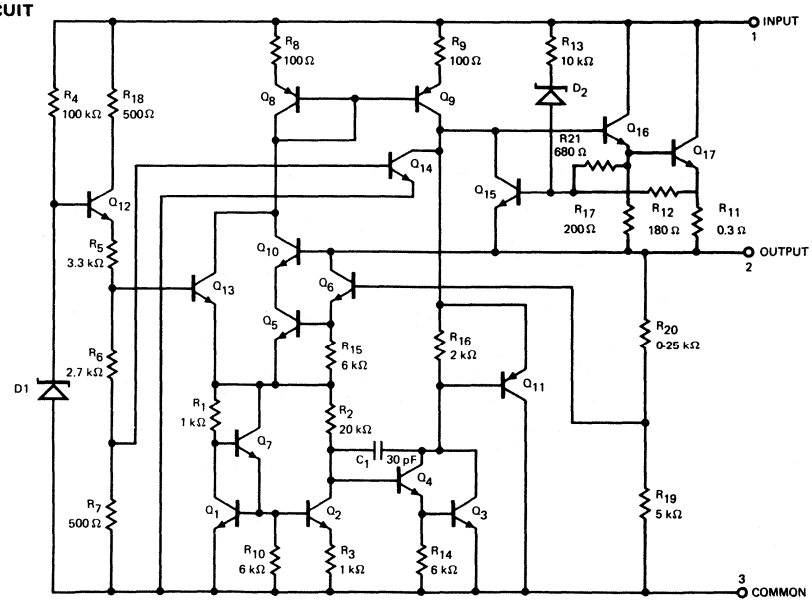


Case is connected to ground.

ORDER INFORMATION

TYPE	PART NO.
μA309	μA309KC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage		$T_J = 25°C$	4.8	5.05	5.2	V
Line Regulation		$T_J = 25°C$ $7.0\ V \leq V_{IN} \leq 25\ V$		4.0	50	mV
Load Regulation		$T_J = 25°C$ $5.0\ mA \leq I_{OUT} \leq 1.5\ A$		50	100	mV
Output Voltage		$7.0\ V \leq V_{IN} \leq 25\ V$ $5.0\ mA \leq I_{OUT} \leq 1.0\ A$ $P \leq 20\ W$	4.75		5.25	V
Quiescent Current		$7.0\ V \leq V_{IN} \leq 25\ V$		5.2	10	mA
Quiescent Current Change	with line	$7.0\ V \leq V_{IN} \leq 25\ V$			0.5	mA
	with load	$5.0\ mA \leq I_{OUT} \leq 1.0\ A$			0.8	mA
Output Noise Voltage		$T_A = 25°C$ $10\ Hz \leq f \leq 100\ kHz$		40		μV
Long Term Stability					20	mV

NOTE:
1. Unless otherwise specified, these specifications apply for $0°C \leq T_J \leq 125°C$, $V_{IN} = 10\ V$ and $I_{OUT} = 0.5\ A$.

DESIGN CONSIDERATIONS

μA309 regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

PACKAGE	TYP θ_{JC}	MAX θ_{JC}	TYP θ_{JA}	MAX θ_{JA}
TO-3	3.5°C/W	5.5°C/W	40°C/W	45°C/W

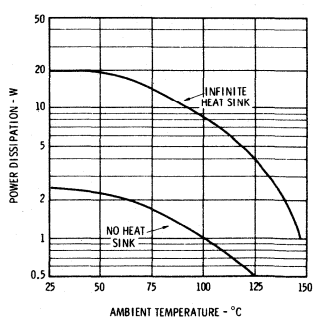
$$P_D\ (MAX) = \frac{T_J\ (MAX) - T_A}{\theta_{JC} + \theta_{CA}} \quad \text{or} \quad \frac{T_J\ (MAX) - T_A}{\theta_{JA}} \quad \text{(Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J: $T_J = T_A + P_D\ (\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where T_J = Junction Temperature; T_A = Ambient Temperature; P_D = Power Dissipation; θ_{JA} = Junction to ambient thermal resistance; θ_{JC} = Junction to case thermal resistance; θ_{CA} = Case to ambient thermal resistance; θ_{CS} = Case to ambient thermal resistance; θ_{SA} = Heat sink to ambient thermal resistance

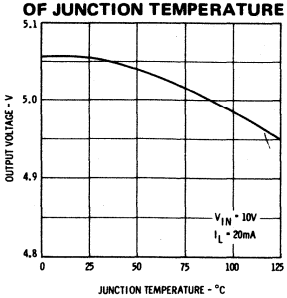
TO-3 PACKAGE MAXIMUM AVERAGE POWER DISSIPATION



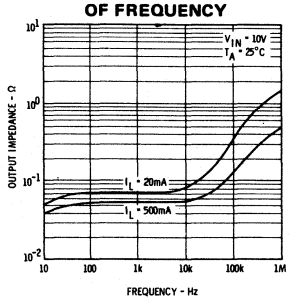
14

TYPICAL PERFORMANCE CURVES

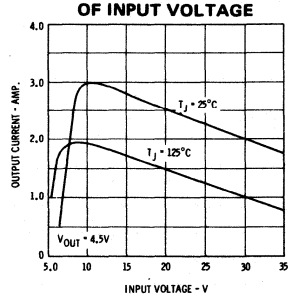
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



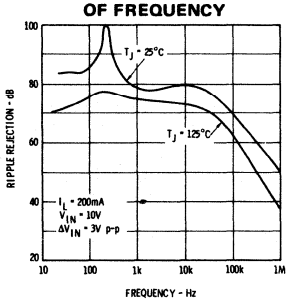
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



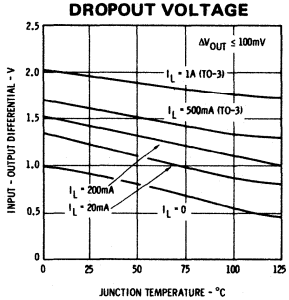
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



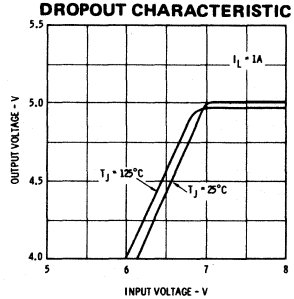
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



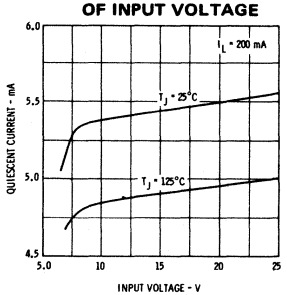
DROPOUT VOLTAGE



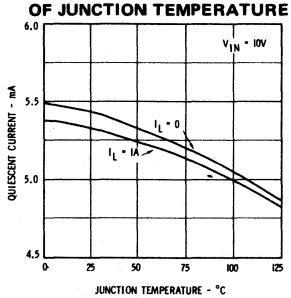
DROPOUT CHARACTERISTIC



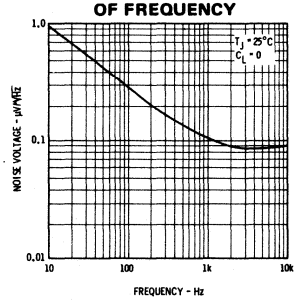
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

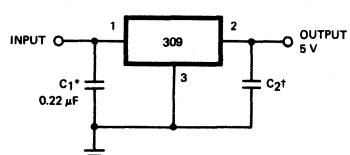


OUTPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



APPLICATIONS

FIXED 5 V REGULATOR

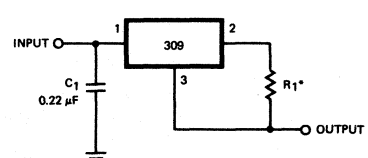


NOTES:

*Required if regulator is located an appreciable distance from power supply filter.

†Although no output capacitor is needed for stability, it does improve transient response.

CURRENT REGULATOR



NOTES:

*Determines output current.

μA723
PRECISION VOLTAGE REGULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

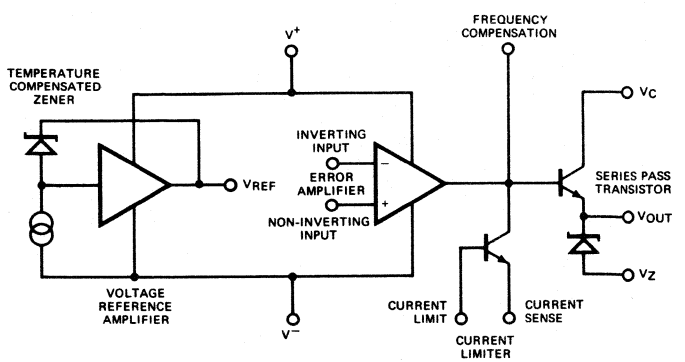
GENERAL DESCRIPTION – The μA723 is a monolithic Voltage Regulator constructed using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

ABSOLUTE MAXIMUM RATINGS

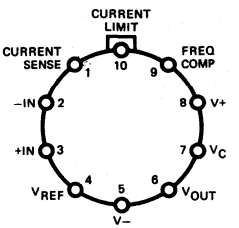
Pulse Voltage from V+ to V–, (50 ms) (μA723)	50 V
Continuous Voltage from V_+ to V_-	40 V
Input/Output Voltage Differential	40 V
Differential Input Voltage	±5 V
Voltage Between Non-Inverting Input and V_-	+8 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	
Metal Can	800 mW
DIP	1000 mW
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	
Military (μA723)	–55°C to +125°C
Commercial (μA723C)	0°C to +70°C
Lead Temperature (Soldering, 60 s)	300°C

EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAMS
10-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5F
PACKAGE CODE H

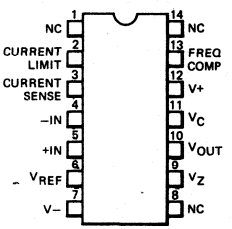


Note: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA723	μA723HM
μA723C	μA723HC

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA723	μA723DM
μA723C	μA723DC
μA723C	μA723PC

*Planar is a patented Fairchild process.

μA723

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V+ = V_C = 12$ V, $V- = 0$, $V_{OUT} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, C1 = 100 pF, $C_{ref} = 0$ and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in Fig. 1, Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Line Regulation	$V_{IN} = 12V$ to $V_{IN} = 15V$		0.01	0.1	$\%V_O$
	$V_{IN} = 12V$ to $V_{IN} = 40V$		0.02	0.2	$\%V_O$
	$-55°C \leq T_A \leq +125°C$, $V_{IN} = 12V$ to $V_{IN} = 15V$			0.3	$\%V_O$
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		0.03	0.15	$\%V_O$
	$-55°C \leq T_A \leq +125°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	$\%V_O$
Ripple Rejection	f = 50 Hz to 10 kHz		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leq T_A \leq +125°C$		0.002	0.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10$ Ω, $V_O = 0$		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30V$		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

μA723C

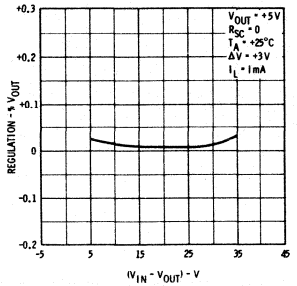
ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V+ = V_C = 12$ V, $V- = 0$, $V_{OUT} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, C1 = 100 pF, $C_{ref} = 0$ and divider impedance as see by error amplifier ≤ 10 kΩ connected as shown in Fig. 1. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

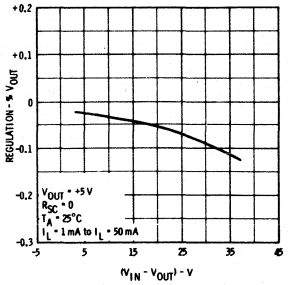
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Line Regulation	$V_{IN} = 12V$ to $V_{IN} = 15V$		0.01	0.1	$\%V_O$
	$V_{IN} = 12V$ to $V_{IN} = 40V$		0.1	0.5	$\%V_O$
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12V$ to $V_{IN} = 15V$			0.3	$\%V_O$
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		0.03	0.2	$\%V_O$
	$0°C \leq T_A \leq 70°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	$\%V_O$
Ripple Rejection	f = 50 Hz to 10 kHz		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		0.003	0.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10$ Ω, $V_O = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30V$		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

TYPICAL PERFORMANCE CURVES FOR μA723 AND μA723C

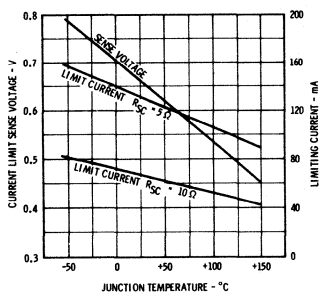
LINE REGULATION AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



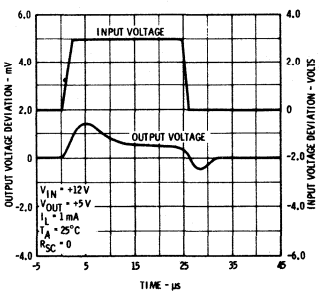
LOAD REGULATION AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



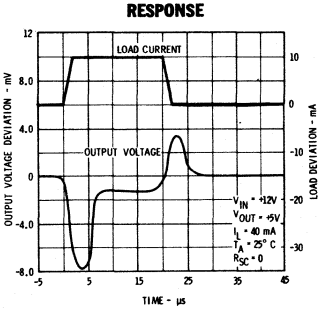
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



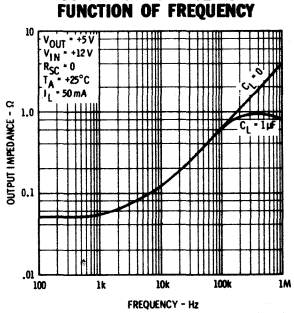
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



NOTES:

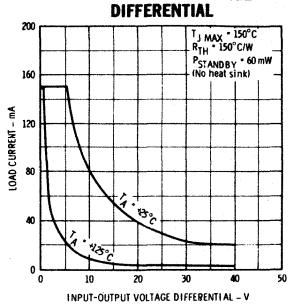
1. Rating applies to ambient temperatures up to 25°C. Above 25°C ambient derate based on the following thermal resistance values:

	θ_{JA}	
	TYP	MAX
TO-5	150	190
Plastic DIP	150	190
Ceramic DIP	125	160

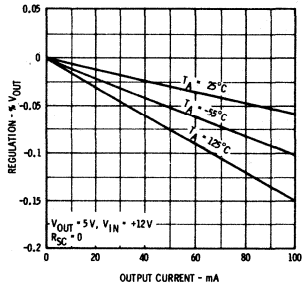
2. L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
3. Figures in parentheses may be used if R_1/R_2 divider is placed on opposite side of error amp.
4. Replace R_1/R_2 in figures with divider shown in figure 13.
5. V^+ must be connected to a +3 V or greater supply.
6. For metal can applications where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

TYPICAL PERFORMANCE CURVES FOR μA723

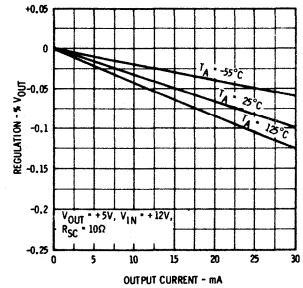
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



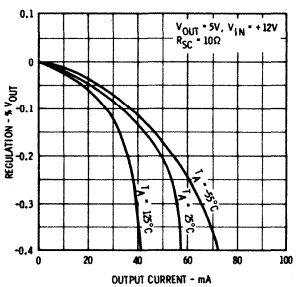
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



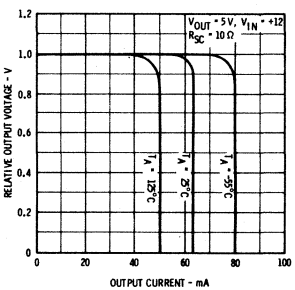
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



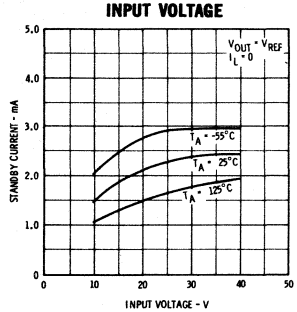
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

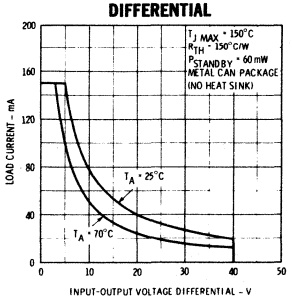


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

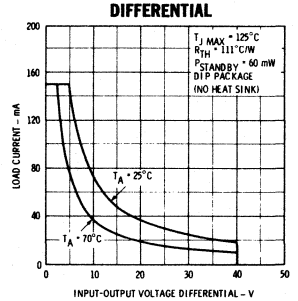


TYPICAL PERFORMANCE CURVES FOR μA723C

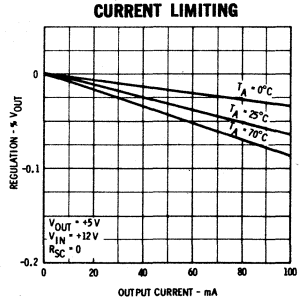
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



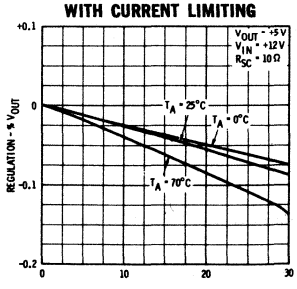
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT/OUTPUT VOLTAGE DIFFERENTIAL



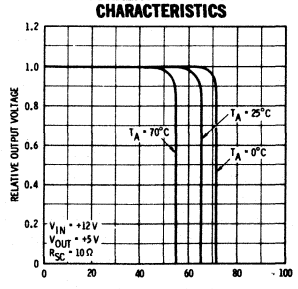
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS



STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

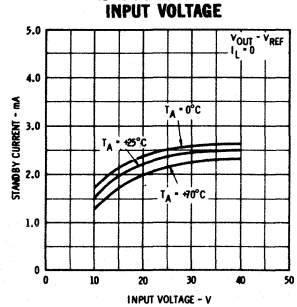


TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 4)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 3)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (Note 5)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts [Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$$

Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts [Figures 3, 8, 10]

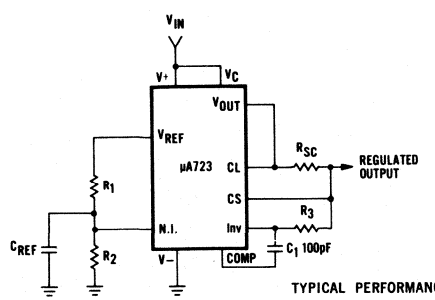
$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$$

BASIC LOW VOLTAGE REGULATOR
(V_{OUT} = 2 to 7 Volts)



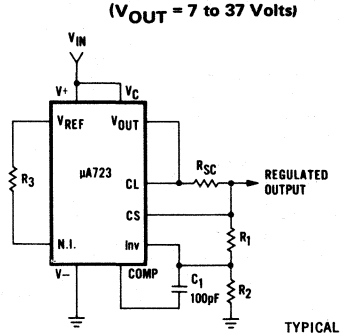
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Fig. 1

BASIC HIGH VOLTAGE REGULATOR
(V_{OUT} = 7 to 37 Volts)



TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

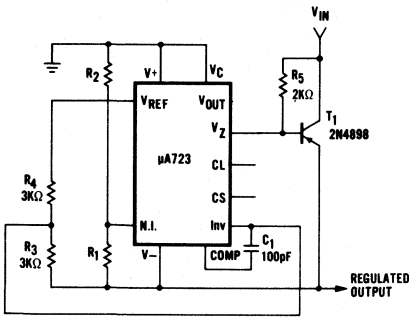
Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Fig. 2

14

NEGATIVE VOLTAGE REGULATOR



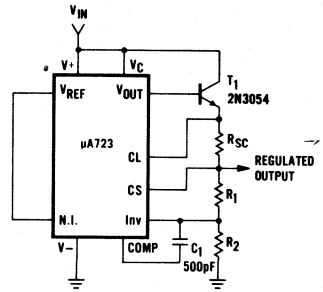
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 6

Fig. 3

POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

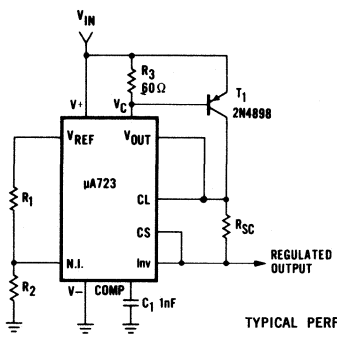


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

Fig. 4

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

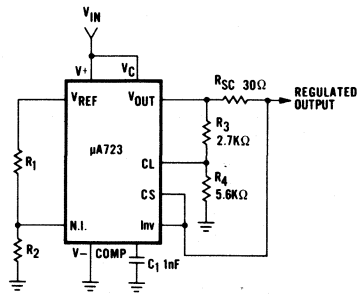


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

Fig. 5

FOLDBACK CURRENT LIMITING

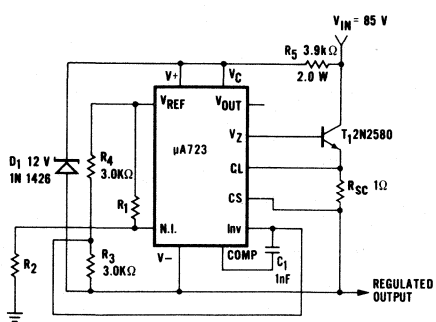


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Short Circuit Current	20 mA

Fig. 6

POSITIVE FLOATING REGULATOR



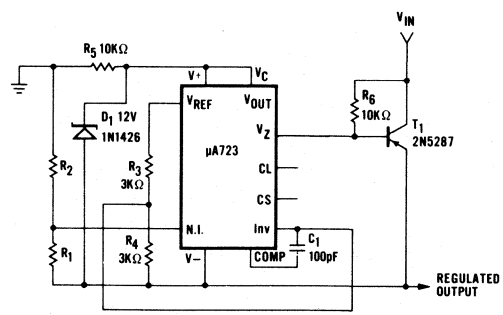
TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Note 6

Fig. 7

NEGATIVE FLOATING REGULATOR



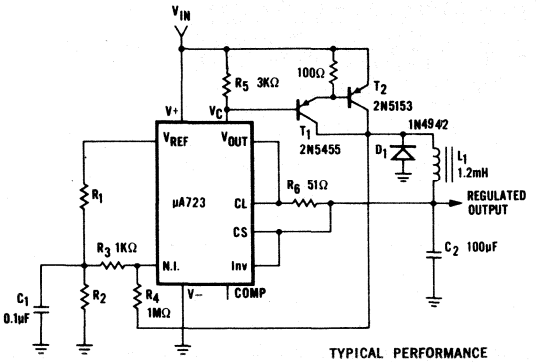
TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Note 6

Fig. 8

POSITIVE SWITCHING REGULATOR



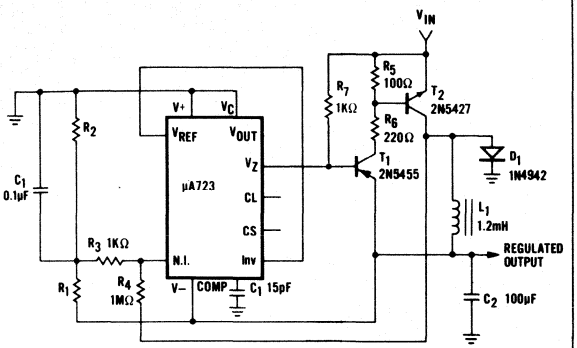
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 2

Fig. 9

NEGATIVE SWITCHING REGULATOR



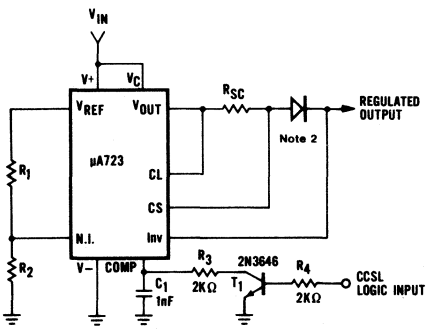
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Notes 2, 6

Fig. 10

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



Note 1: Current limit transistor may be used for shutdown if current limiting is not required.

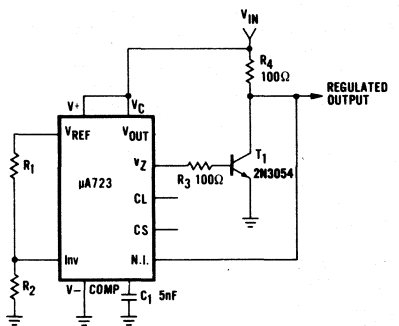
2: Add if Vout > 10V

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Fig. 11

SHUNT REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 10$ V)	0.5 mV
Load Regulation ($\Delta I_L = 100$ mA)	1.5 mV

Note 6

Fig. 12

OUTPUT VOLTAGE ADJUST

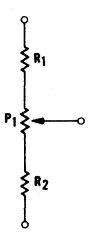
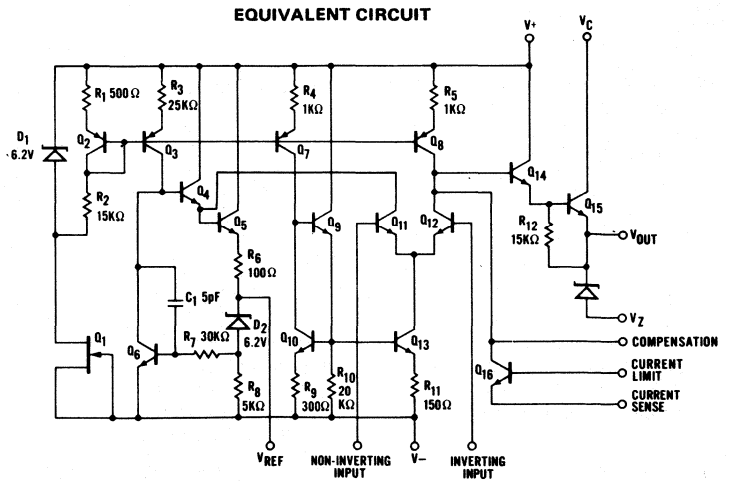


Fig. 13

EQUIVALENT CIRCUIT



14

μA78G • μA79G

4-TERMINAL POSITIVE AND NEGATIVE ADJUSTABLE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA78G and μA79G are 4-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 1.0 A with a maximum input voltage of 40 V for the positive regulator 78G and −40 V for the negative regulator 79G. Output current capability can be increased to greater than 1.0 A through use of one or more external transistors. The output voltage range of the 78G positive voltage regulator is 5 V to 30 V and the output voltage range of the negative 79G is −30 V to −2.2 V. For systems requiring both a positive and negative, the 78G and 79G are excellent for use as a dual tracking regulator with appropriate external circuitry. These 4-terminal voltage regulators are constructed using the Fairchild Planar* process.

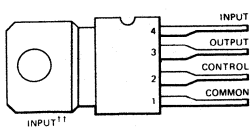
- **OUTPUT CURRENT IN EXCESS OF 1.0 A**
- **μA78G POSITIVE OUTPUT VOLTAGE 5 TO 30 V**
- **μA79G NEGATIVE OUTPUT VOLTAGE −30 TO −2.2 V**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT PROTECTION**
- **OUTPUT TRANSISTOR SAFE AREA PROTECTION**
- **MILITARY AND COMMERCIAL VERSIONS AVAILABLE**
- **AVAILABLE IN 4-PIN TO-202 TYPE AND 4-PIN TO-3**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
μA78G, μA78GC	40 V
μA79G, μA79GC	−40 V
Control Pin Voltage	
μA78G, μA78GC	$0 \leq V \leq V_{OUT}$
μA79G, μA79GC	$-V_{OUT} \leq -V \leq 0$
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
Military (μA78G, μA79G)	−55°C to 150°C
Commercial (μA78GC, μA79GC)	0°C to 150°C
Storage Temperature Range	
4-Pin Power TAB (U1)	−55°C to +150°C
4-Pin TO-3 (K)	−65°C to +150°C
Lead Temperature	
4-Pin Power TAB (U1) (Soldering, 10 s)	230°C
4-Pin TO-3 (K) (Soldering, 60 s)	300°C

μA79G CONNECTION DIAGRAMS (TOP VIEWS)

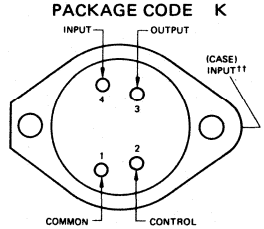
POWER TAB PACKAGE
PACKAGE OUTLINE 8Z
PACKAGE CODE U1



ORDER INFORMATION

TYPE	PART NO.
μA79GC	μA79GU1C

TO-3 PACKAGE
PACKAGE OUTLINE GK
PACKAGE CODE K



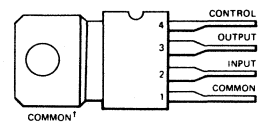
ORDER INFORMATION

TYPE	PART NO.
μA79G	μA79GKM
μA79GC	μA79GKC

††NOTE:
Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

*Planar is a patented Fairchild process.

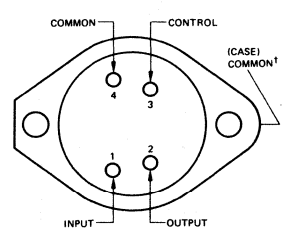
μA78G
POWER TAB PACKAGE
CONNECTION DIAGRAMS
(TOP VIEW)
PACKAGE OUTLINE 8Z
PACKAGE CODE U1



ORDER INFORMATION

TYPE	PART NO.
μA78GC	μA78GU1C

TO-3 PACKAGE
PACKAGE OUTLINE GK
PACKAGE CODE K
(TOP VIEW)

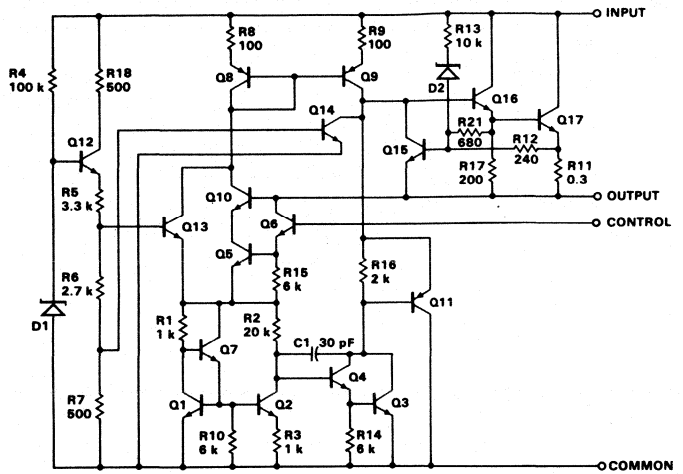


ORDER INFORMATION

TYPE	PART NO.
μA78G	μA78GKM
μA78GC	μA78GKC

†NOTE:
Heat sink tabs connected to common through device substrate.

μA78G EQUIVALENT CIRCUIT



μA78G, μA78GC

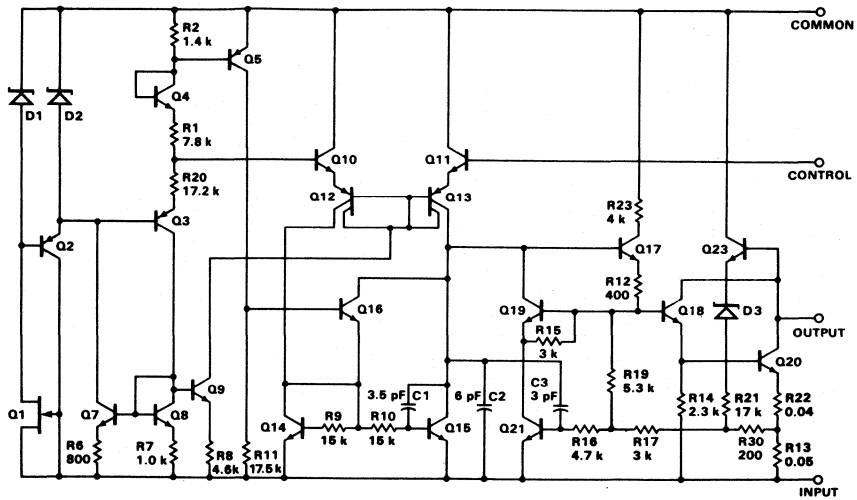
ELECTRICAL CHARACTERISTICS Unless otherwise specified, the following applies: $0°C \leq T_J \leq 125°C$ for 78GC and $-55°C \leq T_J \leq 150°C$ for 78G, $V_{IN} = 10$ V, $I_{OUT} = 500$ mA, Test Circuit 1.

PARAMETER	CONDITION (Note 1)		MIN	TYP	MAX	UNITS
Input Voltage Range	$T_J = 25°C$		7.5		40	V
Output Voltage Range	$V_{IN} = V_{OUT} + 5$ V		5.0		30	V
Output Voltage Tolerance	$V_{OUT} + 3$ V $\leq V_{IN} \leq V_{OUT} + 15$ V, 5 mA $\leq I_{OUT} \leq 1.0$ A, $P_D \leq 15$ W, $V_{IN(MAX)} = 38$ V	$T_J = 25°C$			4.0	%(V_{OUT})
					5.0	%(V_{OUT})
Line Regulation	$T_J = 25°C$, $V_{OUT} \leq 10$ V, $(V_{OUT} + 2.5\text{ V}) \leq V_{IN} \leq (V_{OUT} + 20\text{ V})$				1.0	%(V_{OUT})
	$T_J = 25°C$, $V_{OUT} \geq 10$ V, $(V_{OUT} + 3\text{ V}) \leq V_{IN} \leq (V_{OUT} + 15\text{ V})$				0.75	%(V_{OUT})
	$(V_{OUT} + 3\text{ V}) \leq V_{IN} \leq (V_{OUT} + 7\text{ V})$				0.67	
Load Regulation	$T_J = 25°C$, $V_{IN} = V_{OUT} + 5$ V	250 mA $\leq I_{OUT} \leq$ 750 mA			1.0	%(V_{OUT})
		5 mA $\leq I_{OUT} \leq$ 1.5 A			2.0	
Control Pin Current	$T_J = 25°C$			1.0	5.0	μA
					8.0	μA
Quiescent Current	$T_J = 25°C$			3.2	5.0	mA
					6.0	mA
Ripple Rejection	8 V $\leq V_{IN} \leq$ 18 V, f = 120 Hz, $V_{OUT} = 5$ V	μA78G	68	78		dB
		μA78GC	62	78		dB
Output Noise Voltage	$T_J = 25°C$, 10 Hz < f < 100 kHz, $V_{OUT} = 5$ V			40		μV
Dropout Voltage	Note 2	μA78G			3.0	V
		μA78GC			2.5	V
Short Circuit Current	$T_J = 25°C$, $V_{IN} = 30$ V			750		mA
Peak Output Current	$T_J = 25°C$			2.2		A
Average Temperature Coefficient of Output Voltage	$V_{OUT} = 5$ V, $I_{OUT} = 5$ mA			−1.1		mV/°C
Control Pin Voltage (Reference)	$T_J = 25°C$		4.8	5.0	5.2	V
			4.75		5.25	V

NOTES:

1. V_{OUT} is defined for the 78GC as $V_{OUT} = \frac{R1 + R2}{R2}(5.0)$; The 79GC as $V_{OUT} = \frac{R1 + R2}{R2}(-2.23)$.
2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.

79G EQUIVALENT CIRCUIT



μA79G, μA79GC

ELECTRICAL CHARACTERISTICS Unless otherwise specified, the following applies: $0°C \leq T_J \leq 125°C$ for 79GC and $-55°C \leq T_J \leq 150°C$ for 79G, $V_{IN} = -10$ V, $I_{OUT} = 500$ mA, Test Circuit 2 and Note 3.

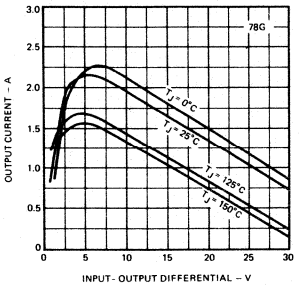
PARAMETER	CONDITION (Note 1)		MIN	TYP	MAX	UNITS
Input Voltage Range	$T_J = 25°C$		−40		−7.0	V
Nominal Output Voltage Range	$V_{IN} = V_{OUT} - 5$ V		−30		−2.23	V
Output Voltage Tolerance	$V_{OUT} - 15$ V $\leq V_{IN} \leq V_{OUT} - 3$ V, 5 mA $\leq I_{OUT} \leq$ 1.0 A, $P_D \leq$ 15 W, $V_{IN(MAX)} = -38$ V	$T_J = 25°C$			4.0	%(V_{OUT})
					5.0	%(V_{OUT})
Line Regulation	$T_J = 25°C$, $V_{OUT} \geq -10$ V, $(V_{OUT} - 20\text{ V}) \leq V_{IN} \leq (V_{OUT} - 2.5\text{ V})$				1.0	%(V_{OUT})
	$T_J = 25°C$, $V_{OUT} \leq -10$ V, $(V_{OUT} - 15\text{ V}) \leq V_{IN} \leq (V_{OUT} - 3\text{ V})$				0.75	%(V_{OUT})
	$(V_{OUT} - 7\text{ V}) \leq V_{IN} \leq (V_{OUT} - 3\text{ V})$				0.67	
Load Regulation	$T_J = 25°C$, $V_{IN} = V_{OUT} - 5$ V	250 mA $\leq I_{OUT} \leq$ 750 mA			1.0	%(V_{OUT})
		5 mA $\leq I_{OUT} \leq$ 1.5 A			2.0	%(V_{OUT})
Control Pin Current	$T_J = 25°C$			0.4	2.0	μA
					3.0	μA
Quiescent Current	$T_J = 25°C$			0.5	1.5	mA
					2.0	mA
Ripple Rejection	$-18\text{ V} \leq V_{IN} \leq -8$ V, $V_{OUT} = -5$ V, f = 120 Hz	μA79G	50	60		dB
		μA79GC	50	60		dB
Output Noise Voltage	$T_J = 25°C$, 10 Hz ≤ f ≤ 100 kHz, $V_{OUT} = -5$ V			125		μV
Dropout Voltage	Note 2	μA79G			2.8	V
		μA79GC			2.3	V
Short Circuit Current	$T_J = 25°C$, $V_{IN} = -30$ V			250		mA
Peak Output Current	$T_J = 25°C$			2.2		A
Average Temperature Coefficient of Output Voltage	$V_{OUT} = -5$ V, $I_{OUT} = 5$ mA			−0.4		mV/°C
Control Pin Voltage (Reference)	$T_J = 25°C$		−2.32	−2.23	−2.14	V
			−2.35		−2.11	V

Note 3.

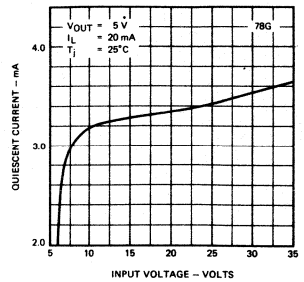
The convention for negative regulators is the algebraic value, thus −15 is less than −10 V.

TYPICAL PERFORMANCE CURVES FOR μA78G

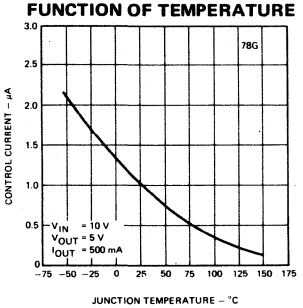
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



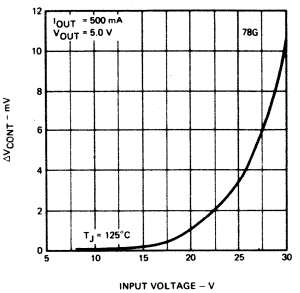
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



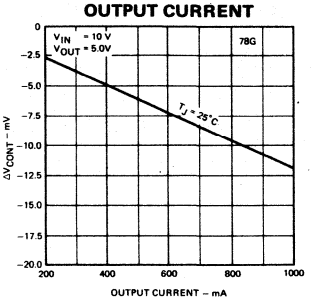
CONTROL CURRENT AS A FUNCTION OF TEMPERATURE



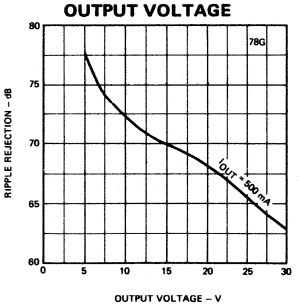
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



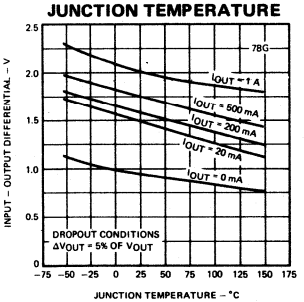
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



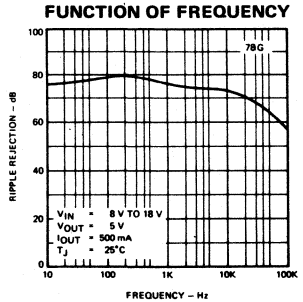
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



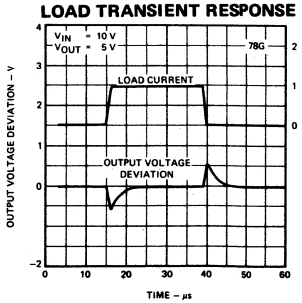
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



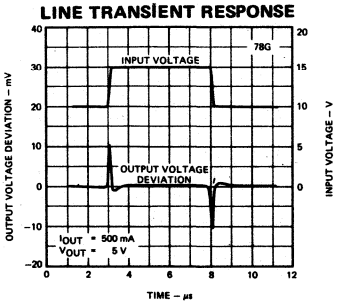
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



LOAD TRANSIENT RESPONSE



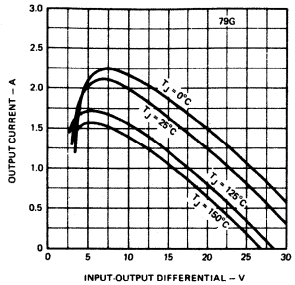
LINE TRANSIENT RESPONSE



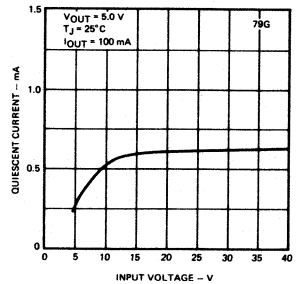
14

TYPICAL PERFORMANCE CURVES FOR μA79G

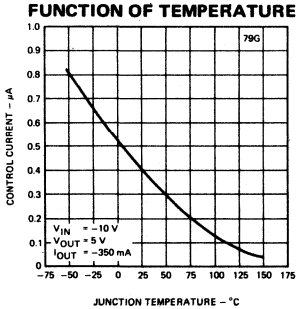
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



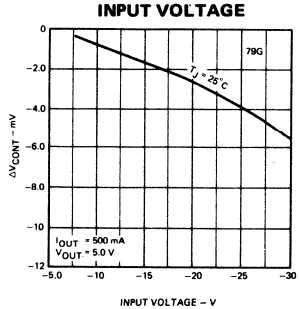
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



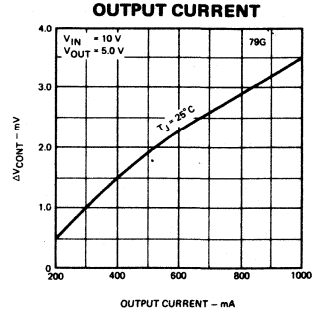
CONTROL CURRENT AS A FUNCTION OF TEMPERATURE



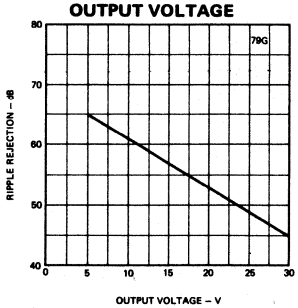
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



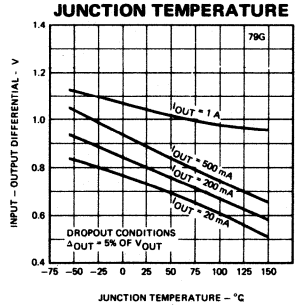
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



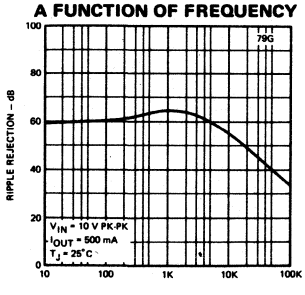
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



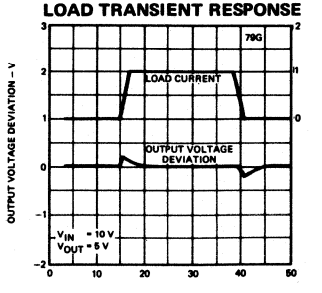
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



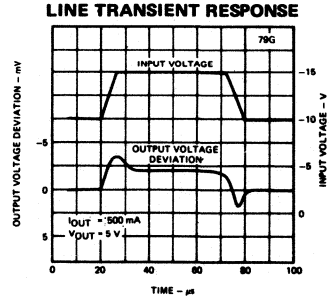
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



DESIGN CONSIDERATIONS – The 78G and 79G adjustable voltage regulators have an output voltage which varies from $V_{CONTROL}$ to typically $V_{IN} - 2$ V by $V_{OUT} = V_{CONTROL} \frac{(R1 + R2)}{R2}$. The nominal reference in the 78G is 5.0 V and 79G is –2.23 V. If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make R2 = 5 kΩ in the 78G. The output voltage is then: V_{OUT} = (R1 + R2) V, where R1 and R2 are in kΩs.

Example: If R2 = 5 kΩ and R1 = 10 kΩ then V_{OUT} = 15 V nominal, for the 78G;
R2 = 2.2 kΩ and R1 = 12.8 kΩ then V_{OUT} = –15.2 V nominal, for the 79G.

By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.

Both 78G and 79G regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	TYP θ_{JC}	MAX θ_{JC}	TYP θ_{JA}	MAX θ_{JA}
POWER TAB	7.5°C/W	11°C/W	75°C/W	80°C/W
TO-3	4.0°C/W	6°C/W	44°C/W	47°C/W

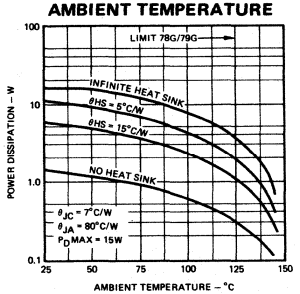
$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(MAX)} - T_A}{\theta_{JA}}, \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

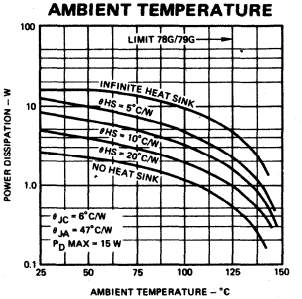
Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$\theta_{J\text{-}A}$ = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to Ambient thermal resistance
θ_{CS} = Case to heat sink resistance
θ_{SA} = Heat sink to ambient thermal resistance

μA78G AND μA79G POWER TAB (U1) PACKAGE WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

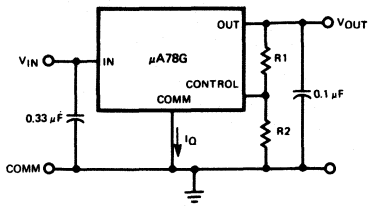


μA78G AND μA79G TO-3 PACKAGE WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



14

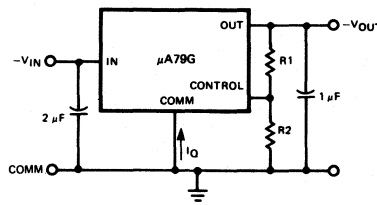
μA78G TEST CIRCUIT 1



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominal = 5 V

μA79G TEST CIRCUIT 2



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

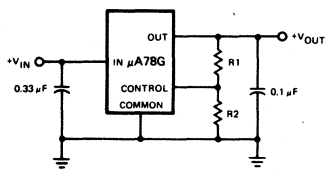
$V_{CONTROL}$ Nominal = −2.23 V

Recommended R2 current ≈ 1 mA
∴R2 = 5 kΩ (78G)
R2 = 2.2 kΩ (79G)

TYPICAL APPLICATIONS FOR μA78G

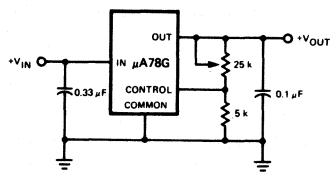
In many μA78G applications, compensation capacitors may not be required. However, for stable operation of the regulator over all input voltage and output current ranges, bypassing of the input and output (0.33 μF and 0.1 μF, respectively) is recommended. Input bypassing is necessary if the regulator is located far from the filter capacitor of the power supply. Bypassing the output will improve the transient response of the regulator.

BASIC POSITIVE REGULATOR

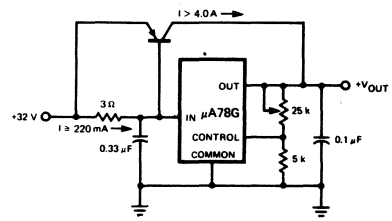


$$V_{OUT} = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

POSITIVE 5 TO 30 V ADJUSTABLE REGULATOR

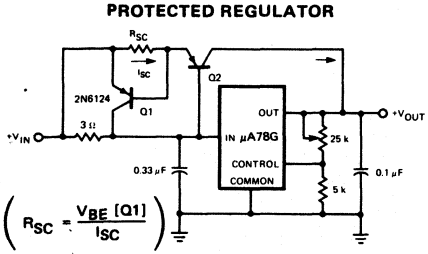


POSITIVE 5 TO 30 V ADJUSTABLE REGULATOR I_{OUT} > 5.0 A



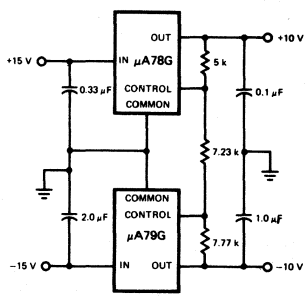
NOTE: External series pass device is not short circuit protected.

POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR



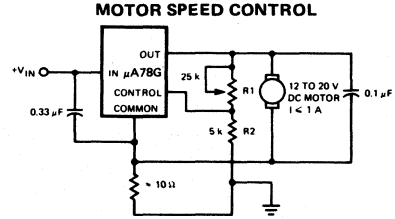
$$\left(R_{SC} = \frac{V_{BE\ [Q1]}}{I_{SC}}\right)$$

±10 V, 1.0 A DUAL TRACKING REGULATOR



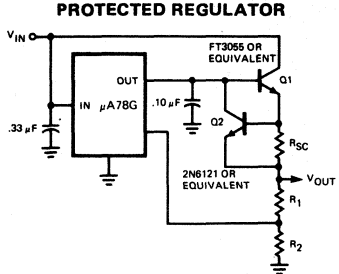
If load is not ground referenced, connect reverse biased diodes from outputs to ground.

MOTOR SPEED CONTROL

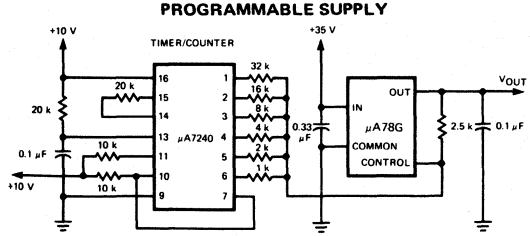


Use flyback diode across motor if necessary.

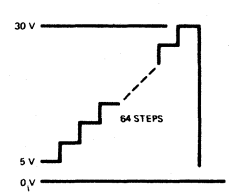
POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR



PROGRAMMABLE SUPPLY



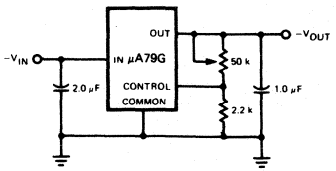
OUTPUT WAVEFORM



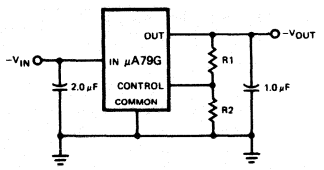
TYPICAL APPLICATIONS FOR μA79G

All μA78G applications apply to the μA79G under the following conditions; R2 values are 2.2 kΩ, all external transistors and diodes reverse polarity.

–30 V TO –2.2 V ADJUSTABLE REGULATOR

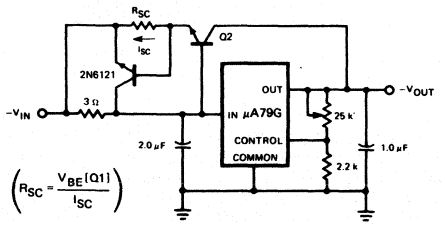


BASIC NEGATIVE REGULATOR



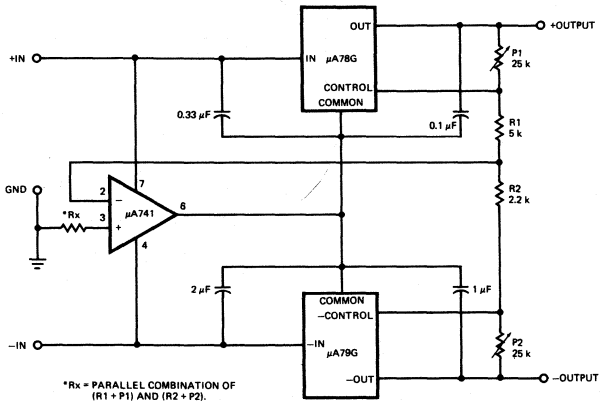
$$V_{OUT} = -V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

NEGATIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR



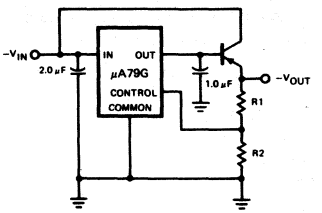
$$\left(R_{SC} = \frac{V_{BE(Q1)}}{I_{SC}}\right)$$

ADJUSTABLE DUAL TRACKING REGULATOR



*Rx = PARALLEL COMBINATION OF (R1 + P1) AND (R2 + P2).

NEGATIVE HIGH CURRENT VOLTAGE REGULATOR EXTERNAL SERIES PASS



NOTE:

Bypass capacitors are recommended for stable operation of the μA79G series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2 μF on the input, 1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

μA78MG • μA79MG

4-TERMINAL POSITIVE AND NEGATIVE ADJUSTABLE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA78MG and μA79MG are 4-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 500 mA with a maximum input voltage of 40 V for the positive regulator 78MG and –40 V for the negative regulator 79MG. Output current capability can be increased to greater than 10 A through use of one or more external transistors. The output voltage range of the 78MG positive voltage regulator is 5 V to 30 V and the output voltage range of the negative 79MG is –30 V to –2.2 V. For systems requiring both a positive and negative, the 78MG and 79MG are excellent for use as a dual tracking regulator. These 4-terminal voltage regulators are constructed using the Fairchild Planar* process.

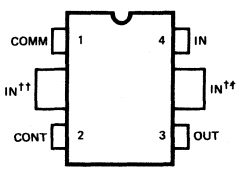
- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **μA78MG POSITIVE OUTPUT VOLTAGE 5 TO 30 V**
- **μA79MG NEGATIVE OUTPUT VOLTAGE –30 V TO –2.2 V**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT PROTECTION**
- **OUTPUT TRANSISTOR SAFE AREA PROTECTION**
- **POWER MINI DUAL IN-LINE PACKAGE**

ABSOLUTE MAXIMUM RATINGS

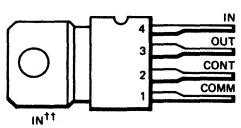
Input Voltage	
μA78MG, μA79MGC	40V
μA79MG, μA79MGC	–40V
Control Pin Voltage	
μA78MG, μA78MGC	$0 \leq V \leq V_{OUT}$
μA79MG, μA79MGC	$-V_{OUT} \leq -V \leq 0$
Power Dissipation	Internally Limited
Operating Junction Temperature Range (Note 1)	
Military (μA78MG, μA79MG)	–55°C to 150°C
Commercial (μA78MGC, μA79MGC)	0°C to 150°C
Storage Temperature Range	
4-Pin TO-39	–65°C to +150°C
Power Mini DIP and Power TAB	–55°C to +150°C
Lead Temperature	
Power TAB and Power Mini DIP (Soldering, 10 s)	230°C
4-Pin TO-39(Soldering, 60 s)	300°C

μA79MG CONNECTION DIAGRAMS (TOP VIEWS)

POWER MINI DIP
PACKAGE OUTLINE 9V
PACKAGE CODE T2



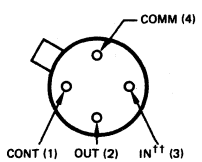
POWER TAB
PACKAGE OUTLINE 8Z
PACKAGE CODE U1



ORDER INFORMATION

TYPE	PART NO.
μA79MG	μA79MGU1C

4-LEAD TO-39
PACKAGE OUTLINE 5K
PACKAGE CODE H



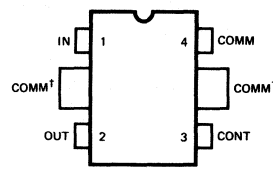
ORDER INFORMATION

TYPE	PART NO.
μA79MG	μA79MGHM
μA79MGC	μA79MGHC

††NOTE:
Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

μA78MG CONNECTION DIAGRAMS (TOP VIEWS)

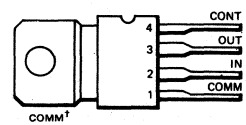
POWER MINI DIP
PACKAGE OUTLINE 9V
PACKAGE CODE T2



ORDER INFORMATION

TYPE	PART NO.
μA78MGC	μA78MGT2C

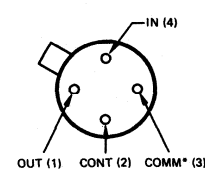
POWER TAB
PACKAGE OUTLINE 8Z
PACKAGE CODE U1



ORDER INFORMATION

TYPE	PART NO.
μA78MGC	μA78MGU1C

4-PIN TO-39
PACKAGE OUTLINE 5K
PACKAGE CODE H

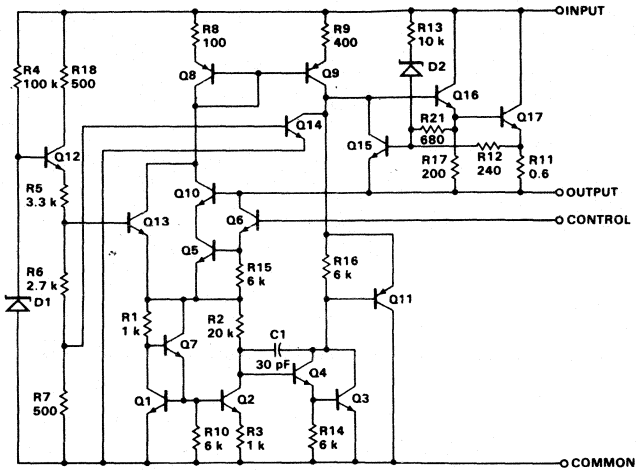


ORDER INFORMATION

TYPE	PART NO.
μA78MG	μA78MGHM
μA78MG	μA78MGHC

†NOTE:
Heat sink tabs connected to common through device substrate.

78MG EQUIVALENT CIRCUIT



Resistor values in Ω unless otherwise noted.

μA78MG (C, HC, HM)

ELECTRICAL CHARACTERISTICS Unless otherwise specified, the following specifications apply: $0°C \leq T_J \leq 125°C$ for μA78MGHC and μA78MGC, $-55°C \leq T_J \leq 150°C$ for μA78MGHM, V_{IN} = 10 V, I_{OUT} = 350 mA, Test Circuit 1.

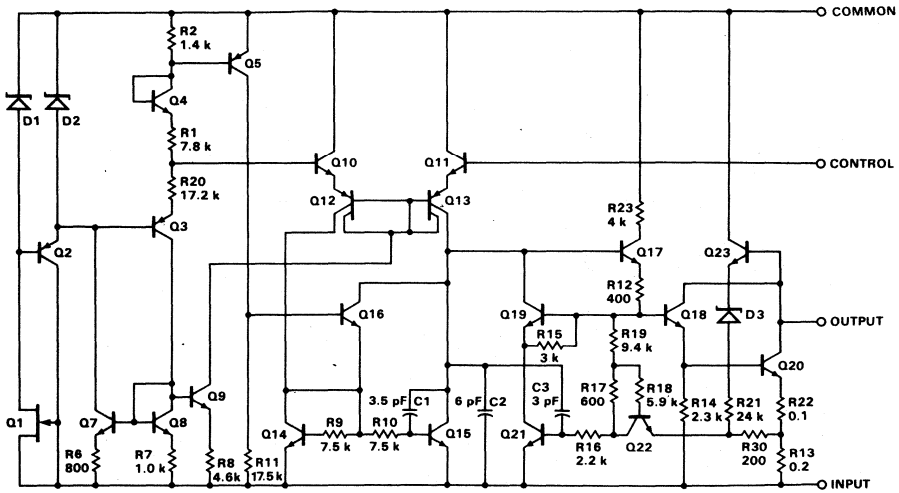
PARAMETER	CONDITION (Note 1)		MIN	TYP	MAX	UNITS
Input Voltage Range	$T_J = 25°C$		7.5		40	V V
Output Voltage Range	$V_{IN} = V_{OUT} + 5$ V		5.0		30	V
Output Voltage Tolerance	$V_{OUT} + 3$ V $\leq V_{IN} \leq V_{OUT} + 15$ V,	$T_J = 25°C$			4.0	%(V_{OUT})
	5 mA $\leq I_{OUT} \leq$ 350 mA $P_D \leq 5$ W, V_{INMAX} = 38 V				5.0	%(V_{OUT})
Line Regulation	$T_J = 25°C$, I_{OUT} = 200 mA, $V_{OUT} \leq 10$ V (V_{OUT} + 2.5 V) $\leq V_{IN} \leq$ (V_{OUT} + 20 V)				1.0	%(V_{OUT})
	$T_J = 25°C$, I_{OUT} = 200 mA, $V_{OUT} \geq 10$ V (V_{OUT} + 3 V) $\leq V_{IN} \leq$ (V_{OUT} + 15 V) (V_{OUT} + 3 V) $\leq V_{IN} \leq$ (V_{OUT} + 7 V)				0.75 0.67	%(V_{OUT}) %(V_{OUT})
Load Regulation	$T_J = 25°C$ 5 mA $\leq I_{OUT} \leq$ 500 mA, $V_{IN} = V_{OUT} + 7$ V				1.0	%(V_{OUT})
Control Pin Current	$T_J = 25°C$			1.0	5.0	μA
					8.0	μA
Quiescent Current	$T_J = 25°C$			2.8	4.0	mA
					5.0	mA
Ripple Rejection	8 V $\leq V_{IN} \leq$ 18 V	I_{OUT} = 300 mA, $T_J = 25°C$	62	80		dB
	V_{OUT} = 5 V, f = 120 Hz	I_{OUT} = 100 mA	62			dB
Output Noise Voltage	10 Hz $\leq$ f $\leq$ 100 kHz, V_{OUT} = 5 V			25		μV
Dropout Voltage	(Note 2)	μA78MGHM			3.0	V
		μA78MG(HC and C)			2.5	
Short Circuit Current	$V_{IN} = 35$ V, $T_J = 25°C$			300		mA
Peak Output Current	$T_J = 25°C$			800		mA
Average Temperature Coefficient of Output Voltage	V_{OUT} = 5 V I_{OUT} = 5 mA			−0.5		mV/°C
Control Pin Voltage (Reference)	$T_J = 25°C$		4.8	5.0	5.2	V
			4.75		5.25	V

NOTES:

1. V_{OUT} is defined for the 78MGC as $V_{OUT} = \frac{R1 + R2}{R2}$ (5.0); The 79MGC as $V_{OUT} = \frac{R1 + R2}{R2}$ (−2.23).

2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.

79MG EQUIVALENT CIRCUIT



Resistor values in Ω unless otherwise noted.

μA79MG (C, HC, HM)

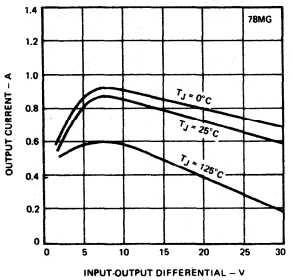
ELECTRICAL CHARACTERISTICS Unless otherwise specified, the following specifications apply: $0°C \leq T_J \leq 125°C$ for μA79MGHC and μA79MGC, $-55°C \leq T_J \leq 150°C$ for μA79MGHM, $V_{IN} = -10$ V, $I_{OUT} = 350$ mA, Test Circuit 2.

PARRMETER	CONDITION (Note 1)		MIN	TYP	MAX	UNITS
Input Voltage Range	$T_J = 25°C$		−40		−7.0	V
Output Voltage Range	$V_{IN} = V_{OUT} - 5$ V		−30		−2.23	V
Output Voltage Tolerance	$V_{OUT} - 15$ V ≤ $V_{IN} \leq V_{OUT} - 3$ V,	$T_J = 25°C$			4.0	%(V_{OUT})
	5 mA ≤ $I_{OUT} \leq$ 350 mA				5.0	%(V_{OUT})
	$P_D \leq$ 5 W, $V_{INMAX} = -38$ V					
Line Regulation	$T_J = 25°C$, I_{OUT} = 200 mA, $V_{OUT} \geq -10$ V					
	($V_{OUT} - 20$ V) ≤ $V_{IN} \leq$ ($V_{OUT} - 2.5$ V)				1.0	%(V_{OUT})
	$T_J = 25°C$, I_{OUT} = 200 mA, $V_{OUT} \leq -10$ V					
	($V_{OUT} - 15$ V(≤ $V_{IN} \leq$ ($V_{OUT} - 3$ V)				0.75	%(V_{OUT})
	($V_{OUT} - 7$ V) ≤ $V_{IN} \leq$($V_{OUT} - 3$ V)				0.67	%(V_{OUT})
Load Regulation	$V_{IN} = V_{OUT} - 7$ V, 5 mA ≤ $I_{OUT} \leq$ 500 mA				1.0	%(V_{OUT})
	$T_J = 25°C$					
Control Pin Current	$T_J = 25°C$				3.0	μA
					2.0	μA
Quiescent Current	$T_J = 25°C$			0.5	1.5	mA
					2.5	mA
Ripple Rejection	−18 V ≤ $V_{IN} \leq -8$ V	$T_J = 25°C$, I_{OUT} = 300 mA	54	65		dB
	$V_{OUT} = -5$ V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, $V_{OUT} = -5$ V			125		μV
Dropout Voltage	(Note 2)	μA79MGHM			2.5	V
		μA79MG (HC and C)			2.3	
Short Circuit Current	$V_{IN} = -35$ V			100		mA
Peak Output Current				650		mA
Average Temperature Coefficient of Output Voltage	$V_{OUT} = -5$ V I_{OUT} = 5 mA			−0.4		mV/°C
Control Pin Voltage (Reference)	$T_J = 25°C$		−2.32	−2.23	−2.14	V
			−2.35		−2.11	V

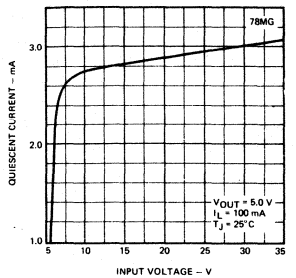
NOTE: The convention for Negative Regulators is the Algebraic value, thus −15 is less than −10 V.

TYPICAL PERFORMANCE CURVES FOR μA78MG

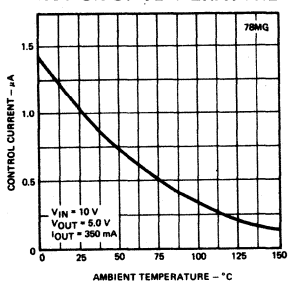
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



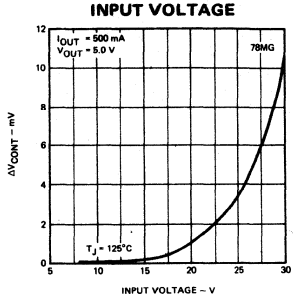
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



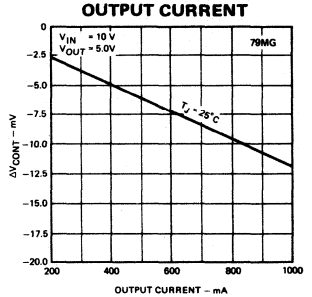
CONTROL CURRENT AS A FUNCTION OF TEMPERATURE



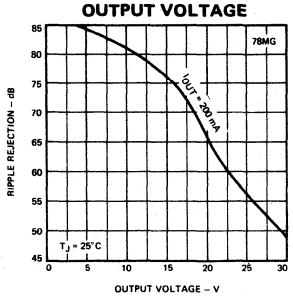
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



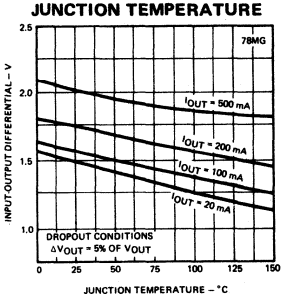
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



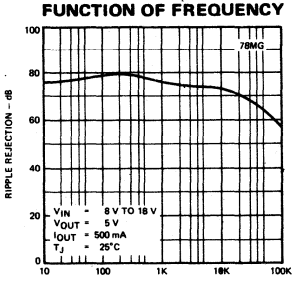
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



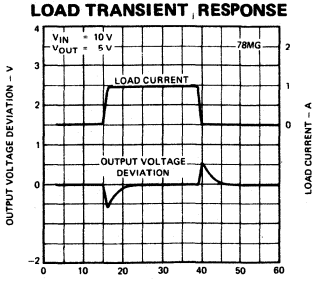
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



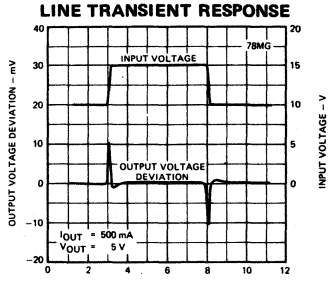
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



LOAD TRANSIENT RESPONSE



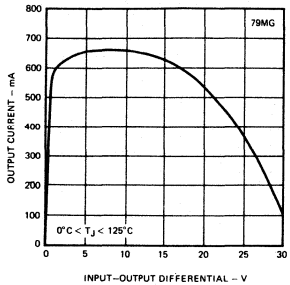
LINE TRANSIENT RESPONSE



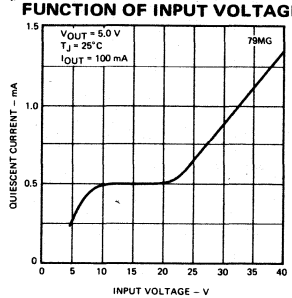
14

TYPICAL PERFORMANCE CURVES FOR μA79MG

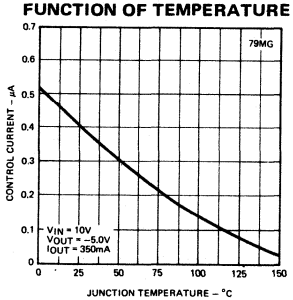
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



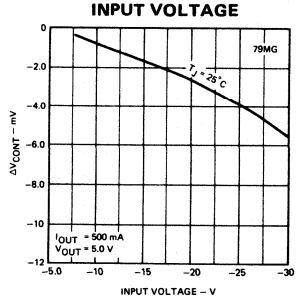
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



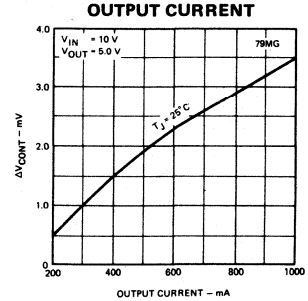
CONTROL CURRENT AS A FUNCTION OF TEMPERATURE



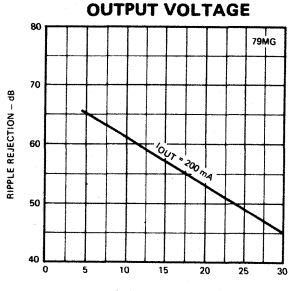
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



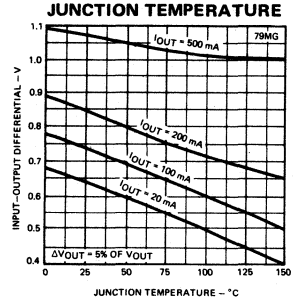
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



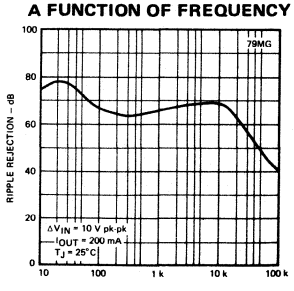
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



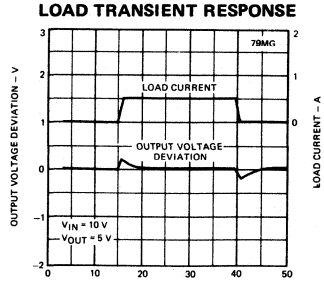
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



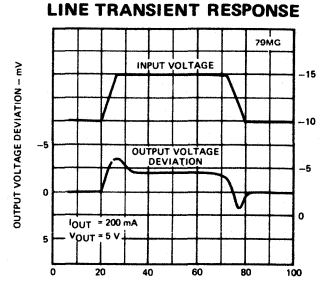
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



DESIGN CONSIDERATIONS – The 78MG and 79MG variable voltage regulators have an output voltage which varies from $V_{CONTROL}$ to typically $V_{IN} - 2$ V by $V_{OUT} = V_{CONTROL} \frac{(R1 + R2)}{R2}$. The nominal reference in the 78MG is 5.0 V and 79MG is −2.23 V. If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make R2 = 5 kΩ in the 78MG. The output voltage is then: V_{OUT} = (R1 + R2) Volts, where R1 and R2 are in kΩs.

Example: If R2 = 5 kΩ and R1 = 10 kΩ then V_{OUT} = 15 V nominal, for the 78MG;
R2 = 2.2 kΩ and R1 = 12.8 kΩ then V_{OUT} = −15.2 V nominal , for the 79MG.

By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.

Both 78MG and 79MG regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

PACKAGE	TYPICAL θ_{JC}	MAX θ_{JC}	TYPICAL θ_{JA}	MAX θ_{JA}
Power Mini DIP (T2)	7.5	11.0	75	80
Power TAB	8.0	12.0	75	80
TO-39	18.0	25.0	120	190

$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \quad \text{or} \quad \frac{T_{J\,(MAX)} - T_A}{\theta_{JA}} \quad \text{(Without a heat sink)}$$

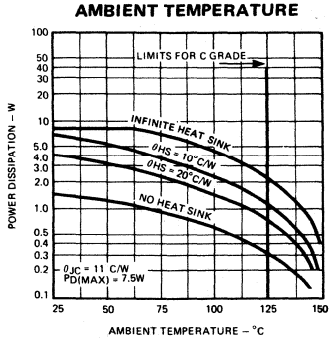
$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to ambient thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance
θ_{JA} = Junction to ambient thermal resistance

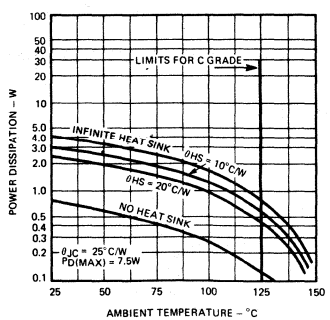
μA78MG AND μA79MG POWER MINI DIP (T2)

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



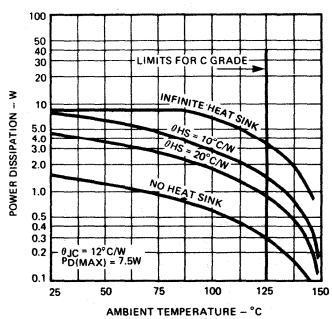
μA78MG AND μA79MG TO-39

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



μA78MG AND μA79MG POWER TAB (U1)

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

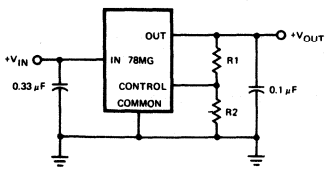


14

TYPICAL APPLICATIONS FOR μA78MG

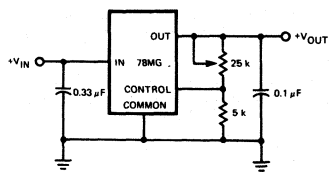
In many μA78MG applications, compensation capacitors may not be required. However, for stable operation of the regulator over all input voltage and output current ranges, bypassing of the input and output (0.33 μF and 0.1 μF, respectively) is recommended. Input bypassing is necessary if the regulator is located far from the filter capacitor of the power supply. Bypassing the output will improve the transient response of the regulator.

BASIC POSITIVE REGULATOR

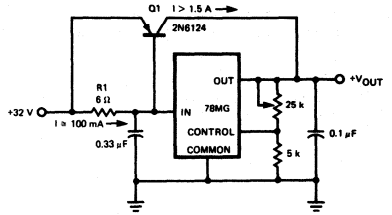


$$V_{OUT} = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

POSITIVE 5 TO 30 V ADJUSTABLE REGULATOR



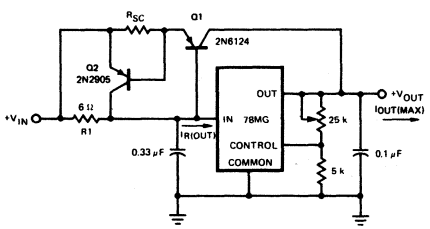
POSITIVE 5 TO 30 V ADJUSTABLE REGULATOR $I_{OUT} > 1.5$ A



$$R1 = \frac{\beta V_{BE(Q1)}}{V_{R(MAX)}\,(\beta+1) - I_{OUT(MAX)}}$$

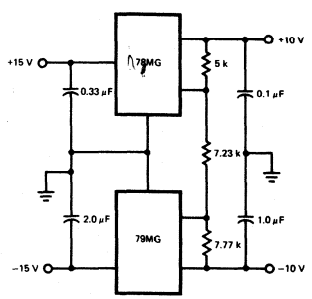
NOTE: External series pass device is not short circuit protected.

POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR



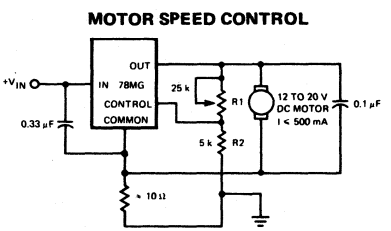
$$R1 = \frac{\beta V_{BE(Q1)}}{V_{R(MAX)}\,(\beta+1) - I_{OUT(MAX)}}$$

±10 V, 500 mA DUAL TRACKING REGULATOR



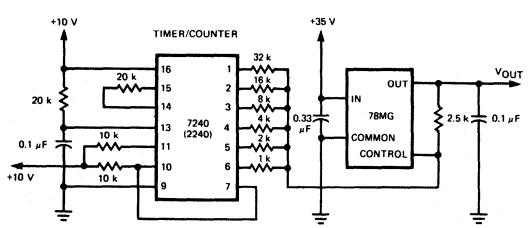
If load is not ground referenced, connect reverse biased diodes from outputs to ground.

MOTOR SPEED CONTROL

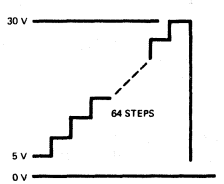


Use flyback diode across motor if necessary.

PROGRAMMABLE SUPPLY

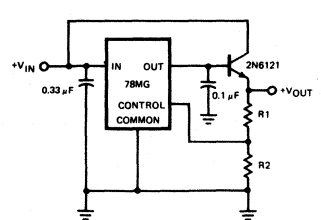


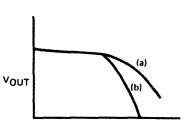
OUTPUT WAVEFORM



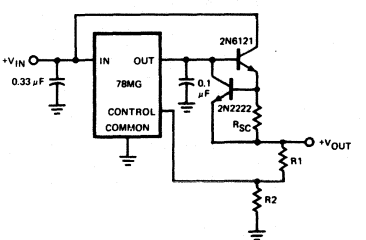
POSITIVE HIGH CURRENT VOLTAGE REGULATOR

EXTERNAL SERIES PASS (a)





SHORT CIRCUIT LIMIT (b)

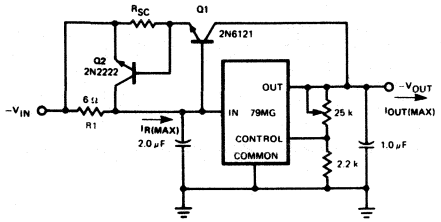


TYPICAL APPLICATIONS FOR 79MG

Bypass capacitors are recommended for stable operation of the μA79MG over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

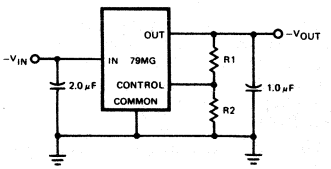
The bypass capacitors, (2 μF on the input, 1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

NEGATIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR



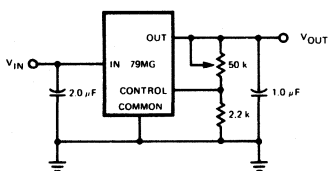
$$R1 = \frac{\beta V_{BE(Q1)}}{V_{R(MAX)}\,(\beta+1) - I_{OUT(MAX)}}$$

BASIC NEGATIVE REGULATOR

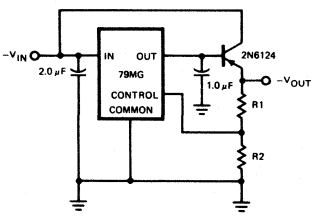


$$V_{OUT} = -V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

−30 V TO −2.2 V ADJUSTABLE REGULATOR

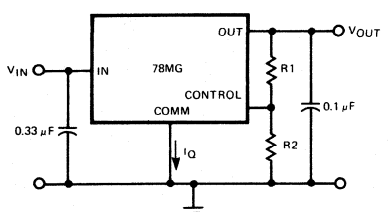


NEGATIVE HIGH CURRENT VOLTAGE REGULATOR EXTERNAL SERIES PASS



14

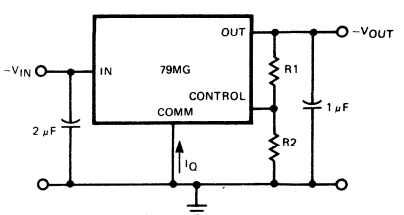
78MG TEST CIRCUIT 1



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominally = 5 V

79MG TEST CIRCUIT 2



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominally = −2.23 V

Recommended R2 current ≈ 1 mA
∴R2 = 5 kΩ(78MG)
R2 = 2.2 kΩ (79MG)

μA7800 SERIES
3-TERMINAL POSITIVE VOLTAGE REGULATORS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

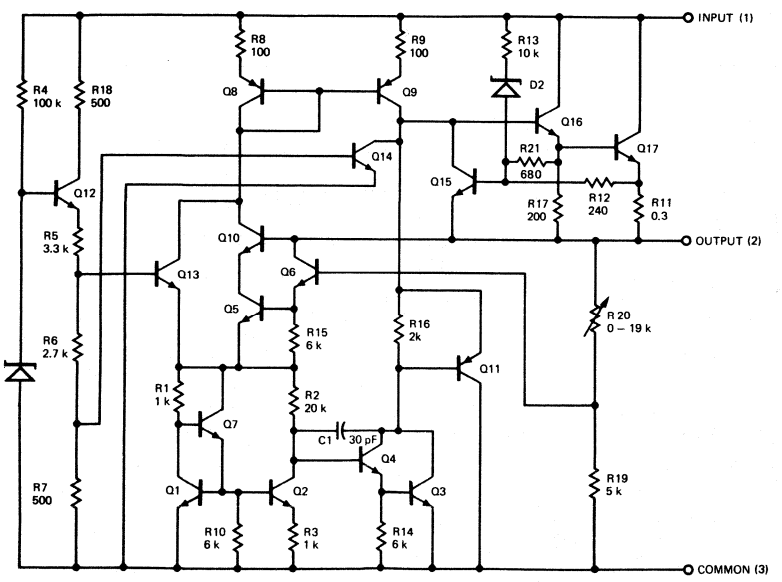
GENERAL DESCRIPTION – The μA7800 series of monolithic 3-Terminal Positive Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1 A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **OUTPUT CURRENT IN EXCESS OF 1 A**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE AREA COMPENSATION**
- **AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE**
- **OUTPUT VOLTAGES OF 5, 6, 8, 8.5, 12, 15, 18, AND 24 V**

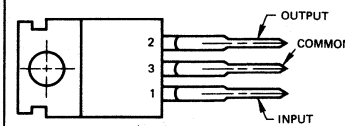
ABSOLUTE MAXIMUM RATINGS

Input Voltage (5 V through 18 V)		35 V
(24 V)		40 V
Internal Power Dissipation		Internally Limited
Storage Temperature Range		−65°C to +150°C
Operating Junction Temperature Range	μA7800	−55°C to +150°C
	μA7800C	0°C to +150°C
Lead Temperature (Soldering, 60 s time limit) TO-3 Package		300°C
(Soldering, 10 s time limit) TO-220 Package		230°C

EQUIVALENT CIRCUIT



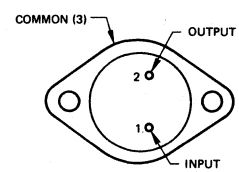
CONNECTION DIAGRAMS
TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA7805C	μA7805UC
6 V	μA7806C	μA7806UC
8 V	μA7808C	μA7808UC
8.5 V	μA7885C	μA7885UC
12 V	μA7812C	μA7812UC
15 V	μA7815C	μA7815UC
18 V	μA7818C	μA7818UC
24 V	μA7824C	μA7824UC

TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA7805	μA7805KM
6 V	μA7806	μA7806KM
8 V	μA7808	μA7808KM
8.5 V	μA7885	μA7885KM
12 V	μA7812	μA7812KM
15 V	μA7815	μA7815KM
18 V	μA7818	μA7818KM
24 V	μA7824	μA7824KM
5 V	μA7805C	μA7805KC
6 V	μA7806C	μA7806KC
8 V	μA7808C	μA7808KC
8.5 V	μA7885	μA7885KC
12 V	μA7812C	μA7812KC
15 V	μA7815C	μA7815KC
18 V	μA7818C	μA7818KC
24 V	μA7824C	μA7824KC

*Planar is a patented Fairchild process.

μA7805

ELECTRICAL CHARACTERISTICS

(V_{IN} = 10 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V		3	50	mV
			8 V ≤ V_{IN} ≤ 12 V		1	25	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	50	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	25	mV
Output Voltage		8.0 V ≤ V_{IN} ≤ 20 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.65		5.35	V
Quiescent Current		T_J = 25°C			4.2	6.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V		68	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			17		mΩ
Short Circuit Current		T_J = 25°C			750		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.1		mV/°C

μA7805C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V		3	100	mV
			8 V ≤ V_{IN} ≤ 25 V		1	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output Voltage		7 V ≤ V_{IN} ≤ 20 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.75		5.25	V
Quiescent Current		T_J = 25°C			4.2	8.0	mA
Quiescent Current Change	with line	7 V ≤ V_{IN} ≤ 25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V		62	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			17		mΩ
Short Circuit Current		T_J = 25°C			750		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.1		mV/°C

μA7806

ELECTRICAL CHARACTERISTICS
(V_{IN} = 11 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8 V ≤ V_{IN} ≤ 25 V		5	60	mV
			9 V ≤ V_{IN} ≤ 13 V		1.5	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		14	60	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	30	mV
Output Voltage		9 V ≤ V_{IN} ≤ 21 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		5.65		6.35	V
Quiescent Current		T_J = 25°C			4.3	6.0	mA
Quiescent Current Change	with line	9 V ≤ V_{IN} ≤ 25 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			45		μV
Ripple Rejection		f = 120 Hz, 9 V ≤ V_{IN} ≤ 19 V		65	75		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			19		mΩ
Short Circuit Current		T_J = 25°C			550		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−0.8		mV/°C

μA7806C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 11 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8 V ≤ V_{IN} ≤ 25 V		5	120	mV
			9 V ≤ V_{IN} ≤ 13 V		1.5	60	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		14	120	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	60	mV
Output Voltage		8 V ≤ V_{IN} ≤ 21 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		5.7		6.3	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			45		μV
Ripple Rejection		f = 120 Hz, 9 V ≤ V_{IN} ≤ 19 V		59	75		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			19		mΩ
Short Circuit Current		T_J = 25°C			550		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.8		mV/°C

μA7808

ELECTRICAL CHARACTERISTICS
(V_{IN} = 14 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	80	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	40	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	80	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	40	mV
Output Voltage		11.5 V ≤ V_{IN} ≤ 23 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.3	6.0	mA
Quiescent Current Change	with line	11.5 V ≤ V_{IN} ≤ 25 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			52		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		62	72		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			16		mΩ
Short Circuit Current		T_J = 25°C			450		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−0.8		mV/°C

μA7808C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 14 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	160	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	80	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	160	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	80	mV
Output Voltage		10.5 V ≤ V_{IN} ≤ 23 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	10.5 V ≤ V_{IN} ≤ 25 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz, ≤ f ≤ 100 kHz			52		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		56	72		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			16		mΩ
Short Circuit Current		T_J = 25°C			450		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.8		mV/°C

μA7885

ELECTRICAL CHARACTERISTICS
(V_{IN} = 15 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		8.15	8.5	8.85	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	85	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	40	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	85	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	40	mV
Output Voltage		12 V ≤ V_{IN} ≤ 23.5 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		8.1		8.9	V
Quiescent Current		T_J = 25°C			4.3	6.0	mA
Quiescent Current Change	with line	11.5 V ≤ V_{IN} ≤ 25 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			55		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		60	70		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			16		mΩ
Short Circuit Current		T_J = 25°C			450		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−0.8		mV/°C

μA7885C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 15 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		8.15	8.5	8.85	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	170	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	85	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	170	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	85	mV
Output Voltage		11 V ≤ V_{IN} ≤ 23.5 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		8.1		8.9	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	10.5 V ≤ V_{IN} ≤ 25 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz, ≤ f ≤ 100 kHz			55		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		54	70		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			16		mΩ
Short Circuit Current		T_J = 25°C			450		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.8		mV/°C

μA7812

ELECTRICAL CHARACTERISTICS
(V_{IN} = 19 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		11.5	12.0	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V		10	120	mV
			16 V ≤ V_{IN} ≤ 22 V		3.0	60	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	120	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	60	mV
Output Voltage		15.5 V ≤ V_{IN} ≤ 27 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.3	6.0	mA
Quiescent Current Change	with line	15 V ≤ V_{IN} ≤ 30 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V		61	71		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			18		mΩ
Short Circuit Current		T_J = 25°C			350		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.0		mV/°C

μA7812C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 19 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		11.5	12.0	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V		10	240	mV
			16 V ≤ V_{IN} ≤ 22 V		3.0	120	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	240	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	120	mV
Output Voltage		14.5 V ≤ V_{IN} ≤ 27 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	14.5 V ≤ V_{IN} ≤ 30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 ≤ V_{IN} ≤ 25 V		55	71		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			18		mΩ
Short Circuit Current		T_J = 25°C			350		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.0		mV/°C

14

μA7815

ELECTRICAL CHARACTERISTICS
(V_{IN} = 23 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		14.4	15.0	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V		11	150	mV
			20 V ≤ V_{IN} ≤ 26 V		3	75	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	150	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	75	mV
Output Voltage		18.5 V ≤ V_{IN} ≤ 30 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.4	6.0	mA
Quiescent Current Change	with line	18.5 V ≤ V_{IN} ≤ 30 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V		60	70		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			19		mΩ
Short Circuit Current		T_J = 25°C			230		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.0		mV/°C

μA7815C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 23 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		14.4	15.0	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V		11	300	mV
			20 V ≤ V_{IN} ≤ 26 V		3	150	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	300	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	150	mV
Output Voltage		17.5 V ≤ V_{IN} ≤ 30 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.4	8.0	mA
Quiescent Current Change	with line	17.5 V ≤ V_{IN} ≤ 30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V		54	70		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			19		mΩ
Short Circuit Current		T_J = 25°C			230		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.0		mV/°C

μA7818

ELECTRICAL CHARACTERISTICS
(V_{IN} = 27 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		17.3	18.0	18.7	V
Line Regulation		T_J = 25°C	21 V ≤ V_{IN} ≤ 33 V		15	180	mV
			24 V ≤ V_{IN} ≤ 30 V		5.0	90	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	180	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	90	mV
Output Voltage		22 V ≤ V_{IN} ≤ 33 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		17.1		18.9	V
Quiescent Current		T_J = 25°C			4.5	6.0	mA
Quiescent Current Change	with line	22 V ≤ V_{IN} ≤ 33 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			110		μV
Ripple Rejection		f = 120 Hz, 22 V ≤ V_{IN} ≤ 32 V		59	69		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			22		mΩ
Short Circuit Current		T_J = 25°C			200		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.0		mV/°C

μA7818C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 27 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		17.3	18.0	18.7	V
Line Regulation		T_J = 25°C	21 V ≤ V_{IN} ≤ 33 V		15	360	mV
			24 V ≤ V_{IN} ≤ 30 V		5.0	180	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	360	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	180	mV
Output Voltage		21 V ≤ V_{IN} ≤ 33 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		17.1		18.9	V
Quiescent Current		T_J = 25°C			4.5	8.0	mA
Quiescent Current Change	with line	21 V ≤ V_{IN} ≤ 33 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			110		μV
Ripple Rejection		f = 120 Hz, 22 ≤ V_{IN} ≤ 32 V		53	69		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			22		mΩ
Short Circuit Current		T_J = 25°C			200		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.0		mV/°C

μA7824

ELECTRICAL CHARACTERISTICS
(V_{IN} = 33 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		23.0	24.0	25.0	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V		18	240	mV
			30 V ≤ V_{IN} ≤ 36 V		6	120	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	240	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	120	mV
Output Voltage		28 V ≤ V_{IN} ≤ 38 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		22.8		25.2	V
Quiescent Current		T_J = 25°C			4.6	6.0	mA
Quiescent Current Change	with line	28 V ≤ V_{IN} ≤ 38 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170		μV
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V		56	66		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			28		mΩ
Short Circuit Current		T_J = 25°C			150		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.5		mV/°C

μA7824C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 33 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		23.0	24.0	25.0	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V		18	480	mV
			30 V ≤ V_{IN} ≤ 36 V		6	240	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	480	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	240	mV
Output Voltage		27 V ≤ V_{IN} ≤ 38 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		22.8		25.2	V
Quiescent Current		T_J = 25°C			4.6	8.0	mA
Quiescent Current Change	with line	27 V ≤ V_{IN} ≤ 38 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170		μV
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V		50	66		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			28		mΩ
Short Circuit Current		T_J = 25°C			150		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.5		mV/°C

DESIGN CONSIDERATIONS

The μA7800 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the regulator's maximum current, and output transistor safe area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 7800, 125°C for 7800C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
TO-3	3.5	5.5	40	45
TO-220	3.0	5.0	60	65

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \quad \text{or} \quad \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

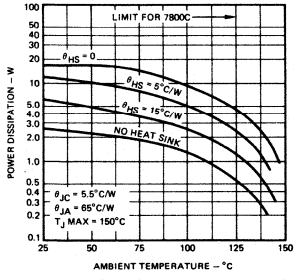
$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (without a heat sink)

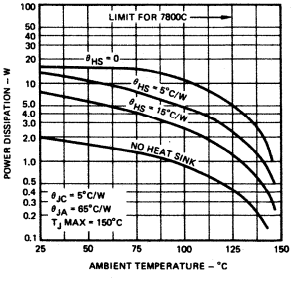
where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation

θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink to resistance
θ_{SA} = Heat sink to ambient thermal resistance
θ_{JA} = Junction to ambient thermal resistance

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE (TO-3)



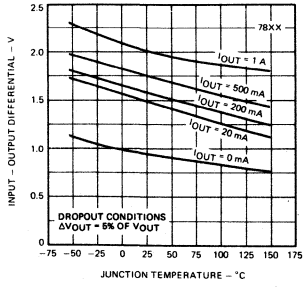
WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE (TO-220)



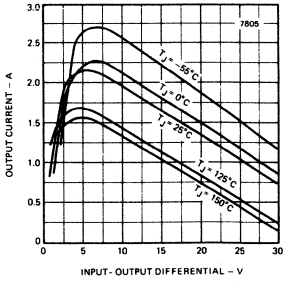
14

TYPICAL PERFORMANCE CURVES

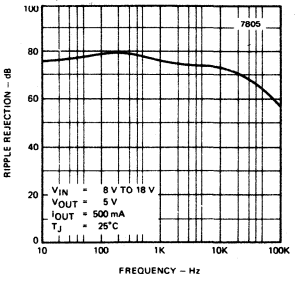
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE

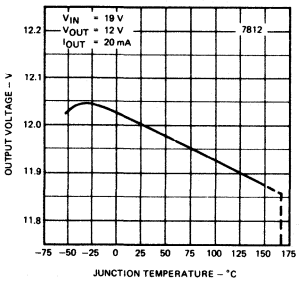


RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

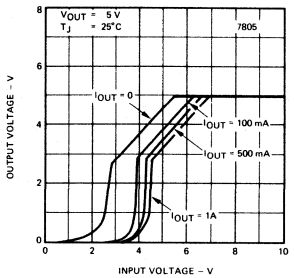


TYPICAL PERFORMANCE CURVES (Cont'd)

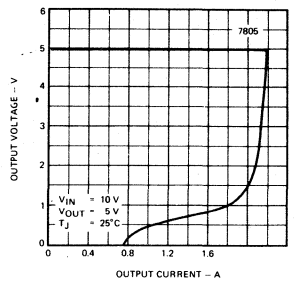
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



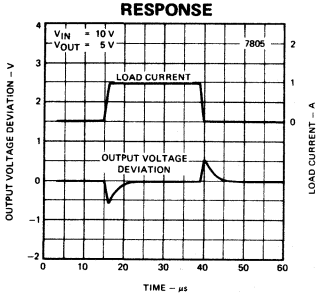
DROPOUT CHARACTERISTICS



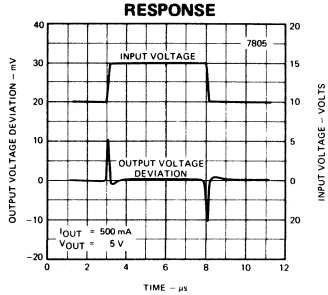
CURRENT LIMITING CHARACTERISTICS



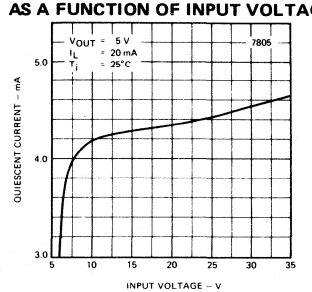
LOAD TRANSIENT RESPONSE



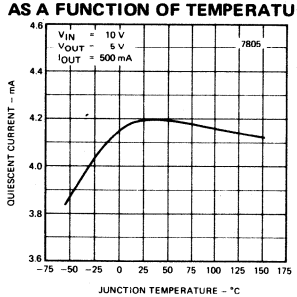
LINE TRANSIENT RESPONSE



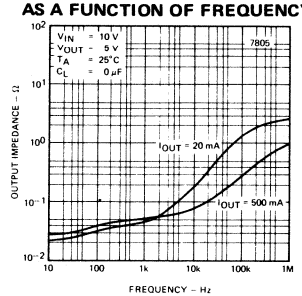
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

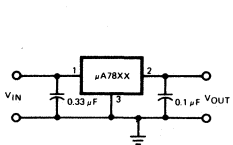


OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

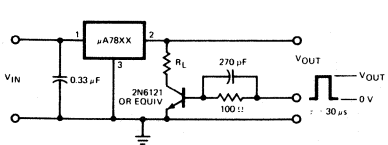


Note: The other μA7800 series devices have similar curves.

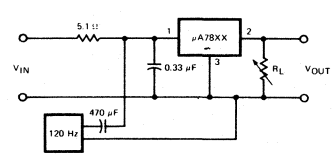
EQUIVALENT TEST CIRCUITS



DC PARAMETER TEST CIRCUIT

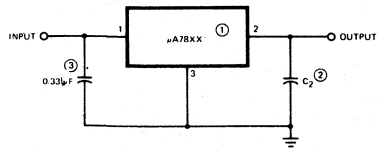


LOAD REGULATION TEST CIRCUIT



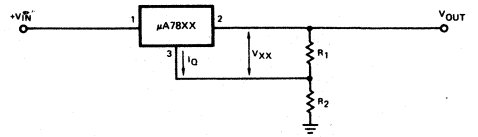
RIPPLE REJECTION TEST CIRCUIT

TYPICAL APPLICATIONS



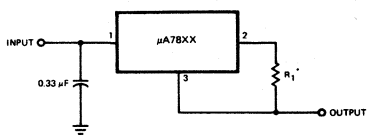
NOTES:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

FIXED OUTPUT REGULATOR



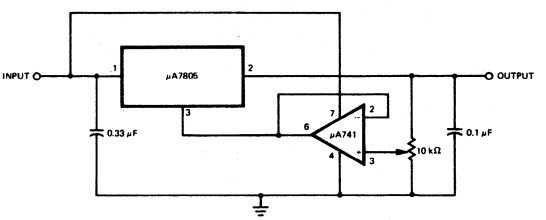
$$V_{OUT} = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_Q R_2$$

CIRCUIT FOR INCREASING OUTPUT VOLTAGE

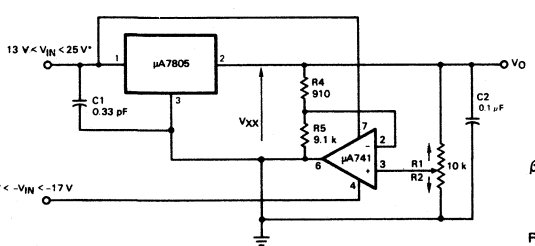


$$\text{Output Current} = \frac{V_{OUT}}{R_1}$$

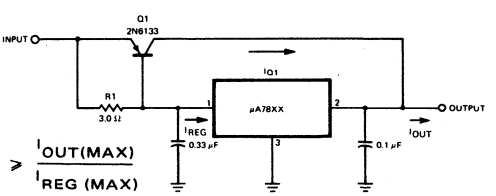
CURRENT REGULATOR



ADJUSTABLE OUTPUT REGULATOR, 7 to 30 VOLTS



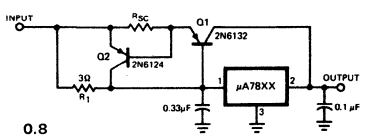
0.5 TO 10 V REGULATOR



$$\beta(Q1) \geq \frac{I_{OUT(MAX)}}{I_{REG\ (MAX)}}$$

$$R1 = \frac{0.9}{I_{REG}} = \frac{\beta(Q1)\, V_{BE(Q1)}}{I_{REG(MAX)}\,(\beta+1) - I_{OUT(MAX)}}$$

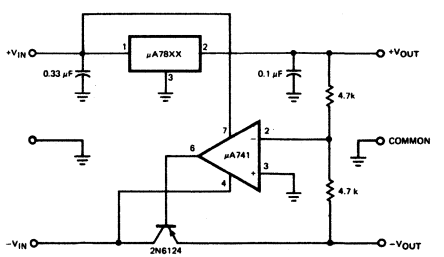
HIGH CURRENT VOLTAGE REGULATOR



$$R_{SC} = \frac{0.8}{I_{SC}}$$

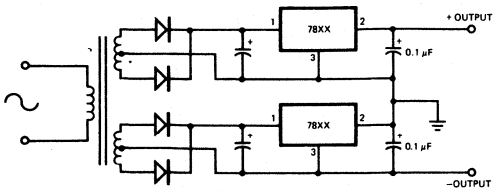
$$R1 = \frac{\beta V_{BE\ (Q1)}}{I_{REG(MAX)}\,(\beta+1) - I_{OUT(MAX)}}$$

HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED

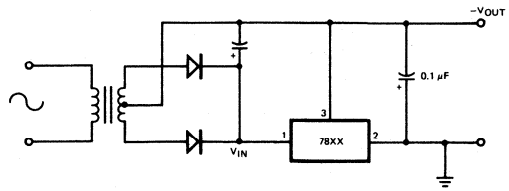


± TRACKING VOLTAGE REGULATOR

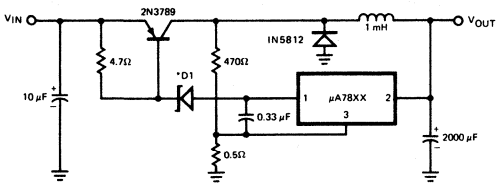
TYPICAL APPLICATIONS (Cont'd)



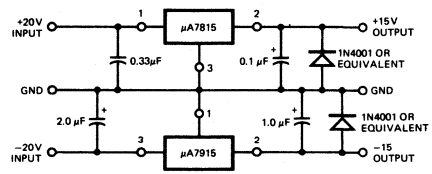
POSITIVE AND NEGATIVE REGULATOR



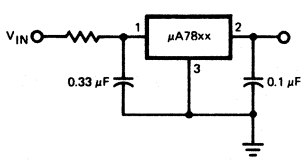
NEGATIVE OUTPUT VOLTAGE CIRCUIT

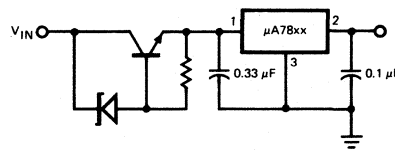


SWITCHING REGULATOR



DUAL SUPPLY
OPERATIONAL AMPLIFIER SUPPLY (±15 V @ 1.0 A)





HIGH INPUT VOLTAGE CIRCUITS

μA78L00 SERIES

3-TERMINAL POSITIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

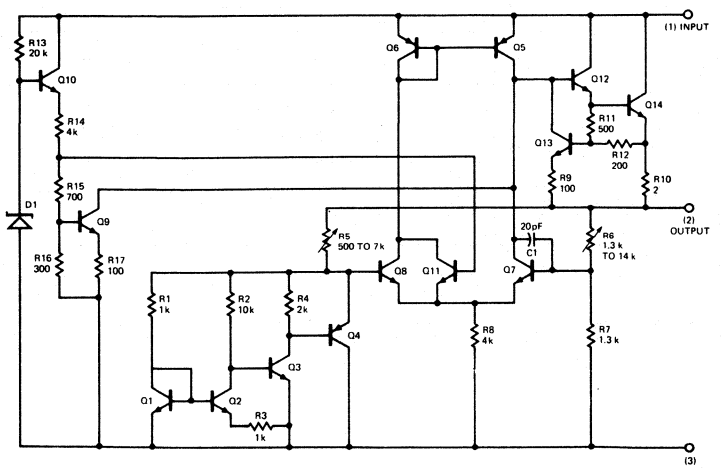
GENERAL DESCRIPTION – The μA78L00 series of 3-Terminal Positive Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on card regulation for elimination of noise and distribution problems associated with single point regulation. In addition, they can be used with power pass elements to make high current voltage regulators. The μA78L00 used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

- **OUTPUT CURRENT UP TO 100 mA**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **AVAILABLE IN JEDEC TO-92 AND LOW PROFILE TO-39 PACKAGES**
- **OUTPUT VOLTAGES OF 2.6 V, 5 V, 6.2 V, 8.2 V, 12 V, AND 15 V**
- **OUTPUT VOLTAGE TOLERANCES OF ±5% (78L00AC) AND ±10% (78L00C) OVER THE TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
2.6 V, 5 V, 6.2 V and 8.2 V	30 V
12 V and 15 V	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
Metal Can (TO-39 Type)	−65°C to +150°C
Molded TO-92	−55°C to +150°C
Operating Junction Temperature Ranges	
μA78L00C (Commercial)	0°C to +150°C
μA78L00V (Vehicular-Automotive)	−40°C to +125°C
Lead Temperatures	
Metal Can (Soldering, 60 s)	300°C
Molded TO-92 (Soldering, 10s)	260°C

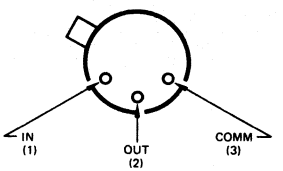
EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAMS

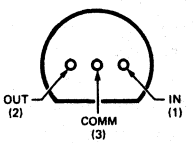
TO-39 TYPE METAL CAN
(TOP VIEW)
PACKAGE OUTLINE HC
PACKAGE CODE H



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA78L05AC	μA78L05AHC
12 V	μA78L12AC	μA78L12AHC
15 V	μA78L15AC	μA78L15AHC

JEDEC (TO-92) PACKAGE
(TOP VIEW)
PACKAGE OUTLINE EI
PACKAGE CODE W



ORDER INFORMATION†

OUTPUT VOLTAGE	TYPE	PART NO.
2.6 V	μA78L26AC	μA78L26AWC
5 V	μA78L05AC	μA78L05AWC
6.2 V	μA78L62AC	μA78L62AWC
8.2 V	μA78L82AC	μA78L82AWC
12 V	μA78L12AC	μA78L12AWC
15 V	μA78L15AC	μA78L15AWC
5 V	μA78L05AV	μA78L05AWV
6.2 V	μA78L62AV	μA78L62AWV
8.2 V	μA78L82AV	μA78L82AWV
12 V	μA78L12AV	μA78L12AWV

†Product previously specified as "HC" or "WC" has been deleted.

*Planar is a patented Fairchild process.

14

μA78L26AC

ELECTRICAL CHARACTERISTICS (Note 1)

V_{IN} = 9.0 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		2.5	2.6	2.7	V
Line Regulation		T_J = 25°C	4.75 V ≤ V_{IN} ≤ 20 V		40	100	mV
			5 V ≤ V_{IN} ≤ 20 V		30	75	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		10	50	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		4.0	25	mV
Output Voltage		4.75 V ≤ V_{IN} ≤ 20 V	1 mA ≤ I_{OUT} ≤ 40 mA	2.45		2.75	V
			1 mA ≤ I_{OUT} ≤ 70 mA	2.45		2.75	V
Quiescent Current		T_J = 25°C			3.6	6.0	mA
		T_J = 125°C				5.5	mA
Quiescent Current Change	with line	5 V ≤ V_{IN} ≤ 20 V				2.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			30		μV
Temp. Coef. of V_{OUT}		I_{OUT} = 5 mA			−0.4		mV/°C
Ripple Rejection		f = 120 Hz, 6 V ≤ V_{IN} ≤ 16 V, T_J = 25°C		43	51		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short Circuit Current		T_J = 25°C			140		mA

μA78L05AC and μA78L05AV

ELECTRICAL CHARACTERISTICS (Note 1)

V_{IN} = 10 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		4.6	5.0	5.4	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 20 V		55	200	mV
			8 V ≤ V_{IN} ≤ 20 V		45	150	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		11	60	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		5.0	30	mV
Output Voltage		7 V ≤ V_{IN} ≤ 20 V	1 mA ≤ I_{OUT} ≤ 40 mA	4.5		5.5	V
			1 mA ≤ I_{OUT} ≤ 70 mA	4.5		5.5	V
Quiescent Current		T_J = 25°C			3.8	6.0	mA
		T_J = 125°C				5.5	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 20 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.2	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Temp. Coef. of V_{OUT}		I_{OUT} = 5 mA			−0.65		mV/°C
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V, T_J = 25°C		40	49		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short Circuit Current		T_J = 25°C			140		mA

NOTE:

1. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

μA78L62AC and μA78L62AV

ELECTRICAL CHARACTERISTICS (Note 1)

V_{IN} = 12 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		5.95	6.2	6.45	V
Line Regulation		T_J = 25°C	8.5 V ≤ V_{IN} ≤ 20 V		65	175	mV
			9 V ≤ V_{IN} ≤ 20 V		55	125	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		13	80	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		6.0	40	mV
Output Voltage		8.5 V ≤ V_{IN} ≤ 20 V	1 mA ≤ I_{OUT} ≤ 40 mA	5.90		6.5	V
			1 mA ≤ I_{OUT} ≤ 70 mA	5.90		6.5	V
Quiescent Current		T_J = 25°C			3.9	6.0	mA
		T_J = 125°C				5.5	mA
Quiescent Current Change	with line	9.0 V ≤ V_{IN} ≤ 20 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			50		μV
Temp. Coef. of V_{OUT}		I_{OUT} = 5 mA			–0.75		mV/°C
Ripple Rejection		f = 120 Hz, 10 V ≤ V_{IN} ≤ 20 V, T_J = 25°C		40	46		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short Circuit Current		T_J = 25°C			140		mA

μA78L82AC and μA78L82AV

ELECTRICAL CHARACTERISTICS (Note 1)

V_{IN} = 14V , I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		7.87	8.2	8.53	V
Line Regulation		T_J = 25°C	11 V ≤ V_{IN} ≤ 23 V		80	175	mV
			12 V ≤ V_{IN} ≤ 23 V		70	125	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		15	80	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		8.0	40	mV
Output Voltage		11 V ≤ V_{IN} ≤ 23 V	1 mA ≤ I_{OUT} ≤ 40 mA	7.8		8.5	V
			1 mA ≤ I_{OUT} ≤ 70 mA	7.8		8.6	V
Quiescent Current		T_J = 25°C			3.9	6.0	mA
		T_J = 125°C				5.5	mA
Quiescent Current Change	with line	12 V ≤ V_{IN} ≤ 23 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			60		μV
Temp. Coef. of V_{OUT}		I_{OUT} = 5 mA			–0.8		mV/°C
Ripple Rejection		f = 120 Hz, 12 V ≤ V_{IN} ≤ 22 V, T_J = 25°C		39	45		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short Circuit Current		T_J = 25°C			140		mA

μA78L12AC and μA78L12AV

ELECTRICAL CHARACTERISTICS (Note 1)

V_{IN} = 19 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 27 V		120	250	mV
			16 V ≤ V_{IN} ≤ 27 V		100	200	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		20	100	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		10	50	mV
Output Voltage		14.5 V ≤ V_{IN} ≤ 27 V	1 mA ≤ I_{OUT} ≤ 40 mA	11.4		12.6	V
			1 mA ≤ I_{OUT} ≤ 70 mA	11.4		12.6	V
Quiescent Current		T_J = 25°C			4.2	6.5	mA
		T_J = 125°C				6.0	mA
Quiescent Current Change	with line	16 V ≤ V_{IN} ≤ 27 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			80		μV
Temp. Coef. of V_{OUT}		I_{OUT} = 5 mA			−1.0		mV/°C
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V, T_J = 25°C		37	42		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short Circuit Current		T_J = 25°C			140		mA

μA78L15AC

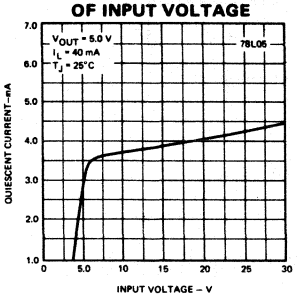
ELECTRICAL CHARACTERISTICS (Note 1)

V_{IN} = 23 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified

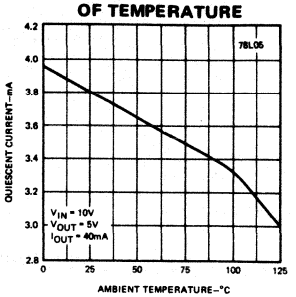
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		14.4	15	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V		130	300	mV
			20 V ≤ V_{IN} ≤ 30 V		110	250	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		25	150	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		12	75	mV
Output Voltage		17.5 V ≤ V_{IN} ≤ 30 V	1 mA ≤ I_{OUT} ≤ 40 mA	14.25		15.75	V
			1 mA ≤ I_{OUT} ≤ 70 mA	14.25		15.75	V
Quiescent Current		T_J = 25°C			4.4	6.5	mA
		T_J = 125°C				6.0	mA
Quiescent Current Change	with line	20 V ≤ V_{IN} ≤ 30 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Temp. Coef. of V_{OUT}		I_{OUT} = 5 mA			−1.3		mV/°C
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V, T_J = 25°C		34	39		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short Circuit Current		T_J = 25°C			140		mA

TYPICAL ELECTRICAL PERFORMANCE CURVES

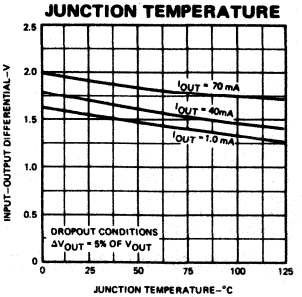
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



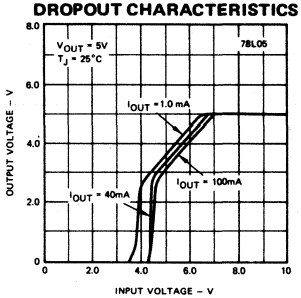
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



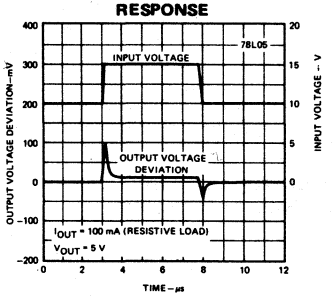
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



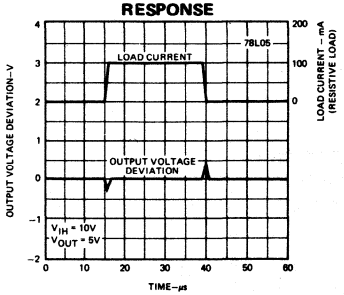
DROPOUT CHARACTERISTICS



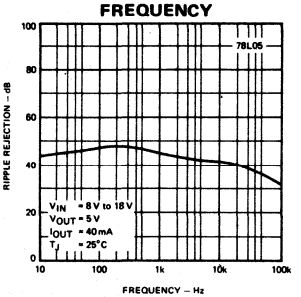
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



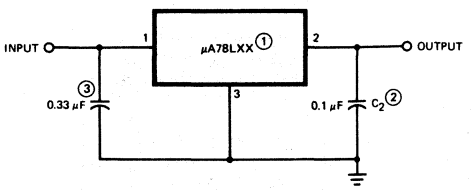
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



NOTE: Other μA78L00 Series Device have similar curves.

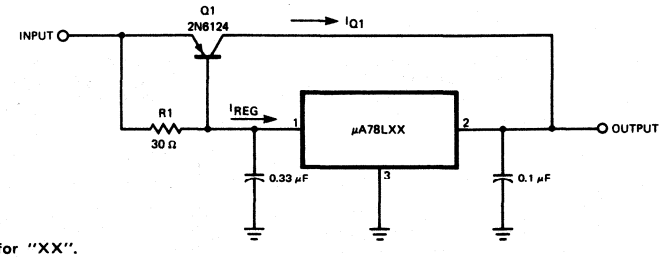
14

APPLICATIONS



NOTES:
① To specify an output voltage, substitute voltage value for "XX".
② Although no output capacitor is needed for stability, it does improve transient response.
③ Required if regulator is located an appreciable distance from power supply filter.

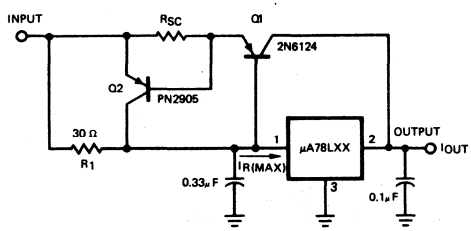
FIXED OUTPUT REGULATOR



For $I_{REG} \approx 23$ mA

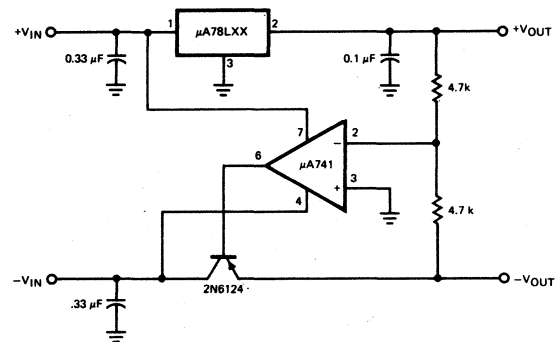
$$I_{REG} = \frac{0.7}{R1} \qquad I_{Q1} = \beta I_{REG}$$

HIGH CURRENT VOLTAGE REGULATOR

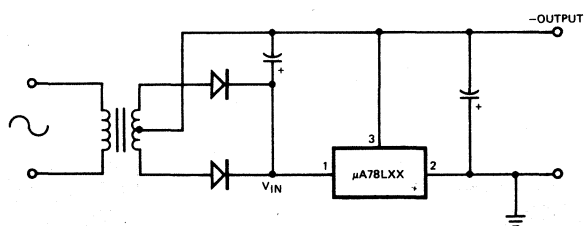


$$R_{SC} = \frac{0.7}{I_{SC}} \qquad R1 = \frac{\beta V_{BE(Q2)}}{V_{R(MAX)}(\beta+1) - I_{OUT(MAX)}}$$

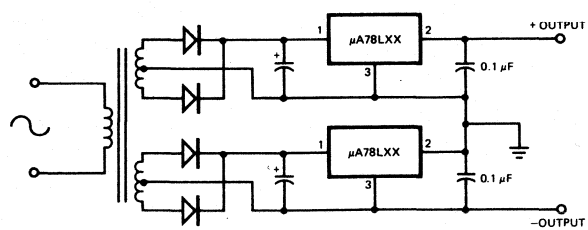
HIGH OUTPUT CURRENT, SHORT-CIRCUIT PROTECTED



± TRACKING VOLTAGE REGULATOR



NEGATIVE OUTPUT VOLTAGE CIRCUIT



POSITIVE AND NEGATIVE REGULATOR

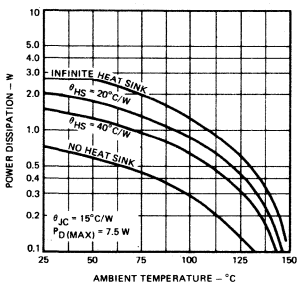
DESIGN CONSIDERATIONS

The μA78L series regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

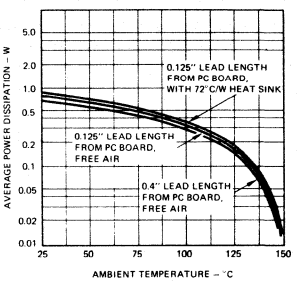
Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
TO-39	20	40	140	190
TO-92			180	190

TO-39 WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



TO-92 WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



THERMAL CONSIDERATIONS

The TO-92 molded package manufactured by Fairchild is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1 cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 and comparison of the thermal equivalent circuit of the TO-39 metal package with that of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

THE METAL CAN THERMAL MODEL

In the TO-39 case, where the die is attached directly to the base of a metal package, the thermal equivalent circuit is often represented simply as a series connection of the junction-to-case thermal resistance, θ_{JC}, and the case-to-ambient thermal resistance, θ_{CA}, as shown in Figure 1.

In this model, the current source represents the thermal energy source; T_J is the junction temperature, assuming a constant surface temperature across the die; θ_{JC} is the junction-to-case thermal resistance, measured at a point on the case directly beneath the die location; θ_{CA} is the thermal resistance from the case to the ultimate heat sink, ambient temperature, as represented by the battery. The heat flow is analogous to electrical current, and temperature to voltage. The total thermal resistance from junction to ambient is then:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

The maximum power dissipation is a function of the maximum permissible junction temperature (which is a function of the package materials and construction) and the total thermal resistance from the junction to ambient temperature. Junction temperature is assumed to be the limiting factor.

Thus: maximum power dissipation $P_D = \dfrac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$

Since $\theta_{JA} = \theta_{JC} + \theta_{CA}$

Then $\theta_{JA} = \dfrac{T_{J(MAX)} - T_A}{P_D}$

Or $\theta_{JA} P_D = T_J - T_A$

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

Therefore, using the V_{BE} method of junction temperature sensing, and attaching a thermocouple to the case at the location specified, the relative values of θ_{JC} and θ_{CA} can readily be determined.

The thermal ratings of the metal can package are normally presented with the case attached to an infinite heat sink at still air ambient temperature. This causes θ_{CA} to go to zero resulting in θ_{JC} representing the total θ_{JA}. The infinite heat sink is an unrealizable condition in the practical world, but serves to project a goal.

14

THE TO-92 PACKAGE

The TO-92 package thermal paths are considerably more complex than those of the TO-39 metal can package. In addition to the path through the molding compound to ambient temperature, there is another path through the leads, in parallel with the case path, to ambient temperature, as shown in Figure 2.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}} \quad (3)$$

Where: θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.

θ_{CA} = thermal resistance between the case and air at ambient temperature.

θ_{JL} = thermal resistance from transistor die through the collector lead to a point 1/16" below the regulator case.

θ_{LA} = total thermal resistance of the collector-base-emitter leads to ambient temperature.

θ_{JA} = junction to ambient thermal resistance.

As one can see from Figure 1, the metal can package generally does not have the lead cooling path because of the high thermal resistances resulting from the construction of the header, case and leads. Normally, this material is kovar. Now, θ_{JC} and θ_{JL} are within the package and not variable by the user. However, θ_{CA} and θ_{LA} are outside the package and can be effectively used to control the total thermal resistance and, therefore, junction temperature.

Replacing θ_{JA} of equation (1) with θ_{JA} of equation (3) gives:

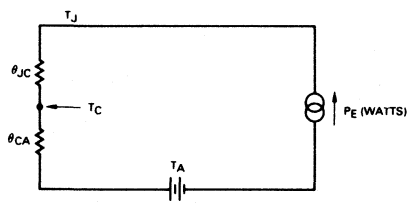
$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}} = \frac{T_J - T_A}{P_D} \quad (4)$$

The maximum T_J allowed in equation (4) is 150°C. The maximum power dissipation is determined by the net total thermal resistance θ_{JA}, the parallel equivalent networks of the case series path and lead series path, divided into the difference of the maximum junction temperature, 150°C, and ambient temperature generally specified as 25°C. In the case of the 78LXX, the maximum dissipation in a .4 inch condition is:

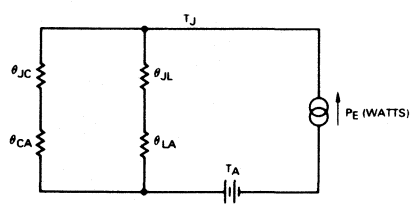
$$P_D = \frac{150-25}{\theta_{JA}}, \quad \theta_{JA} = 180°C/W$$

$$P_D = 0.7\ W$$

If lead length is reduced to .125 inch θ_{JA} becomes 160°C, and $P_{D(MAX)} = 0.78$ W.



THERMAL EQUIVALENT CIRCUIT TO-39 PACKAGE (DIE ATTACHED TO METAL PACKAGE BASE)
Fig. 1



TO-92 THERMAL EQUIVALENT CIRCUIT
Fig. 2

METHODS OF HEAT SINKING

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the θ_{CA} (Figure 2) and the new thermal resistance, θ'_{JA}, is:

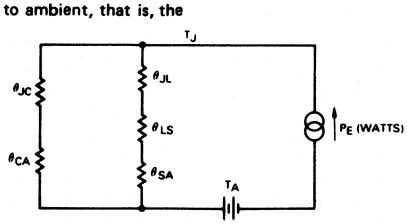
$$\theta'_{JA} = 145°C/W \quad \text{(assuming .125 inch lead length)}$$

The net change of 15°C/W increases the allowable power dissipation to 0.86 W with an inserted cost of 1-2 cents. A still further decrease in θ_{JA} could be achieved by using a sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the leads at the mounting point to ambient, that is, the mounting medium. θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in Figure 3.

In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but lead sinking would not be accomplished.

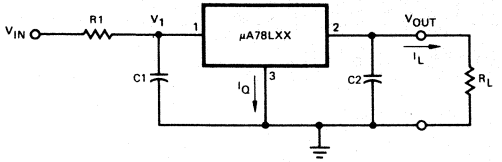
In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the leads. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.



TO-92 THERMAL EQUIVALENT CIRCUIT
(LEAD AT OTHER THAN AMBIENT TEMPERATURE)
Fig. 3

HIGH DISSIPATION APPLICATIONS



When it is necessary to operate a μA78L00 regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

R1 may be calculated from

$$R1 = \frac{V_{IN(MIN)} - V_{OUT} - 2.0\ V}{I_{L(MAX)} + I_Q}$$

where I_Q is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D(MAX)} = (V_1 - V_{OUT})\ I_{L(MAX)} + V_1\ I_Q$$

where

$$V_1 = V_{IN(MAX)} - (I_{L(MAX)} + I_Q)\ R1$$

The presence of R1 will affect load regulation according to the equation:

load regulation (at constant V_{IN}) = load regulation (at constant V_1) + (line regulation, mV per V) x (R1) x (ΔI_L).

As an example, consider a 15 V regulator with a supply voltage of 30 ±5 V, required to supply a maximum load current of 30 mA. I_Q is 4.3 mA, and minimum load current is to be 10 mA.

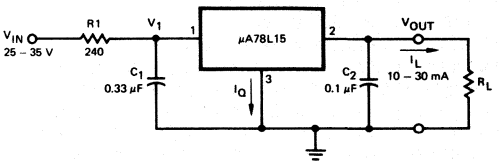
$$R1 = \frac{25 - 15 - 2}{30 + 4.3} = \frac{8}{34.3} \cong 240\ \Omega$$

$$V_1 = 35 - (30 + 4.3).24 = 35 - 8.2 = 26.8\ V$$

$$P_{D(MAX)} = (26.8 - 15)\ 30 + 26.8\ (4.3)$$

$$= 354 + 115$$

= 470 mW, which will permit operation up to 70°C in most applications.



Line regulation of this circuit is typically 110 mV for an input range of 25-35 V at a constant load current, i.e. 11 mV/V.

Load regulation = constant V_1 load regulation (typically 10 mV, 10-30 mA I_L)

+ (11 mV/V) x 0.24 x 20 mA (typically 53 mV)

= 63 mV for a load current change of 20 mA at a constant V_{IN} of 30 V.

14

μA78M00 SERIES

3-TERMINAL POSITIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

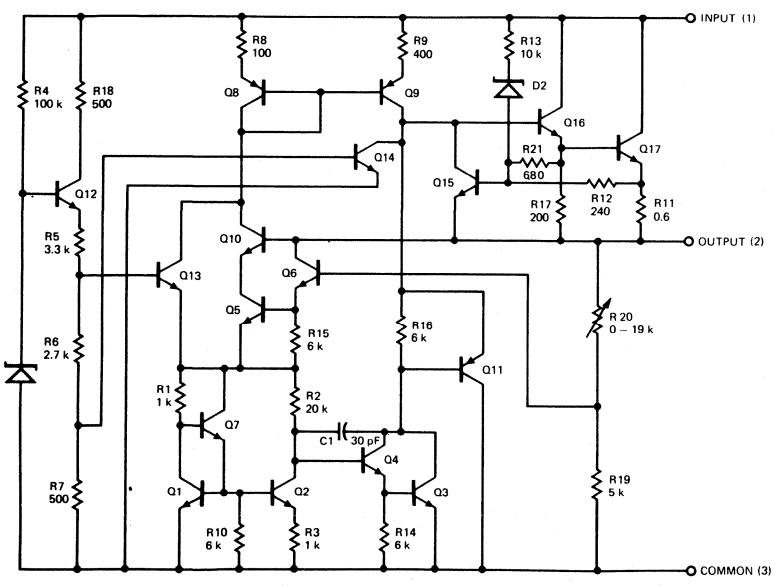
GENERAL DESCRIPTION – The μA78M00 series of 3-Terminal Medium Current Positive Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver in excess of 500 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE AREA COMPENSATION**
- **AVAILABLE IN JEDEC TO-220 AND TO-39 PACKAGES**
- **OUTPUT VOLTAGES OF 5 V, 6 V, 8 V, 12 V, 15 V, 20 V AND 24 V**
- **MILITARY AND COMMERCIAL TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS

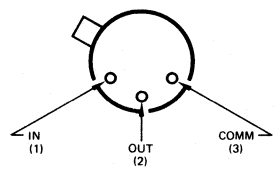
Input Voltage	
(5 V through 15 V)	35 V
(20 V, 24 V)	40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-39	−65°C to +150°C
TO-220	−55°C to +150°C
Operating Junction Temperature Range	
μA78M00	−55°C to +150°C
μA78M00C	0°C to +150°C
Lead Temperatures (Soldering, 60 s time limit) TO-39	300°C
(Soldering, 10 s time limit) TO-220	230°C

EQUIVALENT CIRCUIT



Notes on following pages.

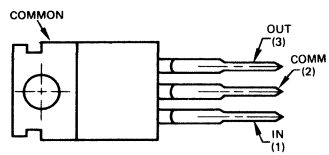
CONNECTION DIAGRAM
TO-39 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE BF
PACKAGE CODE H



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA78M05	μA78M05HM
6 V	μA78M06	μA78M06HM
8 V	μA78M08	μA78M08HM
12 V	μA78M12	μA78M12HM
15 V	μA78M15	μA78M15HM
20 V	μA78M20	μA78M20HM
24 V	μA78M24	μA78M24HM
5 V	μA78M05C	μA78M05HC
6 V	μA78M06C	μA78M06HC
8 V	μA78M08C	μA78M08HC
12 V	μA78M12C	μA78M12HC
15 V	μA78M15C	μA78M15HC
20 V	μA78M20C	μA78M20HC
24 V	μA78M24C	μA78M24HC

TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5 V	μA78M05C	μA78M05UC
6 V	μA78M06C	μA78M06UC
8 V	μA78M08C	μA78M08UC
12 V	μA78M12C	μA78M12UC
15 V	μA78M15C	μA78M15UC
20 V	μA78M20C	μA78M20UC
24 V	μA78M24C	μA78M24UC

*Planar is a patented Fairchild process.

μA78M05

ELECTRICAL CHARACTERISTICS
(V_{IN} = 10 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		3.0	50	mV
			8 V ≤ V_{IN} ≤ 20 V, I_{OUT} = 200 mA		1.0	25	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	50	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	25	mV
Output Voltage		8 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 350 mA		4.7		5.3	V
Quiescent Current		T_J = 25°C			4.5	6.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	I_{OUT} = 100 mA	62			dB
			I_{OUT} = 300 mA, T_J = 25°C	62	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			300		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA78M05C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 10 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		3.0	100	mV
			8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		1.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	100	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	50	mV
Output Voltage		7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 350 mA		4.75		5.25	V
Quiescent Current		T_J = 25°C			4.5	6.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	I_{OUT} = 100 mA	62			dB
			I_{OUT} = 300 mA, T_J = 25°C	62	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			300		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

14

μA78M06

ELECTRICAL CHARACTERISTICS
(V_{IN} = 11 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		5.0	60	mV
			9 V ≤ V_{IN} ≤ 20 V, I_{OUT} = 200 mA		1.5	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	60	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	30	mV
Output Voltage		9 V ≤ V_{IN} ≤ 21 V, 5 mA ≤ I_{OUT} ≤ 350 mA		5.7		6.3	V
Quiescent Current		T_J = 25°C			4.5	6.0	mA
Quiescent Current Change	with line	9 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			45		μV
Ripple Rejection		f = 120 Hz, 9 V ≤ V_{IN} ≤ 19 V	I_{OUT} = 100 mA	59			dB
			I_{OUT} = 300 mA, T_J = 25°C	59	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			270		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.5		mV/°C

μA78M06C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 11 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		5.0	100	mV
			9 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		1.5	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	120	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	60	mV
Output Voltage		8 V ≤ V_{IN} ≤ 21 V, 5 mA ≤ I_{OUT} ≤ 350 mA		5.7		6.3	V
Quiescent Current		T_J = 25°C			4.5	6.0	mA
Quiescent Current Change	with line	9 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			45		μV
Ripple Rejection		f = 120 Hz, 9 V ≤ V_{IN} ≤ 19 V	I_{OUT} = 100 mA	59			dB
			I_{OUT} = 300 mA, T_J = 25°C	59	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			270		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.5		mV/°C

μA78M08

ELECTRICAL CHARACTERISTICS
(V_{IN} = 14 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		6.0	60	mV
			11 V ≤ V_{IN} ≤ 20 V, I_{OUT} = 200 mA		2.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	80	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	40	mV
Output Voltage		11.5 V ≤ V_{IN} ≤ 23 V, 5 mA ≤ I_{OUT} ≤ 350 mA		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.6	6.0	mA
Quiescent Current Change	with line	11.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			52		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V	I_{OUT} = 100 mA	56			dB
			I_{OUT} = 300 mA, T_J = 25°C	56	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			250		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.5		mV/°C

μA78M08C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 14 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		6.0	100	mV
			11 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		2.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	160	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	80	mV
Output Voltage		10.5 V ≤ V_{IN} ≤ 23 V, 5 mA ≤ I_{OUT} ≤ 350 mA		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.6	6.0	mA
Quiescent Current Change	with line	10.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			52		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V	I_{OUT} = 100 mA	56			dB
			I_{OUT} = 300 mA, T_J = 25°C	56	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			250		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.5		mV/°C

14

μA78M12

ELECTRICAL CHARACTERISTICS
(V_{IN} = 19 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		8.0	60	mV
			16 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		2.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	120	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	60	mV
Output Voltage		15.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 350 mA		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.8	6.0	mA
Quiescent Current Change	with line	15 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V	I_{OUT} = 100 mA	55			dB
			I_{OUT} = 300 mA, T_J = 25°C	55	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA78M12C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 19 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		8.0	100	mV
			16 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		2.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	240	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	120	mV
Output Voltage		14.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 350 mA		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.8	6.0	mA
Quiescent Current Change	with line	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V	I_{OUT} = 100 mA	55			dB
			I_{OUT} = 300 mA, T_J = 25°C	55	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA78M15

ELECTRICAL CHARACTERISTICS
(V_{IN} = 23 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		14.4	15	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		10	60	mV
			20 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		3.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	150	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	75	mV
Output Voltage		18.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_{OUT} ≤ 350 mA		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.8	6.0	mA
Quiescent Current Change	with line	18.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V	I_{OUT} = 100 mA	54			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	70		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA78M15C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 23 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		14.4	15	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		10	100	mV
			20 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		3.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	300	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	150	mV
Output Voltage		17.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_{OUT} ≤ 350 mA		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.8	6.0	mA
Quiescent Current Change	with line	17.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V	I_{OUT} = 100 mA	54			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	70		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA78M20

ELECTRICAL CHARACTERISTICS
(V_{IN} = 29 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		19.2	20	20.8	V
Line Regulation		T_J = 25°C	23 V ≤ V_{IN} ≤ 35 V, I_{OUT} = 200 mA		10	60	mV
			24 V ≤ V_{IN} ≤ 35 V, I_{OUT} = 200 mA		5.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		30	200	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	100	mV
Output Voltage		24 V ≤ V_{IN} ≤ 35 V, 5 mA ≤ I_{OUT} ≤ 350 mA		19		21	V
Quiescent Current		T_J = 25°C			4.9	6.0	mA
Quiescent Current Change	with line	24 V ≤ V_{IN} ≤ 35 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			110		μV
Ripple Rejection		f = 120 Hz. 24 V ≤ V_{IN} ≤ 34 V	I_{OUT} = 100 mA	53			dB
			I_{OUT} = 300 mA, T_J = 25°C	53	70		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.1		mV/°C

μA78M20C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 29 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		19.2	20	20.8	V
Line Regulation		T_J = 25°C	23 V ≤ V_{IN} ≤ 35 V, I_{OUT} = 200 mA		10	100	mV
			24 V ≤ V_{IN} ≤ 35 V, I_{OUT} = 200 mA		5.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		30	400	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	200	mV
Output Voltage		23 V ≤ V_{IN} ≤ 35 V, 5 mA ≤ I_{OUT} ≤ 350 mA		19		21	V
Quiescent Current		T_J = 25°C			4.9	6.0	mA
Quiescent Current Change	with line	23 V ≤ V_{IN} ≤ 35 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			110		μV
Ripple Rejection		f = 120 Hz. 24 V ≤ V_{IN} ≤ 34 V	I_{OUT} = 100 mA	53			dB
			I_{OUT} = 300 mA T_J = 25°C	53	70		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.1		mV/°C

μA78M24

ELECTRICAL CHARACTERISTICS
(V_{IN} = 33 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		23	24	25	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA		10	60	mV
			30 V ≤ V_{IN} ≤ 36 V, I_{OUT} = 200 mA		5.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		30	240	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	120	mV
Output Voltage		28 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_{OUT} ≤ 350 mA		22.8		25.2	V
Quiescent Current		T_J = 25°C			5.0	6.0	mA
Quiescent Current Change	with line	28 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170		μV
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	50	70		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.2		mV/°C

μA78M24C

ELECTRICAL CHARACTERISTICS
(V_{IN} = 33 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		23	24	25	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA		10	100	mV
			28 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA		5.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		30	480	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	240	mV
Output Voltage		27 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_{OUT} ≤ 350 mA		22.8		25.2	V
Quiescent Current		T_J = 25°C			5.0	6.0	mA
Quiescent Current Change	with line	27 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170		μV
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	50	70		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.2		mV/°C

DESIGN CONSIDERATIONS

The μA78M00 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe area compensation for reducing the output short circuit current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 78M00, 125°C for 78M00C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	TYP θ_{JC}	MAX θ_{JC}	TYP θ_{JA}	MAX θ_{JA}
TO-39	18	25	120	185
TO-220	3	5	62	70

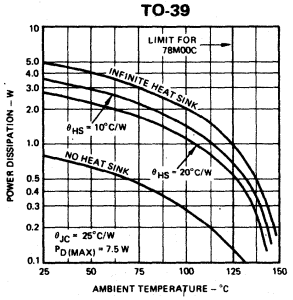
$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(MAX)} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

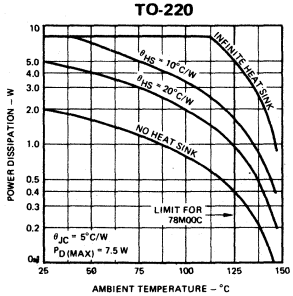
Solving for T_J: $T_J = T_A + P_D(\theta_{JC}+\theta_{CA})$ or $T_A + P_D\,\theta\,JA$ (Without a heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to Ambient thermal resistance
θ_{CS} = Case to heat sink to resistance
θ_{SA} = Heat sink to ambient thermal resistance
θ_{JA} = Junction to Ambient thermal resistance

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE TO-39

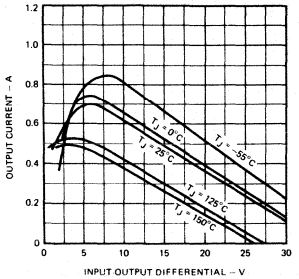


WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE TO-220

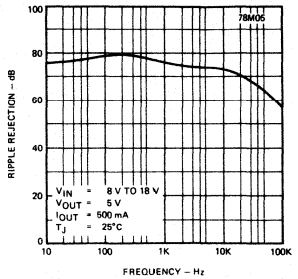


ELECTRICAL PERFORMANCE CURVES

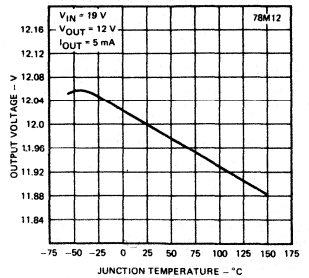
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



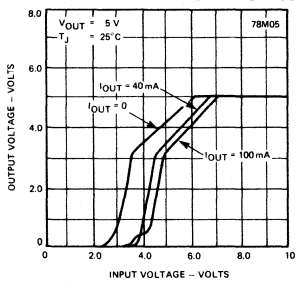
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



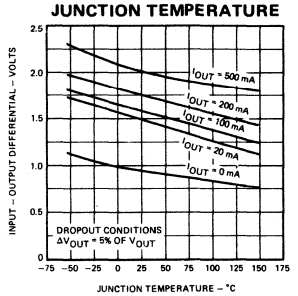
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



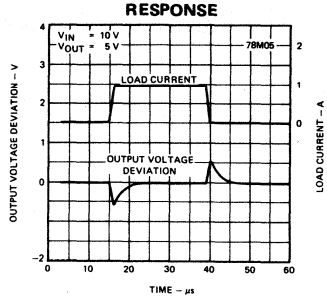
DROPOUT CHARACTERISTICS



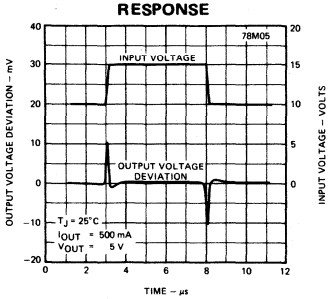
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



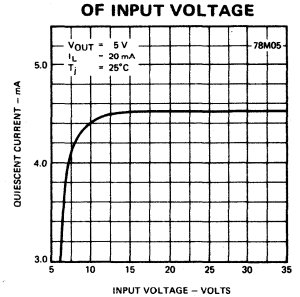
LOAD TRANSIENT RESPONSE



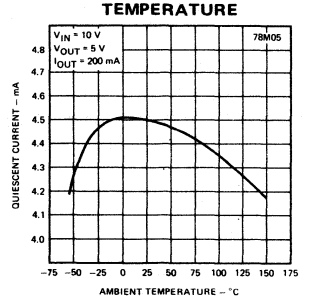
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

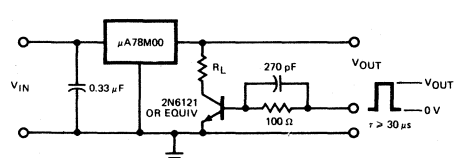


QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

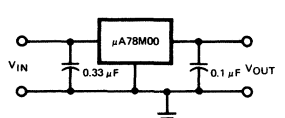


NOTE: Other μA78M00 Series devices have similar curves.

TEST CIRCUITS

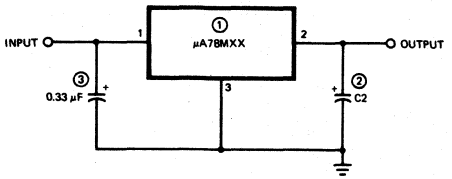


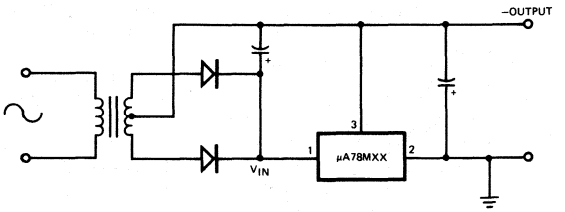
LOAD REGULATION TEST CIRCUIT



DC PARAMETER TEST CIRCUIT

APPLICATIONS

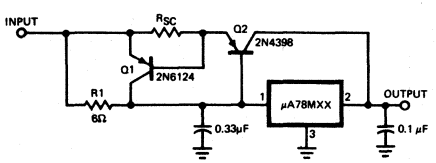


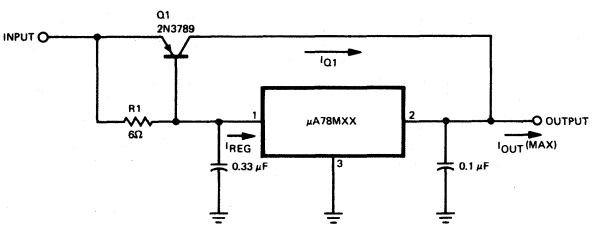


NOTES:
① To specify an output voltage, substitute voltage value for "XX".
② Although no output capacitor is needed for stability, it does improve transient response.
③ Required if regulator is located an appreciable distance from power supply filter.

FIXED OUTPUT REGULATOR

NEGATIVE OUTPUT VOLTAGE CIRCUIT





$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

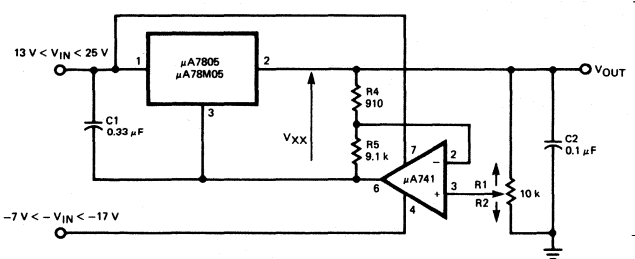
$$R_{SC} = \frac{V_{BE(Q1)}}{I_{OUT}}$$

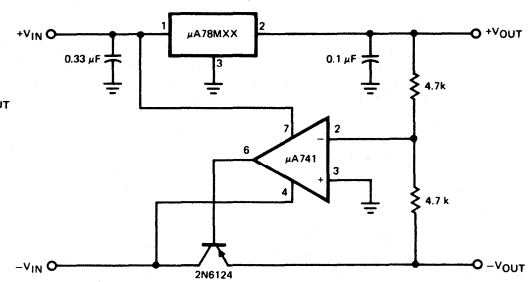
$$R1 = \frac{V_{BE(Q1)}}{I_{REG}} = \frac{\beta V_{BE(Q1)}}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

$$\beta_{Q1} \geq \frac{I_{OUT}}{I_{REG}}$$

HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED

HIGH CURRENT VOLTAGE REGULATOR

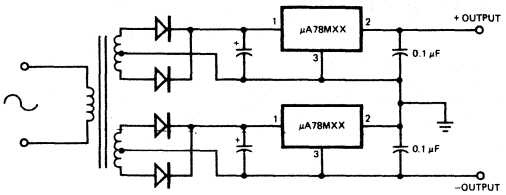




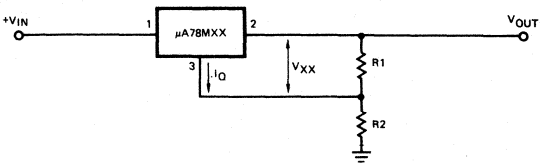
VARIABLE OUTPUT VOLTAGE, 0.5 TO 10 V

± TRACKING VOLTAGE REGULATOR

APPLICATIONS (Cont'd)

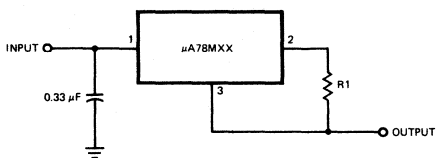


POSITIVE AND NEGATIVE REGULATOR



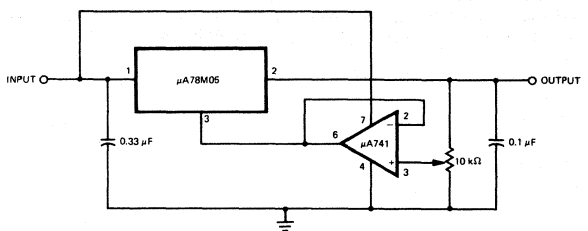
$$V_{OUT} = V_{XX}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

CIRCUIT FOR INCREASING OUTPUT VOLTAGE



$$\text{Output Current} = \frac{V_{OUT}}{R1}$$

CURRENT REGULATOR



ADJUSTABLE OUTPUT REGULATOR, 7 V TO 30 V

14

μA7900 SERIES

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA7900 series of monolithic 3-Terminal Negative Regulators is manufactured using the Fairchild Planar* epitaxial process. These negative regulators are intended as complements to the popular μA7800 series of positive voltage regulators, and they are available in the same voltage options from −5 to −24 V. The 7900s employ internal current limiting, safe-area protection, and thermal shutdown, making them virtually indestructible.

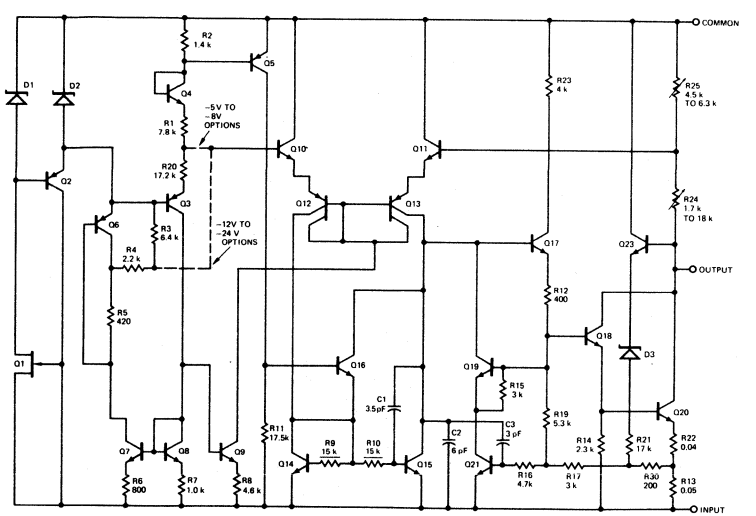
- **OUTPUT CURRENT IN EXCESS OF 1 A**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE AREA COMPENSATION**
- **AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE**
- **OUTPUT VOLTAGES ARE 5, 6, 8, 12, 15, 18 AND 24 V**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
(5 V through 18 V)	−35 V
(24 V)	−40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-3 (Al. or Steel)	−65°C to +150°C
TO-220	−55°C to +150°C
Operating Junction Temperature Range	
Military (μA7900)	−55°C to +150°C
Commercial (μA7900C)	0°C to +150°C
Lead Temperature	
TO-3 (Soldering, 60 s)	300°C
TO-220 (Soldering, 10 s)	230°C

NOTE: The convention for Negative Regulators is the Algebraic value, thus −15 is less than −10 V.

EQUIVALENT CIRCUIT

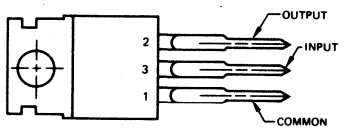


Resistor values in Ω unless otherwise noted.

*Planar is a patented Fairchild process.

CONNECTION DIAGRAMS

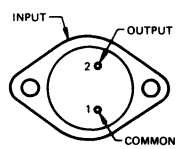
TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
−5 V	μA7905C	μA7905UC
−6 V	μA7906C	μA7906UC
−8 V	μA7908C	μA7908UC
−12 V	μA7912C	μA7912UC
−15 V	μA7915C	μA7915UC
−18 V	μA7918C	μA7918UC
−24 V	μA7924C	μA7924UC

TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
−5 V	μA7905	μA7905KM
−6 V	μA7906	μA7906KM
−8 V	μA7908	μA7908KM
−12 V	μA7912	μA7912KM
−15 V	μA7915	μA7915KM
−18 V	μA7918	μA7918KM
−24 V	μA7924	μA7924KM
−5 V	μA7905C	μA7905KC
−6 V	μA7906C	μA7908KC
−8 V	μA7908C	μA7908KC
−12 V	μA7912C	μA7912KC
−15 V	μA7915C	μA7915KC
−18 V	μA7918C	μA7918KC
−24 V	μA7924C	μA7924KC

μA7905

ELECTRICAL CHARACTERISTICS (V_{IN} = −10 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−4.8	−5.0	−5.2	V
Line Regulation		T_J = 25°C	−7 V ≤ V_{IN} ≤ −25 V		3	50	mV
			−8 V ≤ V_{IN} ≤ −12 V		1	25	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	50	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	25	mV
Output Voltage		−8.0 V ≤ V_{IN} ≤ −20 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−4.70		−5.30	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−8 V ≤ V_{IN} ≤ −25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			125		μV
Ripple Rejection		f = 120 Hz, −8 V ≤ V_{IN} ≤ −18 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−0.4		mV/°C

μA7905C

ELECTRICAL CHARACTERISTICS (V_{IN} = −10 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−4.8	−5.0	−5.2	V
Line Regulation		T_J = 25°C	−7 V ≤ V_{IN} ≤ −25 V		3.0	100	mV
			−8 V ≤ V_{IN} ≤ −12 V		1.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5.0	50	mV
Output Voltage		−7 V ≤ V_{IN} ≤ −20 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−4.75		−5.25	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−7 V ≤ V_{IN} ≤ −25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			125		μV
Ripple Rejection		f = 120 Hz, −8 V ≤ V_{IN} ≤ −18 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.4		mV/°C

μA7906

ELECTRICAL CHARACTERISTICS (V_{IN} = –11 V, I_{OUT} = 500 mA, –55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		–5.75	–6.0	–6.25	V
Line Regulation		T_J = 25°C	–8 V ≤ V_{IN} ≤ –25 V		5.0	60	mV
			–9 V ≤ V_{IN} ≤ –13 V		1.5	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		14	60	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	30	mV
Output Voltage		–9 V ≤ V_{IN} ≤ –21 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		–5.65		–6.35	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	–9 V ≤ V_{IN} ≤ –25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			150		μV
Ripple Rejection		f = 120 Hz, –9 V ≤ V_{IN} ≤ –19 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			–0.4		mV/°C

μA7906C

ELECTRICAL CHARACTERISTICS (V_{IN} = –11 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		–5.75	–6.0	–6.25	V
Line Regulation		T_J = 25°C	–8 V ≤ V_{IN} ≤ –25 V		5.0	120	mV
			–9 V ≤ V_{IN} ≤ –13 V		1.5	60	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		14	120	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	60	mV
Output Voltage		–8 V ≤ V_{IN} ≤ –21 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		–5.7		–6.3	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	–8 V ≤ V_{IN} ≤ –25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			150		μV
Ripple Rejection		f = 120 Hz, –9 V ≤ V_{IN} ≤ –19 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ V_{IN} ≤ 125°C			–0.4		mV/°C

μA7908

ELECTRICAL CHARACTERISTICS (V_{IN} = −14 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−7.7	−8.0	−8.3	V
Line Regulation		T_J = 25°C	−10.5 V ≤ V_{IN} ≤ −25 V		6.0	80	mV
			−11 V ≤ V_{IN} ≤ −17 V		2.0	40	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	80	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	40	mV
Output Voltage		−11.5 V ≤ V_{IN} ≤ −23 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−7.6		−8.4	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−11.5 V ≤ V_{IN} ≤ −25 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			200		μV
Ripple Rejection		f = 120 Hz, −11.5 V ≤ V_{IN} ≤ −21.5 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−0.6		mV/°C

μA7908C

ELECTRICAL CHARACTERISTICS (V_{IN} = −14 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−7.7	−8.0	−8.3	V
Line Regulation		T_J = 25°C	−10.5 V ≤ V_{IN} ≤ −25 V		6.0	160	mV
			−11 V ≤ V_{IN} ≤ −17 V		2.0	80	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	160	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	80	mV
Output Voltage		−10.5 V ≤ V_{IN} ≤ −23 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−7.6		−8.4	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−10.5 V ≤ V_{IN} ≤ −25 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz, ≤ f ≤ 100 kHz			200		μV
Ripple Rejection		f = 120 Hz, −11.5 V ≤ V_{IN} ≤ −21.5 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.6		mV/°C

μA7912

ELECTRICAL CHARACTERISTICS (V_{IN} = −19 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−11.5	−12.0	−12.5	V
Line Regulation		T_J = 25°C	−14.5 V ≤ V_{IN} ≤ −30 V		10	120	mV
			−16 V ≤ V_{IN} ≤ −22 V		3.0	60	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	120	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	60	mV
Output Voltage		−15.5 V ≤ V_{IN} ≤ −27 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−11.4		−12.6	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−15 V ≤ V_{IN} ≤ −30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			300		μV
Ripple Rejection		f = 120 Hz, −15 V ≤ V_{IN} ≤ −25 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−0.8		mV/°C

μA7912C

ELECTRICAL CHARACTERISTICS (V_{IN} = −19 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−11.5	−12.0	−12.5	V
Line Regulation		T_J = 25°C	−14.5 V ≤ V_{IN} ≤ −30 V		10	240	mV
			−16 V ≤ V_{IN} ≤ −22 V		3.0	120	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	240	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	120	mV
Output Voltage		−14.5 V ≤ V_{IN} ≤ −27 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−11.4		−12.6	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−14.5 V ≤ V_{IN} ≤ −30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			300		μV
Ripple Rejection		f = 120 Hz, −15 V ≤ V_{IN} ≤ −25 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−0.8		mV/°C

μA7915

ELECTRICAL CHARACTERISTICS (V_{IN} = −23 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−14.4	−15.0	−15.6	V
Line Regulation		T_J = 25°C	−17.5 V ≤ V_{IN} ≤ −30 V		11	150	mV
			−20 V ≤ V_{IN} ≤ −26 V		3.0	75	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	150	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	75	mV
Output Voltage		−18.5 V ≤ V_{IN} ≤ −30 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−14.25		−15.75	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−18.5 V ≤ V_{IN} ≤ −30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			375		μA
Ripple Rejection		f = 120 Hz, −18.5 V ≤ V_{IN} ≤ −28.5 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.0		mV/°C

μA7915C

ELECTRICAL CHARACTERISTICS (V_{IN} = −23 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−14.4	−15.0	−15.6	V
Line Regulation		T_J = 25°C	−17.5 V ≤ V_{IN} ≤ −30 V		11	300	mV
			−20 V ≤ V_{IN} ≤ −26 V		3.0	150	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	300	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	150	mV
Output Voltage		−17.5 V ≤ V_{IN} ≤ −30 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−14.25		−15.75	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−17.5 V ≤ V_{IN} ≤ −30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			375		μV
Ripple Rejection		f = 120 Hz, −18.5 V ≤ V_{IN} ≤ −28.5 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.0		mV/°C

14

μA7918

ELECTRICAL CHARACTERISTICS (V_{IN} = –27 V, I_{OUT} = 500 mA, –55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		–17.3	–18.0	–18.7	V
Line Regulation		T_J = 25°C	–21 V ≤ V_{IN} ≤ –33 V		15	180	mV
			–24 V ≤ V_{IN} ≤ –30 V		5.0	90	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	180	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	90	mV
Output Voltage		–22 V ≤ V_{IN} ≤ –33 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		–17.1		–18.9	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	–22 V ≤ V_{IN} ≤ –33 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			450		μV
Ripple Rejection		f = 120 Hz, –22 V ≤ V_{IN} ≤ –32 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			–1.0		mV/°C

μA7918C

ELECTRICAL CHARACTERISTICS (V_{IN} = –27 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		–17.3	–18.0	–18.7	V
Line Regulation		T_J = 25°C	–21 V ≤ V_{IN} ≤ –33 V		15	360	mV
			–24 V ≤ V_{IN} ≤ –30 V		5.0	180	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	360	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	180	mV
Output Voltage		–21 V ≤ V_{IN} ≤ –33 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		–17.1		–18.9	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	–21 V ≤ V_{IN} ≤ –33 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			450		μV
Ripple Rejection		f = 120 Hz, –22 V ≤ V_{IN} ≤ –32 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			–1.0		mV/°C

μA7924

ELECTRICAL CHARACTERISTICS (V_{IN} = −33 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−23.0	−24.0	−25.0	V
Line Regulation		T_J = 25°C	−27 V ≤ V_{IN} ≤ −38 V		18	240	mV
			−30 V ≤ V_{IN} ≤ −36 V		6.0	120	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	240	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	120	mV
Output Voltage		−28 V ≤ V_{IN} ≤ −38 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−22.8		−25.2	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−28 V ≤ V_{IN} ≤ −38 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			600		μV
Ripple Rejection		f = 120 Ha, −28 V ≤ V_{IN} ≤ −38 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 150°C			−1.0		mV/°C

μA7924C

ELECTRICAL CHARACTERISTICS (V_{IN} = −33 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−23.0	−24.0	−25.0	V
Line Regulation		T_J = 25°C	−27 V ≤ V_{IN} ≤ −38 V		18	480	mV
			−30 V ≤ V_{IN} ≤ −36 V		6.0	240	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	480	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	240	mV
Output Voltage		−27 V ≤ V_{IN} ≤ −38 V 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W		−22.8		−25.2	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−27 V ≤ V_{IN} ≤ −38 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			600		μV
Ripple Rejection		f = 120 Hz, −28 V ≤ V_{IN} ≤ −38 V		54	60		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			1.1		V
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			−1.0		mV/°C

14

DESIGN CONSIDERATIONS

The μA7900 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 7900, 125°C for 7900C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	TYP θ_{JC}	MAX θ_{JC}	TYP θ_{JC}	MAX θ_{JA}
TO-3	3.5°C/W	5.5°C/W	40°C/W	45°C/W
TO-220	3.0°C/W	5.0°C/W	60°C/W	65°C/W

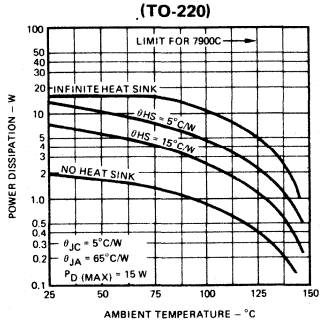
$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(MAX)}\ T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

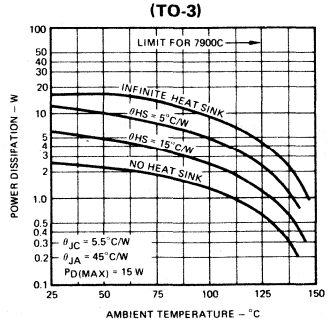
Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where
- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JA} = Junction to Ambient Thermal Resistance
- θ_{JC} = Junction to Case Thermal Resistance
- θ_{CA} = Case to Ambient Thermal Resistance
- θ_{CS} = Case to Heat Sink Resistance
- θ_{SA} = Heat Sink to Ambient Thermal Resistance

WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)

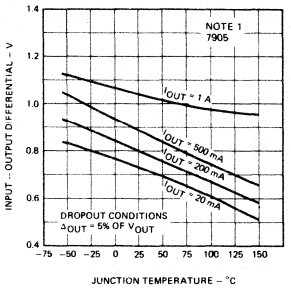


WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3)

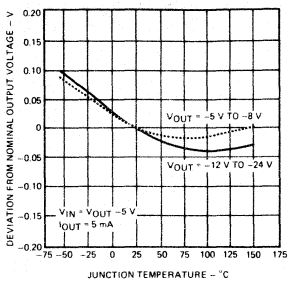


TYPICAL PERFORMANCE CURVES

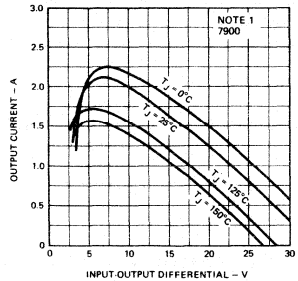
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



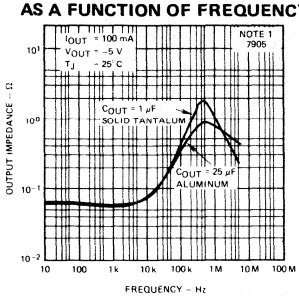
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



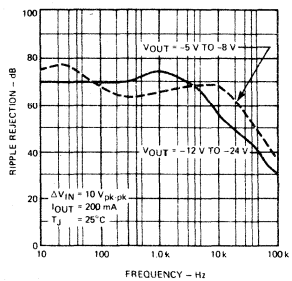
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



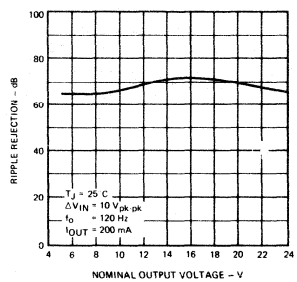
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



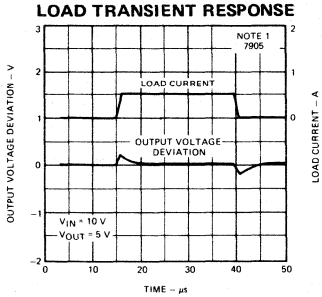
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



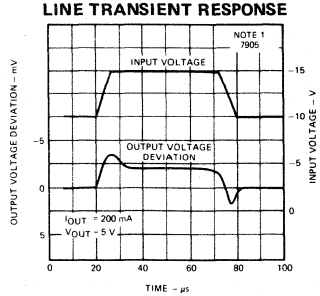
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



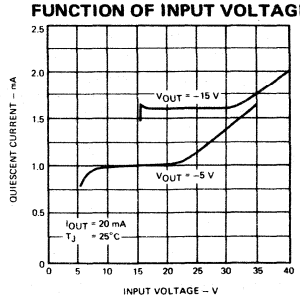
LOAD TRANSIENT RESPONSE



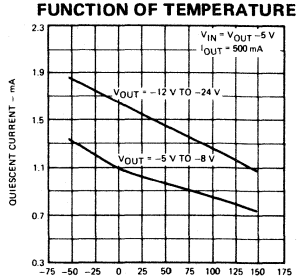
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



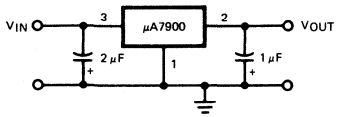
NOTE 1: The other μA7900 series devices have similar performance curves.

14

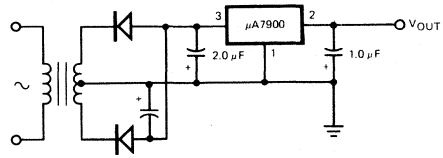
TYPICAL APPLICATIONS

Bypass capacitors are recommended for stable operation of the μA7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

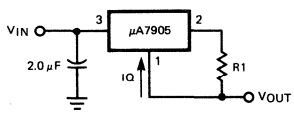
The bypass capacitors, (2 μF on the input, 1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.



FIXED OUTPUT REGULATOR

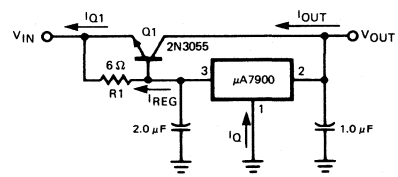


NEGATIVE OUTPUT VOLTAGE CIRCUIT



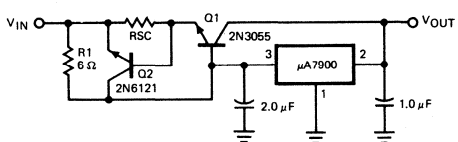
$$\text{OUTPUT CURRENT} = \frac{5.0\ \text{V}}{R1} + I_Q$$

BASIC CURRENT REGULATOR



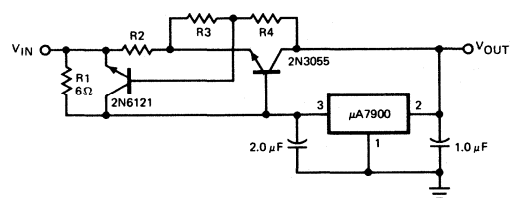
$$R1 = \frac{V_{BE(Q1)}}{I_{REG}} \qquad I_{Q1} = \beta(Q1) I_{REG}$$

HIGH CURRENT VOLTAGE REGULATOR

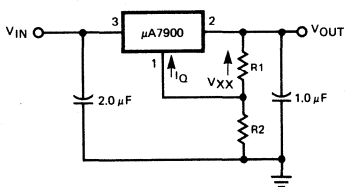


$$R_{SC} = \frac{V_{BE(Q2)}}{I_{SC}}$$

HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED

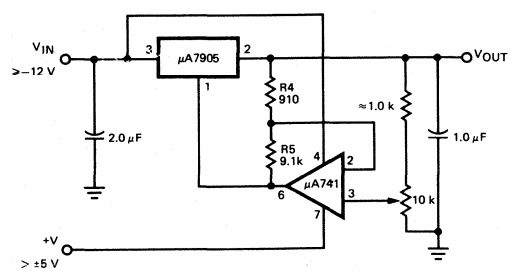


HIGH OUTPUT CURRENT, FOLDBACK CURRENT LIMITED



$$\left|V_{OUT}\right| = V_{XX}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

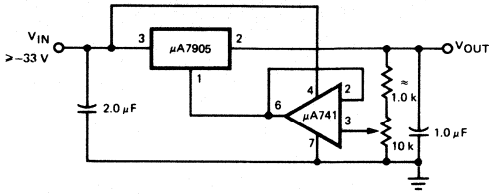
VARIABLE OUTPUT VOLTAGE REGULATOR



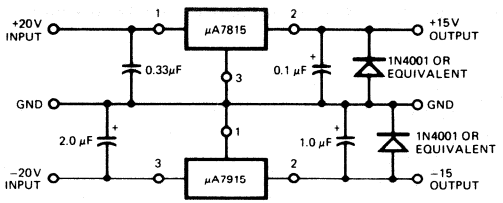
VARIABLE OUTPUT VOLTAGE, −0.5 V TO −10 V

TYPICAL APPLICATIONS (Cont'd)

VARIABLE OUTPUT VOLTAGE, −30 V TO −7 V



OPERATIONAL AMPLIFIER SUPPLY (± 15 V @ 1.0 A)



14

μA79M00 SERIES

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

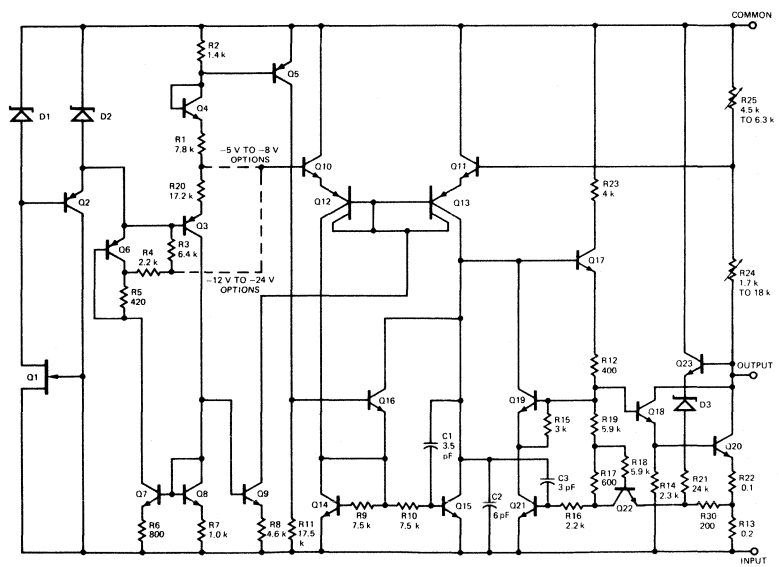
GENERAL DESCRIPTION – The μA79M00 series of 3-Terminal Medium Current Negative Voltage Regulators are constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE AREA COMPENSATION**
- **AVAILABLE IN JEDEC TO-220 AND TO-39 PACKAGES**
- **OUTPUT VOLTAGES OF –5 V, –6 V, –8 V, –12 V, –15 V, –20 V AND –24 V**

ABSOLUTE MAXIMUM RATINGS

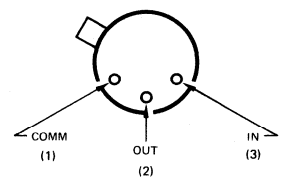
Input Voltage	
(–5 V through –15 V)	–35 V
(–20 V, –24 V)	–40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-39	–65°C to +150°C
TO-220	–55°C to +125°C
Operating Junction Temperature Range	
TO-39 Military (μA79M00)	–55°C to +150°C
Commercial (μA79M00C)	0°C to +150°C
TO-220 Commercial (μA79M00C)	0°C to +150°C
Lead Temperature (Soldering, 60 s) TO-39	300°C
(Soldering, 10 s) T)-220	230°C

EQUIVALENT CIRCUIT



Resistor values in kΩ unless otherwise noted.

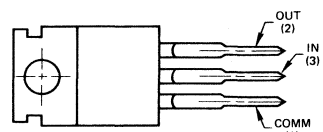
CONNECTION DIAGRAMS
TO-39 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE BF
PACKAGE CODE H



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.	PART NO.
–5 V	μA 79M05HM	μA 79M05AHC
–6 V	μA 79M06HM	μA 79M06AHC
–8 V	μA 79M08HM	μA 79M08AHC
–12 V	μA 79M12HM	μA 79M12AHC
–15 V	μA 79M15HM	μA 79M15AHC
–20 V	μA 79M20HM	μA 79M20AHC
–24 V	μA 79M24HM	μA 79M24AHC

TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.
–5 V	μA 79M05AUC
–6 V	μA 79M06AUC
–8 V	μA 79M08AUC
–12 V	μA 79M12AUC
–15 V	μA 79M15AUC
–20 V	μA 79M20AUC
–24 V	μA 79M24AUC

NOTE:
Product previously specified as HC or UC has been deleted.

Notes on following pages.

*Planar is a patented Fairchild process.

μA79M05HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −10 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified) Note 1 & 2

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−5.2	−5.0	−4.8	V
Line Regulation		T_J = 25°C	−25 V ≤ V_{IN} ≤ −7 V		7.0	50	mV
			−18 V ≤ V_{IN} ≤ −8 V		3.0	30	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			75	100	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			50		mV
Output Voltage		−25 V ≤ V_{IN} ≤ −7 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−5.25		−4.75	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−25 V ≤ V_{IN} ≤ −8 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			125		μV
Ripple Rejection		−18 V ≤ V_{IN} ≤ −8 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.4		mV/°C

μA79M05AHC AND μA79M05AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −10 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−5.2	−5.0	−4.8	V
Line Regulation		T_J = 25°C	−25 V ≤ V_{IN} ≤ −7 V		7.0	50	mV
			−18 V ≤ V_{IN} ≤ −8 V		3.0	30	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			75	100	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			50		mV
Output Voltage		−25 V ≤ V_{IN} ≤ −7 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−5.25		−4.75	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−25 V ≤ V_{IN} ≤ −8 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			125		μV
Ripple Rejection		−18 V ≤ V_{IN} ≤ −8 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.4		mV/°C

*P_D ≤ 4 W

NOTES:

1. See Test Circuit.
2. The convention for negative regulators is the algebraic valves, thus −15 V is less than −10 V.

14

μA79M06HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −11 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−6.25	−6.0	−5.75	V
Line Regulation		T_J = 25°C	−25 V ≤ V_{IN} ≤ −8 V		7.0	60	mV
			−19 V ≤ V_{IN} ≤ −9 V		3.0	40	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			80	120	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA*			55		mV
Output Voltage		−25 V ≤ V_{IN} ≤ −8 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−6.3		−5.7	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−25 V ≤ V_{IN} ≤ −9 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			150		μV
Ripple Rejection		−19 V ≤ V_{IN} ≤ −9 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.4		mV/°C

μA79M06AHC AND μA79M06AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −11 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−6.25	−6.0	−5.75	V
Line Regulation		T_J = 25°C	−25 V ≤ V_{IN} ≤ −8 V		7.0	60	mV
			−19 V ≤ V_{IN} ≤ −9 V		3.0	40	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			80	120	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			55		mV
Output Voltage		−25 V ≤ V_{IN} ≤ −8 V, 5 mA ≤ I_{OUT} ≤ 350 mA		−6.3		−5.7	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−25 V ≤ V_{IN} ≤ −9 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			150		μV
Ripple Rejection		−19 V ≤ V_{IN} ≤ −9 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.4		mV/°C

*P_D ≤ 4 W

μA79M08HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −14 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−8.3	−8.0	−7.7	V
Line Regulation		T_J = 25°C	−25 V ≤ V_{IN} ≤ −10.5 V		8.0	80	mV
			−21 V ≤ V_{IN} ≤ −11 V		4.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			90	160	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			60		mV
Output Voltage		−25 V ≤ V_{IN} ≤ −10.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−8.4		−7.6	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−25 V ≤ V_{IN} ≤ −10.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			200		μV
Ripple Rejection		−21.5 V ≤ V_{IN} ≤ −11.5 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	59		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.6		mV/°C

μA79M08AHC AND μA79M08AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −14 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−8.3	−8.0	−7.7	V
Line Regulation		T_J = 25°C	−25 V ≤ V_{IN} ≤ −10.5 V		8.0	80	mV
			−21 V ≤ V_{IN} ≤ −11 V		4.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			90	160	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			60		mV
Output Voltage		−25 V ≤ V_{IN} ≤ −10.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA		−8.4		−7.6	V
Quiescent Current		T_J = 25°C			1.0	2.0	mA
Quiescent Current Change	with line	−25 V ≤ V_{IN} ≤ −10.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			200		μV
Ripple Rejection		−21.5 V ≤ V_{IN} ≤ −11.5 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	59		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.6		mV/°C

*P_D ≤ 4 W

14

μA79M12HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −19 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−12.5	−12	−11.5	V
Line Regulation		T_J = 25°C	−30 V ≤ V_{IN} ≤ −14.5 V		9.0	80	mV
			−25 V ≤ V_{IN} ≤ −15 V		5.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			65	240	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			45		mV
Output Voltage		−30 V ≤ V_{IN} ≤ −14.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−12.6		−11.4	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−30 V ≤ V_{IN} ≤ −14.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			300		μV
Ripple Rejection		−25 V ≤ V_{IN} ≤ −15 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.8		mV/°C

μA79M12AHC AND μA79M12AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −19 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−12.5	−12	−11.5	V
Line Regulation		T_J = 25°C	−30 V ≤ V_{IN} ≤ −14.5 V		9.0	80	mV
			−25 V ≤ V_{IN} ≤ −15 V		5.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			65	240	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			45		mV
Output Voltage		−30 V ≤ V_{IN} ≤ −14.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA		−12.6		−11.4	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−30 V ≤ V_{IN} ≤ −14.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			300		μV
Ripple Rejection		−25 V ≤ V_{IN} ≤ −15 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	60		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−0.8		mV/°C

*P_D ≤ 4 W

μA79M15HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −23 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−15.6	−15	−14.4	V
Line Regulation		T_J = 25°C	−30 V ≤ V_{IN} ≤ −17.5 V		9.0	80	mV
			−28 V ≤ V_{IN} ≤ −18 V		7.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			65	240	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			45		mV
Output Voltage		−30 V ≤ V_{IN} ≤ −17.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−15.75		−14.25	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−30 V ≤ V_{IN} ≤ −17.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			375		μV
Ripple Rejection		−28.5 V ≤ V_{IN} ≤ −18.5 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	59		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA79M15AHC AND μA79M15AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −23 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−15.6	−15	−14.4	V
Line Regulation		T_J = 25°C	−30 V ≤ V_{IN} ≤ −17.5 V		9.0	80	mV
			−28 V ≤ V_{IN} ≤ −18 V		7.0	50	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			65	240	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			45		mV
Output Voltage		−30 V ≤ V_{IN} ≤ −17.5 V, 5 mA ≤ I_{OUT} ≤ 350 mA		−15.75		−14.25	V
Quiescent Current		T_J = 25°C			1.5	3.0	mA
Quiescent Current Change	with line	−30 V ≤ V_{IN} ≤ −17.5 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			375		μV
Ripple Rejection		−28.5 V ≤ V_{IN} ≤ −18.5 V,	I_{OUT} = 100 mA	50			dB
		f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	54	59		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

*P_D ≤ 4 W

14

μA79M20HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −29 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−20.8	−20	−19.2	V
Line Regulation		T_J = 25°C	−35 V ≤ V_{IN} ≤ −23 V		12	80	mV
			−34 V ≤ V_{IN} ≤ −24 V		10	70	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			75	300	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			50		mV
Output Voltage		−35 V ≤ V_{IN} ≤ −23 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−21		−19	V
Quiescent Current		T_J = 25°C			1.5	3.5	mA
Quiescent Current Change	with line	−35 V ≤ V_{IN} ≤ −23 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			500		μV
Ripple Rejection		−34 V ≤ V_{IN} ≤ −24 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	58		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

μA79M20AHC AND μA79M20AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −29 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−20.8	−20	−19.2	V
Line Regulation		T_J = 25°C	−35 V ≤ V_{IN} ≤ −23 V		12	80	mV
			−34 V ≤ V_{IN} ≤ −24 V		10	70	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			75	300	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			50		mV
Output Voltage		−35 V ≤ V_{IN} ≤ −23 V, 5 mA ≤ I_{OUT} ≤ 350 mA		−21		−19	V
Quiescent Current		T_J = 25°C			1.5	3.5	mA
Quiescent Current Change	with line	−35 V ≤ V_{IN} ≤ −23 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			500		μV
Ripple Rejection		−34 V ≤ V_{IN} ≤ −24 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	58		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

*P_D ≤ 4 W

μA79M24HM

ELECTRICAL CHARACTERISTICS
(V_{IN} = −33 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−25	−24	−23	V
Line Regulation		T_J = 25°C	−38 V ≤ V_{IN} ≤ −27 V		12	80	mV
			−38 V ≤ V_{IN} ≤ −28 V		12	70	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			75	300	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			50		mV
Output Voltage		−38 V ≤ V_{IN} ≤ −27 V, 5 mA ≤ I_{OUT} ≤ 350 mA*		−25.2		−22.8	V
Quiescent Current		T_J = 25°C			1.5	3.5	mA
Quiescent Current Change	with line	−38 V ≤ V_{IN} ≤ −27 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			600		μV
Ripple Rejection		−38 V ≤ V_{IN} ≤ −28 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	58		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

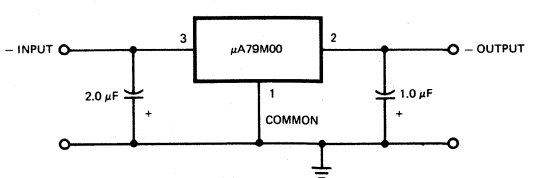
μA79M24AHC AND μA79M24AUC

ELECTRICAL CHARACTERISTICS
(V_{IN} = −33 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 2 μF, C_{OUT} = 1 μF, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C		−25	−24	−23	V
Line Regulation		T_J = 25°C	−38 V ≤ V_{IN} ≤ −27 V		12	80	mV
			−38 V ≤ V_{IN} ≤ −28 V		12	70	mV
Load Regulation		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 500 mA			75	300	mV
		T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 350 mA			50		mV
Output Voltage		−38 V ≤ V_{IN} ≤ −27 V, 5 mA ≤ I_{OUT} ≤ 350 mA		−25.2		−22.8	V
Quiescent Current		T_J = 25°C			1.5	3.5	mA
Quiescent Current Change	with line	−38 V ≤ V_{IN} ≤ −27 V				0.4	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.4	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			600		μV
Ripple Rejection		−38 V ≤ V_{IN} ≤ −28 V, f = 120 Hz	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	58		dB
Dropout Voltage		T_J = 25°C			1.1		V
Short Circuit Current		T_J = 25°C, V_{IN} = −30 V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			−1.0		mV/°C

*P_D ≤ 4 W

DC PARAMETER TEST CIRCUIT



14

DESIGN CONSIDERATIONS

The μA79M00 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 79M00, 125°C for 79M00AC and 79M00C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

	TYP	MAX	TYP	MAX
PACKAGE	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
TO-39	18.0	25	120	185
TO-220	3.0	5.0	62	70

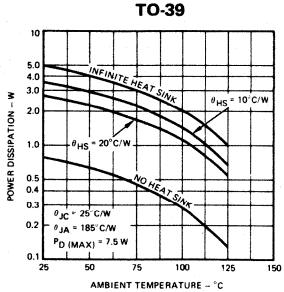
$$P_{D\,(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(MAX)} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

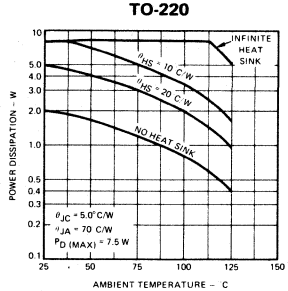
Solving for T_J: $T_J = T_A + P_D(\theta_{JC}+\theta_{CA})$ or $T_A + P_D\,\theta_{JA}$ (Without a heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance
θ_{JA} = Junction to ambient thermal resistance

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE TO-39

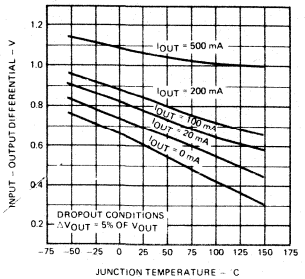


WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE TO-220

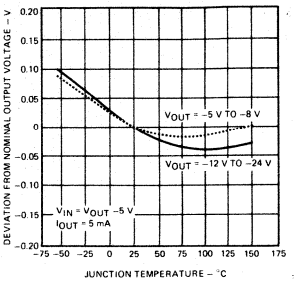


TYPICAL PERFORMANCE CURVES

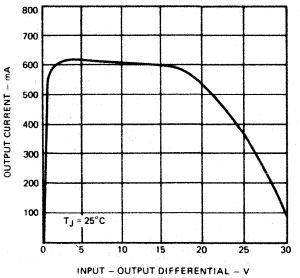
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



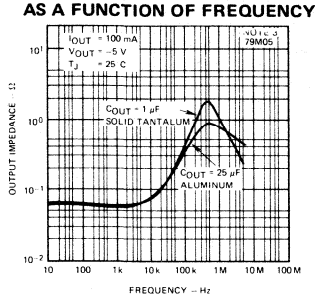
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



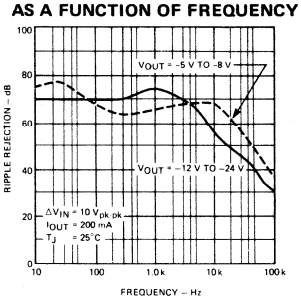
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



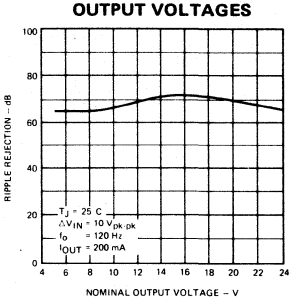
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



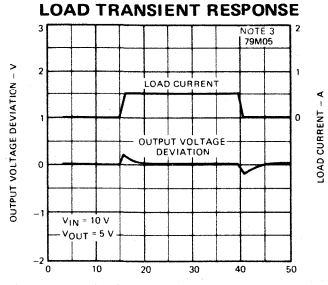
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



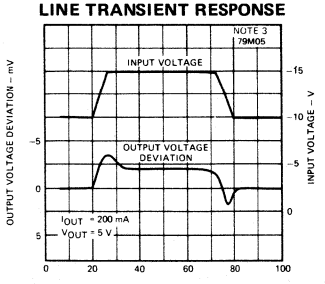
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



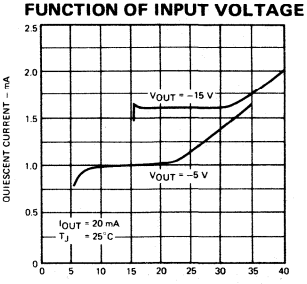
LOAD TRANSIENT RESPONSE



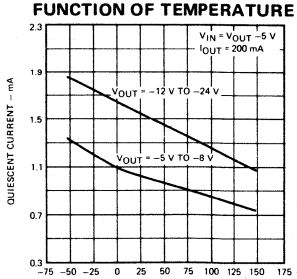
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



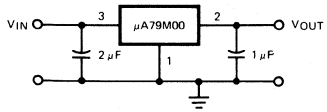
NOTE 3: The other μA79M00 voltage series devices have similar performance curves.

14

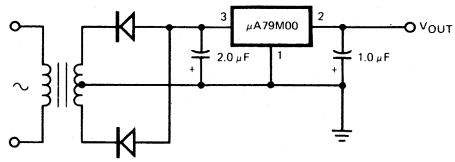
TYPICAL APPLICATIONS

Bypass capacitors are recommended for stable operation of the 79M00 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

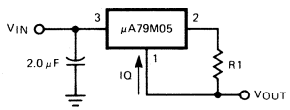
The bypass capacitors, (2 μF on the input, 1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.



FIXED OUTPUT REGULATOR

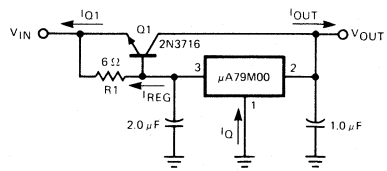


NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$\text{OUTPUT CURRENT} = \frac{5.0\ \text{V}}{R1} + I_Q$$

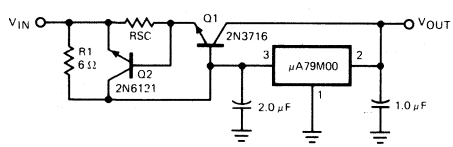
BASIC CURRENT REGULATOR



$$R1 = \frac{V_{BE(Q1)}}{I_{REG}} = \frac{\beta V_{BE(Q1)}}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

$$I_{Q1} = \beta(Q1) I_{REG}$$

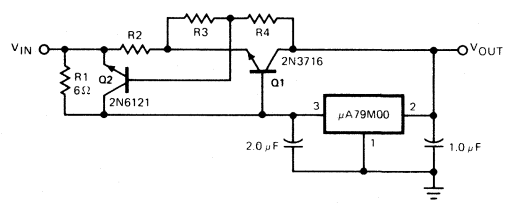
HIGH CURRENT VOLTAGE REGULATOR



$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

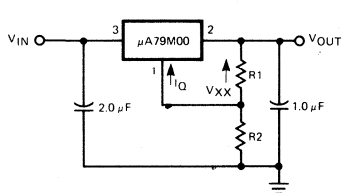
$$R_{SC} = \frac{V_{BE(Q2)}}{I_{SC}}$$

HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED



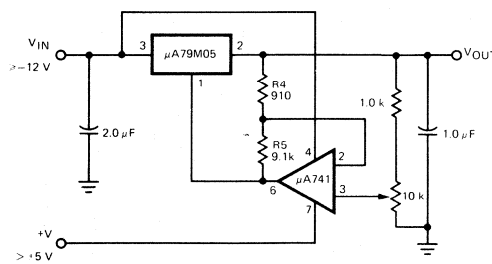
$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

HIGH OUTPUT CURRENT, FOLDBACK CURRENT LIMITED



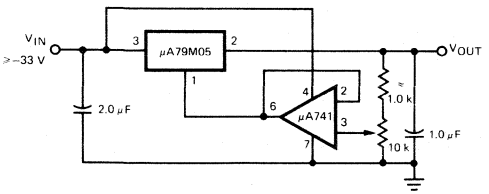
$$\left|V_{OUT}\right| = V_{XX}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

VARIABLE OUTPUT VOLTAGE REGULATOR

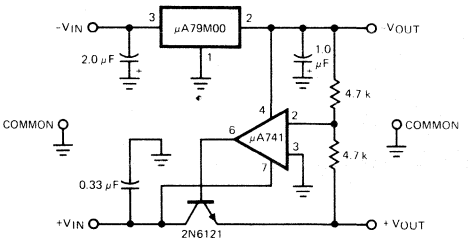


VARIABLE OUTPUT VOLTAGE, −0.5 V TO −10 V

TYPICAL APPLICATIONS (Cont'd)



VARIABLE OUTPUT VOLTAGE, −30 V TO −7 V



POSITIVE AND NEGATIVE TRACKING VOLTAGE REGULATOR

14

78H05

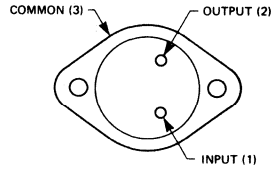
5 AMP VOLTAGE REGULATOR

FAIRCHILD INTEGRATED MICROSYSTEM

GENERAL DESCRIPTION – The 78H05 positive Voltage Regulator is a hybrid integrated circuit. The nominal output voltage is 5.0 V ± 200 mV. The output current capability is 5.0 A. Internal current limiting and thermal shutdown circuitry make the device essentially indestructible. The 78H05 is intended for a wide range of systems where a regulated 5.0 V supply is required and can be used for a variety of on-card regulation and circuit isolation applications.

- **5.0 A OUTPUT CURRENT**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **STANDARD TO-3 PACKAGE**

TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K



ABSOLUTE MAXIMUM RATINGS

Input Voltage	25 V
Internal Power Dissipation	50 W @ 25°C Case
Operating Junction Temperature Range	0°C to +150°C
Storage Temperature Range	−55°C to +150°C

ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5.0 V	78H05	78H05KC

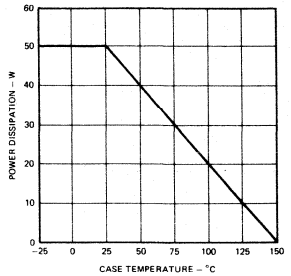
ELECTRICAL CHARACTERISTICS (V_{IN} = 10 V, I_{OUT} = 2.0 A, T_C = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage		4.8	5.0	5.2	V
Line Regulation	8.5 V ≤ V_{IN} ≤ 25 V		5.0	100	mV
Load Regulation	10 mA ≤ I_{OUT} ≤ 5.0 A		80	100	mV
Drop Out Voltage*	I_{OUT} = 3.0 A		2.6	3.0	V
Drop Out Voltage*	I_{OUT} = 5.0 A		3.0	3.5	V
Quiescent Current	I_{OUT} = 0 A			10	mA
Output Noise Voltage	BW = 10 Hz to 100 kHz		40		μV_{rms}
Ripple Rejection	f = 120 Hz, I_{OUT} = 1.0 A	60			dB
Thermal Resistance (Junction to Case)	V_{IN} = 20 V		2.0		°C/W

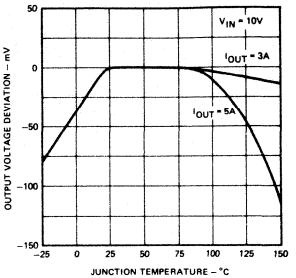
*That value of differential input-output voltage below which the line regulation exceeds the specified maximum value.

TYPICAL PERFORMANCE CHARACTERISTICS

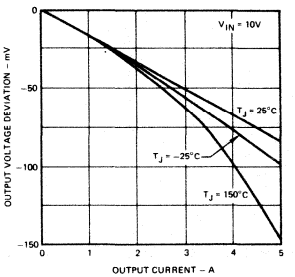
MAXIMUM POWER DISSIPATION



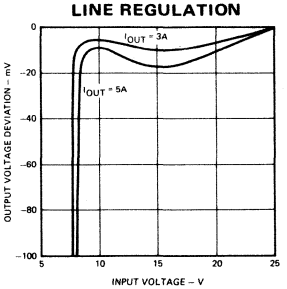
OUTPUT VOLTAGE DEVIATION AS A FUNCTION OF JUNCTION TEMPERATURE



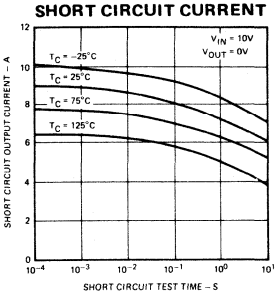
LOAD REGULATION



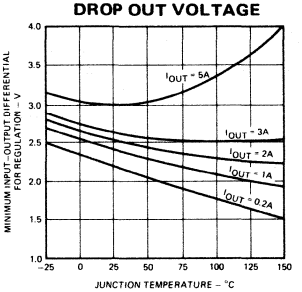
LINE REGULATION



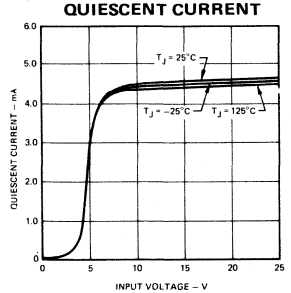
SHORT CIRCUIT CURRENT



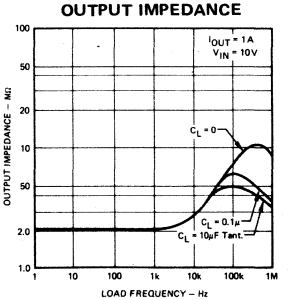
DROP OUT VOLTAGE



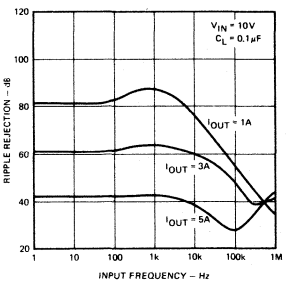
QUIESCENT CURRENT



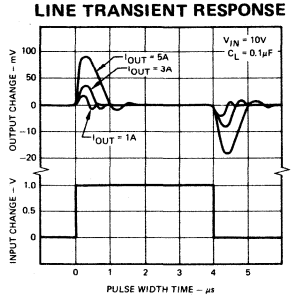
OUTPUT IMPEDANCE



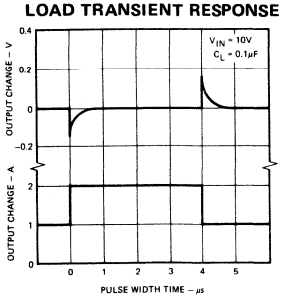
RIPPLE REJECTION



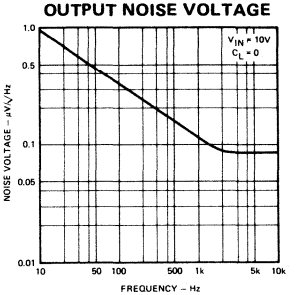
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



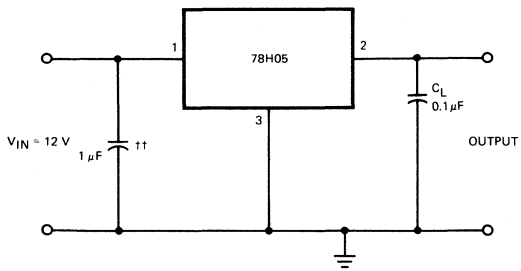
OUTPUT NOISE VOLTAGE



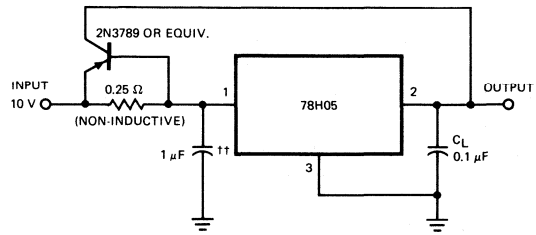
14

TYPICAL APPLICATIONS

5 AMP REGULATOR

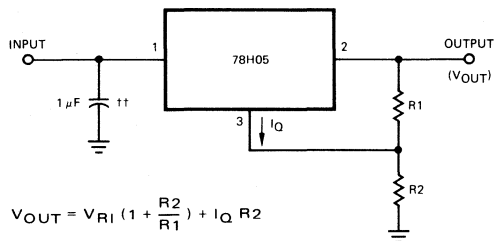


10 + AMP REGULATOR



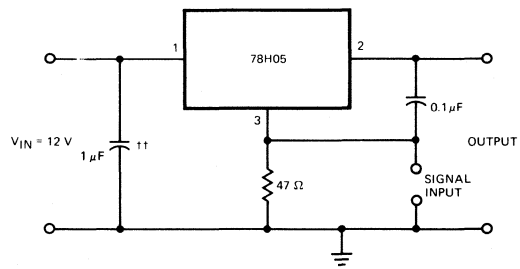
NOTES:
a. No current limit in effect
b. At 10 A out 78H05 passes 4.0 A
c. For 10 A output change, V_{OUT} changes approx. 80 mV

INCREASED OUTPUT VOLTAGE

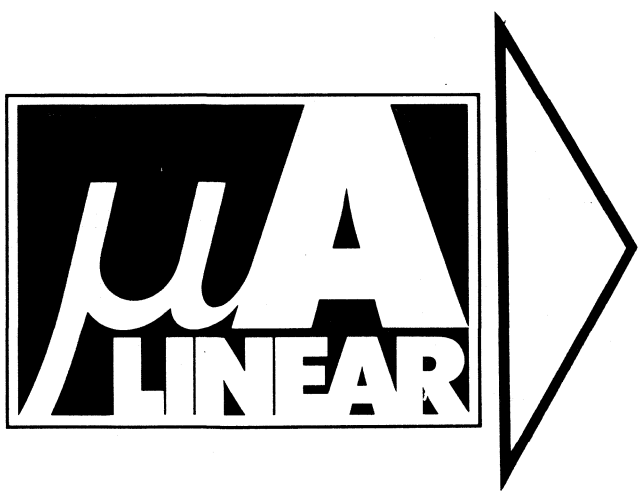


$$V_{OUT} = V_{RI}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

SIGNAL DRIVER/MODULATOR



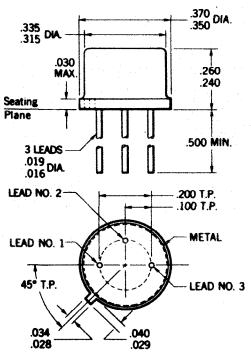
†† Required if regulator is located an appreciable distance from power supply filter.



PACKAGE OUTLINES

(H)CS

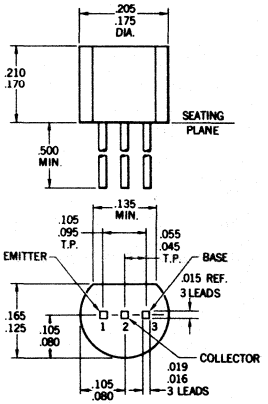
In Accordance with JEDEC (TO-39)



NOTES:
All dimensions in inches
Lead No. 3 connected to case
Low thermal resistance
Package weight is 0.76 gram

(W)EI

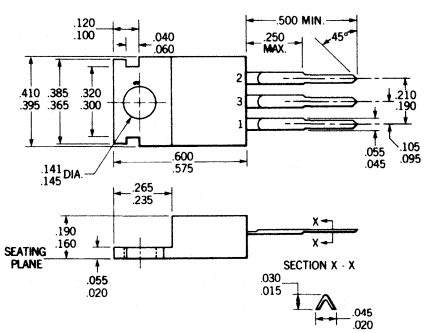
In Accordance with JEDEC (TO-92) Outline



NOTES:
All dimensions in inches
Leads are tin-plated copper
Package material is transfer molded thermosetting plastic
ECB configuration
Package weight is 0.25 gram

(U)GH

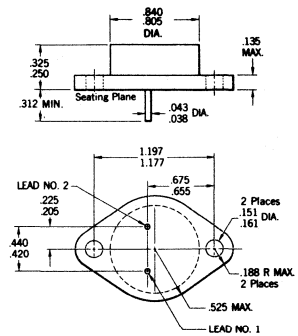
In Accordance with JEDEC (TO-220) Molded Power Package



NOTES:
All dimensions in inches
Mounting tab is electrically connected to COMMON
Package is molded with nickel plated copper tab and leads
Package weight is 2.1 grams

(K)GJ

In Accordance with JEDEC (TO-3)

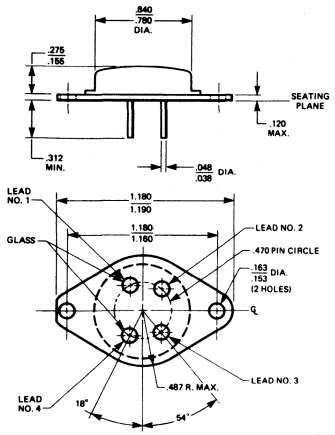


NOTES
All dimensions in inches
Leads 1 and 2 electrically isolated from case
Case is third electrical connection (COMMON)
Leads are gold-plated copper cored kovar
Package weight is 7.4 grams

PACKAGE OUTLINES

(K)GK

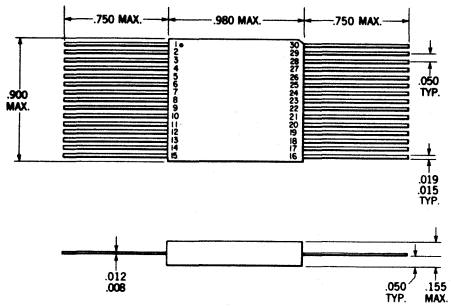
In Accordance with JEDEC (TO-3) Outline (4-Lead)



NOTES:
All dimensions in inches
Leads are gold-plated Alloy 52
All leads electrically isolated from case
Aluminum package
Package weight is 7.4 grams
Leads 1-4 located on a .470 dia. PC

(F) 2B

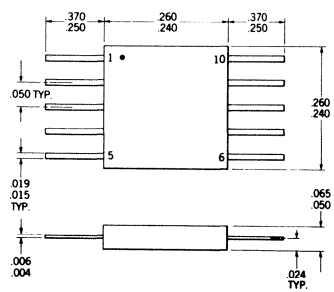
30-Lead Flatpak



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 5.0 grams
Package material is alumina

(F)3F

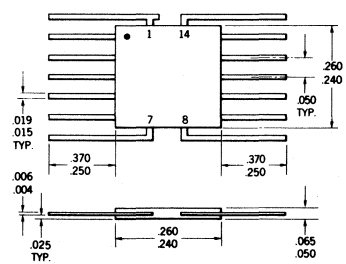
In Accordance with JEDEC (TO-91) 10-Lead Cerpak



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

(F)3 I

In Accordance with JEDEC (TO-86) 14-Lead Cerpak

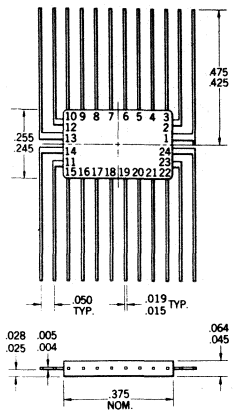


NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram
Lead 1 orientation may be either tab or dot

PACKAGE OUTLINES

(F)3M

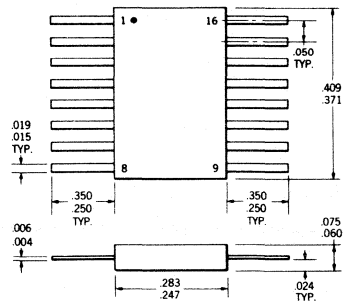
24-Lead Flatpak



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

(F)4L

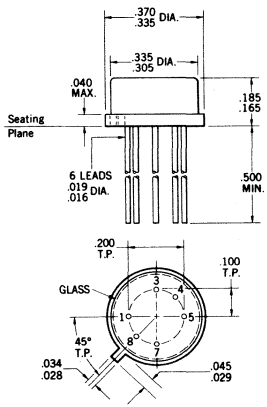
16-Lead Cerpak



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

(H)5C
5Z

In Accordance with JEDEC (TO-78)



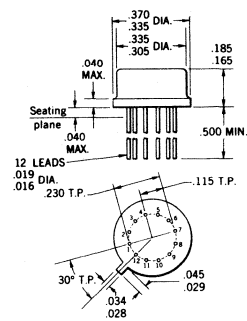
5C

NOTES:
All dimensions in inches
Leads are solder dipped
Package weight is ≈ 0.95 gram
Six leads through, leads 2 and 6 omitted

5Z
All dimensions in inches
Package weight is 0.95 gram
Six leads through, leads 2 and 6 omitted

(H)5D
5G

In Accordance with JEDEC (TO-101) Without Standoff



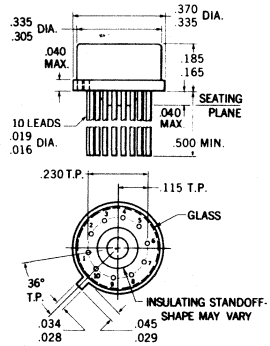
5D

NOTES:
All dimensions in inches
Leads are solder dipped
Similar to JEDEC TO-101 except no standoff
Package weight is ≈ 1.08 grams

5G
All dimensions in inches
Similar to JEDEC TO-101 except no standoff
Package weight is 1.08 grams

PACKAGE OUTLINES

In Accordance with JEDEC (TO-100)



(H)5I
5U

5I

NOTES:
All dimensions in inches
Leads are solder dipped
Package weight is ≈ 1.32 grams
High RTH package
Ten leads through

5U

All dimensions in inches
Package weight is 1.32 grams
High RTH package

(H)5N
5F

5N

NOTES:
All dimensions in inches
Leads are solder dipped
Package weight is ≈ 1.32 grams
Nine leads through, lead 5 is connected to case

5F

NOTES:
All dimensions in inches
Package weight is 2.31 grams
Nine leads through, lead 5 is connected to case

(H)5Q
5E

5Q

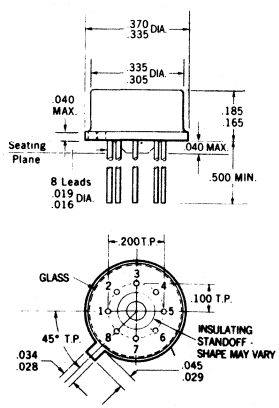
All dimensions in inches
Leads are solder dipped
Package weight is ≈ 1.32 grams
Ten leads through

5E

All dimensions in inches
Package weight is 1.32 grams

(H)5S
5B

In Accordance with JEDEC (TO-99)



5S

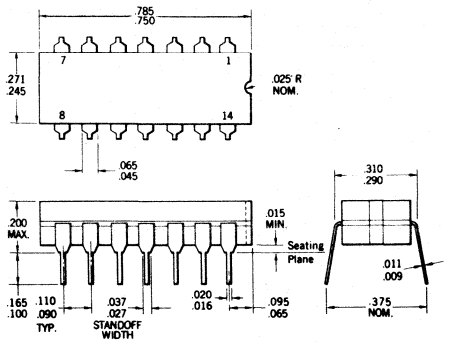
NOTES:
All dimensions in inches
Leads are solder dipped
Package weight is ≈ 1.22 grams
Seven leads through, lead 4 connected to case

5B

All dimensions in inches
Package weight is 1.22 grams
Seven leads through, lead 4 connected to case

(D)6A

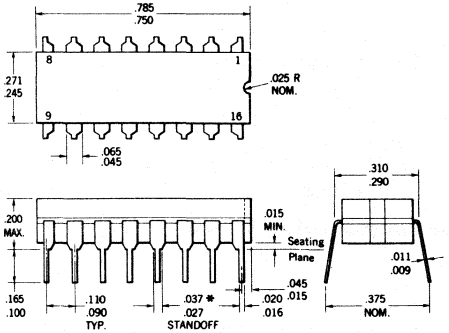
In Accordance with JEDEC (TO-116) 14-Lead Hermetic Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

(D)6B

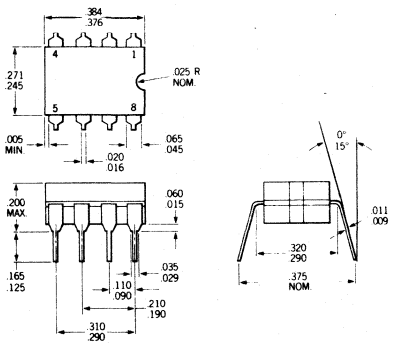
16-Lead Hermetic Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .027/.037 dimension does not apply to the corner leads

(R)6T

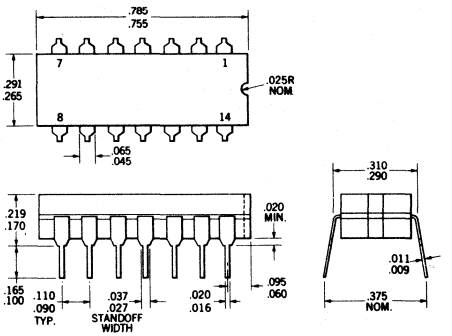
8-Lead SSI Dual In-line



NOTES:
All dimensions in inches
Leads are tin-plated kovar
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Hermetically sealed alumina package
Package weight is 1.0 grams

(D)7A

14-Lead Hermetic Dual In-line

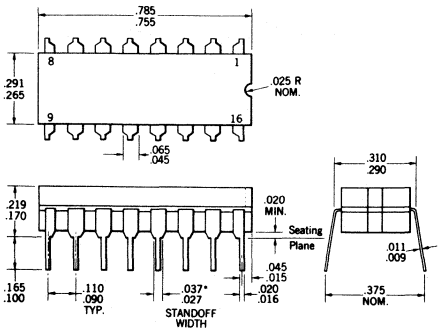


NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams

PACKAGE OUTLINES

(D)7B

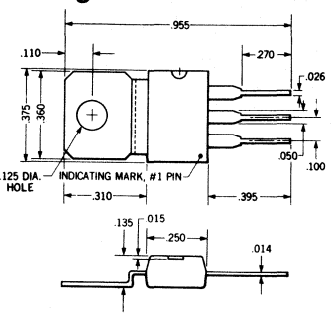
16-Lead Hermetic Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
The .037/.027 dimension does not apply to the corner leads

(U)8Y

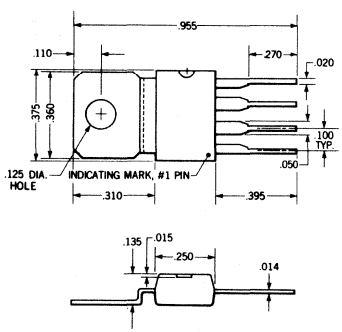
3-Lead Single Side Plastic Power-Tab



NOTES:
All dimensions in inches
Leads are tin-plated copper
Package weight is 0.6 gram
Package material is plastic
Center lead is in electrical contact with the mounting tab
This package is intended to be mounted with the heat sinking tab flush with the top of the PC board or heat sink. #4 screws may be used to secure this package. Thermal compound is recommended.

(U1)8Z

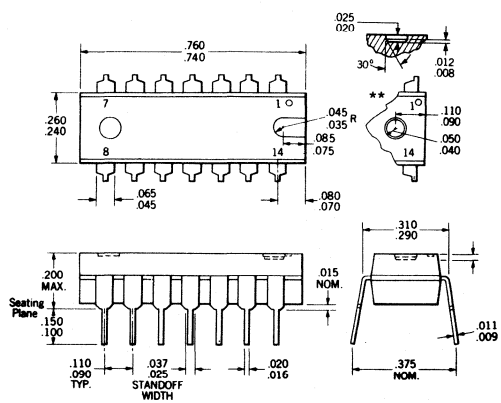
4-Lead Single Side Plastic Power Tab



NOTES:
All dimensions in inches
Leads are tin-plated copper
Board-drilling dimensions should equal you practice for .020 inch diameter lead
Package weight is 0.6 gram
Package material is plastic
Tab is electrically insulated from leads
This package is intended to be mounted with the heat sinking tab flush with the top of the PC board or heat sink. #4 screws may be used to secure this package. Thermal compound is recommended.

(P)9A

In Accordance with JEDEC (TO-116) 14-Lead Molded Dual In-line

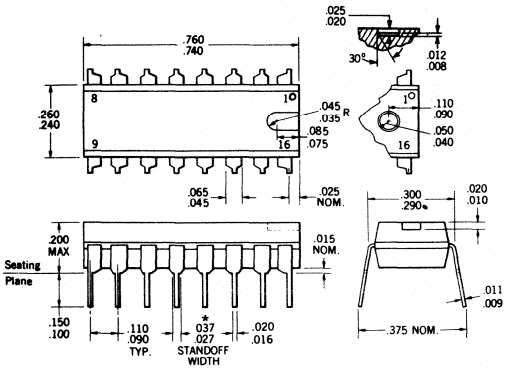


NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram

PACKAGE OUTLINES

(P)9B

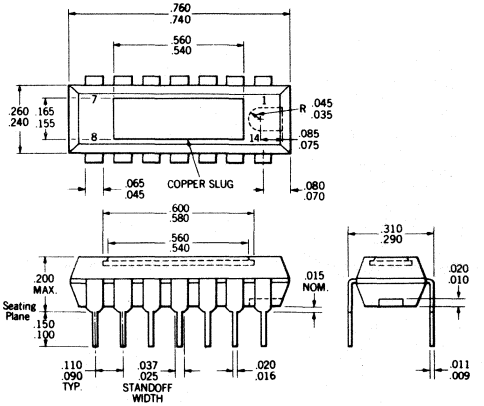
16-Lead Molded Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
*The .037/.027 dimension does not apply to the corner leads

(AP)9H

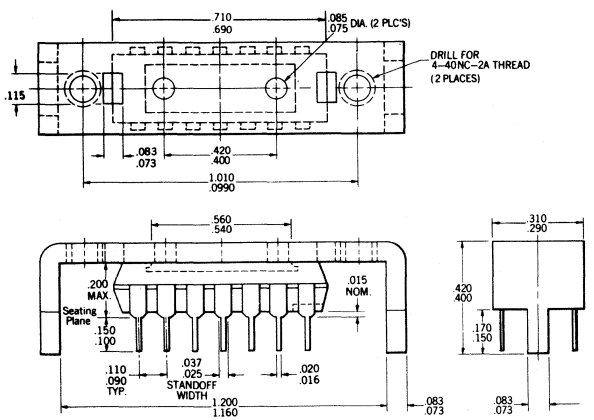
Dual In-line Power Package (DIPP)



NOTES:
All dimensions in inches
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Copper slug

(BP)9J

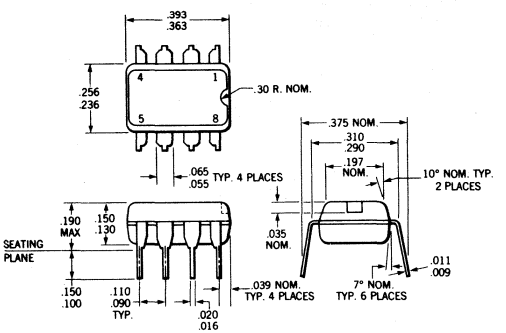
Dual In-line Power Package (DIPP) With Bracket Heat Sink



NOTES:
All dimensions in inches
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Copper slug and tin-plated copper bracket

(T)9T

8-Lead Molded Dual In-line

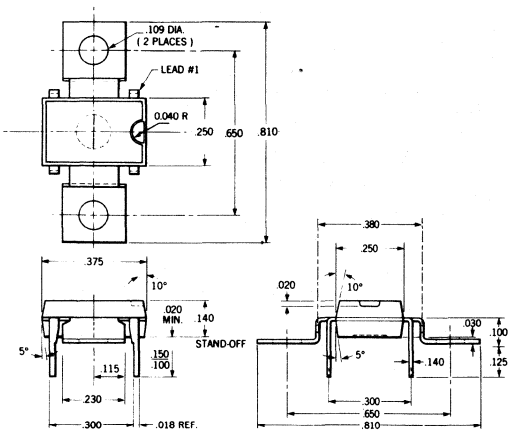


NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Package weight is 0.6 gram
Leads are tin or gold-plate kovar

PACKAGE OUTLINES

(T2)9V

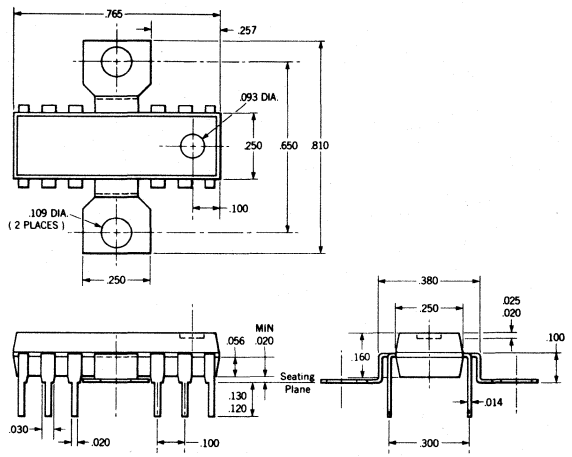
4-Lead Plastic Power Mini Dip



NOTES:
All dimensions in inches
Leads and wings are tin-plated copper
Package body is plastic
Package weight is 0.6 gram
This package is intended to be mounted with the heat sinking tabs flush with the top of the PC board or heat sink. Either #2-56 screws or #2 rivets may be used to secure this this package. Thermal compound is recommended.
The heat sinking tabs are electrically connected to the most negative potential lead.

(P5)9W

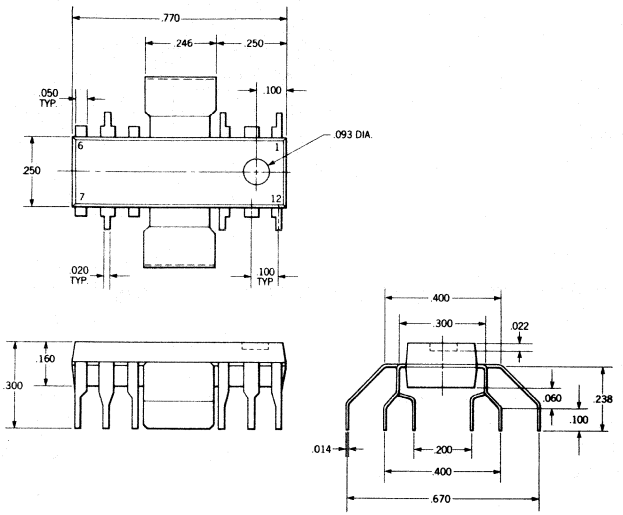
12-Lead Power Plastic Dual In-line



NOTES:
All dimensions in inches
Leads and wings are tin-plated copper
Package body is plastic
Package weight is 0.9 gram
This package is intended to be mounted with the heat sinking tabs flush with the top of the PC board or heat sink. Either #2-56 screws or #2 rivets may be used to secure this package. Thermal compound is recommended.
The heat sinking tabs are electrically connected to the most negative potential lead.

(P3) 9W

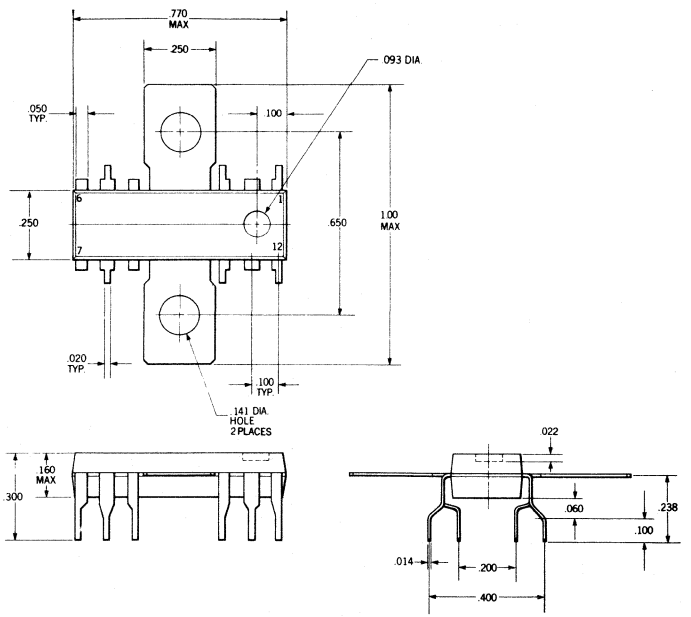
12-Lead Power Package



NOTES:
All dimensions in inches

(P4) 9W

12-Lead Power Package



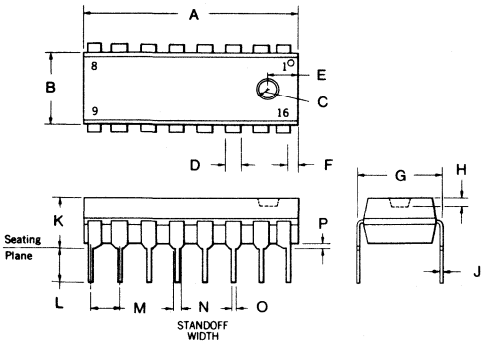
NOTES:
All dimensions in inches

PACKAGE OUTLINES

16-Lead Molded Dual In-line

9B

TAA630S, TBA510, TBA520, TBA530, TBA540, TBA560C, TBA920, TBA970, TBA990



DIM	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.740		.760	18.80		19.30
B	.240		.260	6.10		6.60
C	.035		.045	.89		1.14
D	.045		.065	1.14		1.65
E	.090		.110	2.29		2.79
F		.025			.64	
G	.290		.310	7.37		7.87
H	.010		.020	.25		.51
J	.009		.011	.23		.28
K			.200			5.08
L	.100		.150	2.54		3.81
M	.090		.110	2.29		2.79
*N	.027		.037	.69		.94
O	.016		.020	.41		.51
P		.015			.38	

NOTES:

See table for dimensions in inches and millimeters

Leads are intended for insertion in hole rows on .300" (.76 mm) centers

Board-drilling dimensions should equal your practice for .020" (.51 mm) diameter lead

Leads are tin-plated kovar

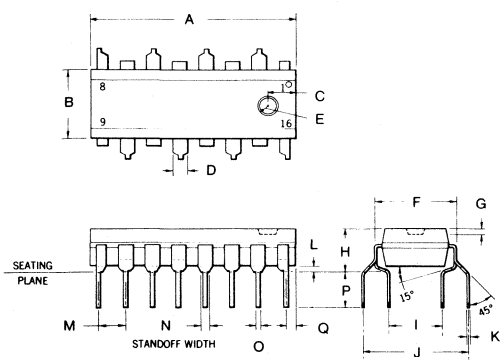
Package weight is 0.9 gram

*The .037"/.027" (.94/.64 mm) dimension does not apply to the corner leads

16-Lead Molded Quad** In-line

9B

TAA630T, TBA510Q, TBA520, TBA530Q, TBA540Q, TBA560CQ, TBA920Q, TBA970Q, TBA990Q



DIM	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.740		.760	18.80		19.30
B	.240		.260	6.10		6.60
C	.035		.045	.89		1.14
D	.045		.065	1.14		1.65
E	.090		.110	2.29		2.79
F	.290		.310	7.37		7.87
G	.010		.020	.25		.51
H			.200			5.08
I	.180		.220	4.57		5.59
J	.380		.420	9.65		10.67
K	.009		.011	.23		.28
L		.015			.38	
M	.090		.110	2.29		2.79
*N	.027		.037	.69		.94
O	.016		.020	.41		.51
P	.118		.138	3.00		3.51
Q		.025			.64	

NOTES:

All dimensions in millimeters

Leads are intended for insertion in hole rows on .300" (.76 mm) centers

Board-drilling dimensions should equal your practice for .020" (.51 mm) diameter lead

Leads are tin-plated kovar

Package weight is 0.9 gram

*The .037"/.027" (.94/.64 mm) dimension does not apply to the corner leads

LINEAR INTEGRATED CIRCUITS
APPLICATION INFORMATION

App. Note Index by Number

App. Note No.	
116	The Operation and Use of a Fast Intergrated Circuit Comparator
117/2	Frequency-Compensation Techniques fro an Integrated Operational Amplifier
171	Applications of the μA739 and μA749 Dual Preamplifier Integrated Circuits in Home Entertainment Equipment
175	The μA739, A Low-Noise Dual Operational Amplifier
199	Design Concepts for Low Cost Transistor AGC Systems
204	An Intergrated Circuit AGC IF Amplifier
205	Thermal Evaluation of Integrated Circuits
210	Integrated TV Chroma Processing System
218	The μA776, An Operational Amplifier with Programmable Gain, Bandwidth, Slew-Rate and Power Dissipation
265	The μA715, A Versatile High Speed Operational Amplifier
267	The μA746 Color TV Chroma Demodulator IC
268	Applications of the μA749 Dual Operational Amplifier
269	The μA749 Dual Operational Amplifier
277	A Low-Drift, Low-Noise Monolithic Operational Amplifier for Low Level Signal Prosessing
286/1	The μA732 and μA767 Integrated Circuit Stereo Multiplex Decoders
293	A Low-Level Wideband Video Amplifier
300	Applications of the μA777
311	μA760, A High Speed Monolithic Comparator
317	A High Output Power (5 Watt), Low Distortion, IC Amplifier
319	The μA758, A Phase Locked Loop FM Stereo Multiplex Decoder
320	9616/17 EIA Interface Driver and Receiver
321	Operational Amplifiers As Inductors
323	Voltage Comparator Applications Using the μA734
325	The μA720, An AM Radio IC
328/1	A fully Integrated High Quality AM/FM Stereo Receiver
	Voltage Regulator Applications Handbook
	Interface Handbook — Line Drivers and Receivers

App. Note Index by Device No.

Device No.	App. Note No.	Device No.	App. Note No.
μA702	117/2	μA749	171, 268,269
μA706	317, 328	μA753	328
μA710	116	μA757	204
μA711	116	μA758	328
μA715	265	μA760	311
μA720	325, 328	μA767	286/1
μA725	277	μA776	218
μA729	286/1	μA777	300, 321
μA732	286/1	μA780	210
μA734	323	μA781	210
μA739	171, 175, 328	μA3075	328
μA742	Trigac Brochure	9616	320
μA746	210, 267	9617	320

APPLICATION INFORMATION (Cont'd)

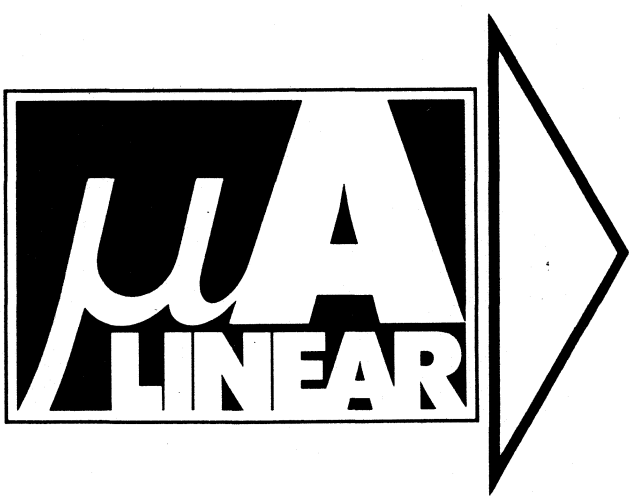
App. Note Index by Function

Functional Category	App. Note No.
AMPLIFIERS	
AGC	199, 204, 325
Audio	171, 175, 300, 317
Comparator	116, 268, 300
Compensation	117/2, 171, 175, 269
Differential	300
DC	269
Dual	268, 269
Head	265
High Input Impedance	265
IF	204, 325
Low Noise	175, 277
Operational	117/2, 171, 175, 218, 265, 268, 269, 277
Power	116, 300
Power-Audio	317
Preamp	171, 175
Pulse	300
RF	325
Sample and Hold	218, 265
Video	265, 293
Wideband	293
COMMUNICATIONS SYSTEMS	
Broadcast	
AM Radio	317, 325, 328
FM Radio	286/1, 317, 319, 328
Data Transmission	320
Pulse Modulation	
PDM	320, 323
COMPARATORS, ANALOG	116, 268, 311, 323
CONTROLS	
Remote	171
CONVERTERS	
Analog to Digital	265
Frequency — See MIXERS	
DATA TRANSMISSION	116, 311, 320
DECODERS	
Multiplex	286/1, 319
DETECTORS	
Level	116, 311
Peak, Peak to Peak	268, 311
Phase	319
Zero Crossing	311
DIVISION	
Sinewave Frequency	323

APPLICATION INFORMATION (Cont'd)

App. Note Index by Function (Cont'd)

Functional Category	App. Note No.
FILTERS, ANALOG	
Active	321
Band Pass	321
INSTRUMENTATION	
Phase Meter	323
Tester/Second Breakdown	227/2
LINE DRIVERS	320, Interface Handbook — Line Drivers & Receivers
LINE RECEIVERS	116, 311, 320, Interface Handbook — Line Drivers and Receivers
MIXERS — See also OSCILLATORS	325
MULTIPLEXERS	
Analog	218
NOISE	
Immunity	116
OSCILLTORS	
Audio	300, 325
Current Controlled	218
Free Running	116, 323
Pulse	323
Sinusoidal	300
Voltage Controlled	319, 321, 323
Wien Bridge	300
PACKAGES, SEMICONDUCTOR	
Thermal Considerations	205
POWER	
Dissipation	205
POWER SUPPLIES	
Regulators	116, 325, Voltage Regulator Applications Handbook
TELEVISION — See also COMMUNICATION SYSTEMS	
AGC Section	199, 204
Audio Section	317
Color Signal Processing Section	210, 267
IF Section	204
Receiver Systems	267
Remote Control	171
Video Amplifier Section	293
TESTING	205
TUNERS	
VHF	199
VOLTAGE REGULATOR	Voltage Regulator Applications Handbook



GLOSSARY

Admittance Characteristics, Forward Transfer Admittance – The ratio of the output current to the input voltage with the output short circuited. (Y_{21}) (mmho)

Admittance Characteristics, Input Admittance – The ratio of the input current to the input voltage with the output short circuited. (Y_{11}) (mmho)

Admittance Characteristics, Output Admittance – The ratio of the output current to the output voltage with the input short circuited. (Y_{22}) (mmho)

Admittance Characteristics, Reverse Transfer Admittance – The ratio of the input current to the output voltage with the input short circuited. (Y_{12}) (mmho)

AGC Range – The amount by which the maximum gain can be reduced. (dB)

AM Rejection – The ratio of the recovered audio output produced by a desired FM signal with specified modulation, amplitude and frequency to that produced by an AM signal, on the same carrier, with specified modulation index.

Average Temperature Coefficient of Input Offset Current – The ratio of the change in input offset current, over the operating temperature range, to the operating temperature range ($\Delta I_{OS}/\Delta T_A$) (pA/°C)

Average Temperature Coefficient of Input Offset Voltage – The ratio of input offset voltage, over the operating temperature range, to the operating temperature range. ($\Delta V_{OS}/\Delta T_A$) (μV/°C)

Average Temperature Coefficient of Output Voltage – The change in output voltage for a specified change in ambient temperature ($\Delta V_{OUT}/\Delta T_A$) (mV/°C)

Bandwidth – The frequency at which the gain of the device is 3 dB below its low frequency value. (BW)

Broadband Noise Figure – The ratio of the input signal-to-noise ratio to the output signal-to-noise ratio over the frequency range for which the parameter is nominally flat. Usually expressed as the common log. (NF) (dB)

Burst Separator Output – The amplitude of the chroma reference burst at the output of the gated burst amplifier.

Channel Balance, Monaural Input – The ratio of the outputs from the right channel to the output of the left channel with a monaural signal applied to the input.

Channel Separation – The log of the ratio of the output of an undriven amplifier to the output of an adjacent driven amplifier. (dB)

Clamped Output High Voltage – The voltage potential necessary to turn on (forward bias) the clamping diode on the output pin (V_{OHC}) (V).

Clamped Output Low Voltage – The voltage potential necessary to turn off (reverse bias) the clamping diode on the output pin. (V_{OLC}) (V)

Clock Frequency – The reciprocal of the clock period; the clock repetition rate. (f_{clock}) (ns)

Clock Input, Amplitude – The peak amplitude of the clock signal.

Clock Input, Width – The time duration of the clock pulse. (t_{PW}) (ns)

Common Mode Gain – The ratio of the output voltage change to the input common mode voltage producing that change.

Common Mode Input Overload Recovery Time – The time delay between removal of an input common mode voltage outside the input common mode range, and resumption of normal device operation. (ns)

Common Mode Input Resistance – The value of resistance with respect to a common mode signal, seen when looking into both inputs. (Ω)

Common Mode Input Voltage Swing – The peak value of the common mode input voltage at which the device will operate in a linear fashion. (V)

Common Mode Output Voltage – The output voltage resulting from the application of a voltage common to both inputs. (V)

Common Mode Rejection Ratio – The ratio of the change in input offset voltage to the total change in common mode voltage. (CMRR) (dB)

Common Mode Voltage – The arithmetic mean of the voltage present at the differential inputs with respect to the device ground reference. (V_{CM}) (V)

Converter Transconductance – The ratio of the converter output ac current to the input voltage causing it.

DC Reverse (Leakage) Current – The leakage current flowing from cathode to anode at some specified reverse bias voltage. (I_{CBO}) (pA or nA)

Delay Time – See Propagation Delay (t_d) (ns)

Differential Input Bias Current – The current required in the differential input stage to bias the stage into operation.

Differential Input Capacitance – The effective capacitance between the two inputs, operating open loop.

Differential Input Impedance – The impedance seen looking between the input terminals.

Differential Input Offset Current – The difference in currents required by the transistors in the input stage to bias the input stage to its quiescent operation point.

Differential Input Overload Recovery Time – The time delay between removal of a differential input voltage that exceeds the differential input voltage operating range, and resumption of normal device operation.

Differential Input Resistance – The effective resistance between the two inputs, operating open loop.

Differential Input Threshold Voltage – The voltage difference between the + and – inputs required to guarantee the output logic state.

Differential Input Voltage Range – The range of voltage applied between the input terminals for which operation remains within specifications.

Differential Load Rejection – The ratio of the change in input offset voltage to the change in differential load current.

Differential Output Resistance – The resistance measured between the two output terminals.

Differential Output Voltage Swing – The peak differential output voltage that can be obtained without clipping the output voltage waveform.

Differential Voltage Gain – The ratio of the change in differential output voltage to the change in differential input voltage.

Dropout Voltage – The input-output voltage differential that causes the output voltage to decrease by 5% of its initial value. (V_{DO}) (V)

Equivalent Input Noise Current – The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance. (i_n) (pA/$\sqrt{Hz}$)

Equivalent Input Noise Voltage – The input noise voltage that would reproduce the noise seen at the output if all amplifier noise sources and the source resistances were set to zero. (e_n) (nV/$\sqrt{Hz}$)

Fall Time – The time required for the signal to fall from 90% to 10% of its output value into a specified load network. (t_f) (ns)

Feedback Capacitance – The effective value of the capacitive coupling from output to input.

Feedback Sense Voltage – The voltage measured on the feedback terminal of the regulator, with respect to ground, when the device is operating in regulation. (V_{sense}) (V)

Forward Transadmittance – See Admittance, Forward Transfer (Y_{21}).

Frequency Response – The frequency at which the output drops to 0.707 of its low frequency value.

Gain Bandwidth Product – The frequency at which the small signal ac gain of the device reduces to unity. (f_t) (MHz)

High Frequency Current Gain – The small signal ac current gain at a specified frequency. (h_{fe})

Hysteresis – The voltage difference between the switching points of the device. See Lower Input Threshold Voltage and Upper Input Threshold Voltage. (ΔV_{TH})

IF Transconductance – The ratio of the output ac IF current to the input signal voltage.

Input Bias Current – The average of the two input currents with no signal applied. (I_{BIAS}) (nA or pA)

Input Bias Current Drift – The change in input bias current with temperature supply voltage, or time. ($\Delta I_{BIAS}/\Delta T$, ΔV_S, Δt)

Input Capacitance – The equivalent capacitance of either input with the other input grounded. (C_{IN}) (pF)

Input Clamp Diode Voltage – The input voltage at which the clamp diode associated with the input becomes forward biased. (V_{CD}) (V)

Input Common Mode Voltage Range – The range of common mode input voltage over which the device will operate within specifications. (CMVR) (V)

Input Current – The current flowing into the input with a specified voltage applied to the input. (I_{IN})

Input Current at Maximum Input Voltage – The current into a TTL or DTL input with the absolute maximum allowed input voltage applied to the input.

Input Forward Current – See Input LOW Current.

Input High Current – The current flowing into a device lead with the specified V_{IH} applied to the input. (I_{IH}) (μA)

Input High Voltage – The minimum input voltage that allows the input to remain in a logic HIGH state. (V_{IH}) (V)

Input Latch Voltage – See Input Clamp Diode Voltage.

Input Low Current – The current flowing out of an input lead with the specified V_{IL} applied to the input (I_{IL}) (mA)

Input Low Voltage – The maximum input voltage that allows the input to remain in a logic LOW state. (V_{IL}) (V)

Input Noise Voltage – The rms noise voltage present at the amplifier output divided by the gain of the amplifier, measured with the inputs connected to ground through a low resistance. (e_n)

Input Offset Current – The difference in current into the two input terminals with the output voltage at zero. In a comparator, it is the difference between the two input currents with the output at the logic threshold voltage. Also, it is defined as the difference in input currents required to give equal output currents from a matched pair of devices (I_{OS}) (nA or pA)

Input Offset Current Drift – The change in input offset current produced with time, voltage or temperature. $\Delta I_{OS}/\Delta T$, ΔV, Δt (pA/°C, V, s)

Input Offset Voltage – The voltage applied between the input terminals, through two equal resistances, to obtain zero output voltage. In Comparators, it is the voltage applied to the input terminals to give the logic threshold voltage at the output. It is also defined as the input voltage differential required to give equal output currents from a matched pair of devices. (V_{OS}) (mV)

Input Offset Voltage Drift – The change in input offset voltage with time, voltage or temperature. ($\Delta V_{OS}/\Delta T$, ΔV, Δt) (μV/°C, V, s)

Input-Output Voltage Differential – The voltage range between the unregulated input voltage and the regulated output voltage in which a regulator operates within specifications.

Input Resistance – The equivalent resistance seen looking into either input terminal with the other terminal grounded. (R_{IN}) (MΩ)

Input Reverse Current – See Input HIGH Current. (I_R) (μA)

Input to Output Delay – See Propagation Delay.

Input Voltage – The voltage potential between the input terminal and the device ground reference. (V_{IN}) (V)

Input Voltage (Min) – The minimum voltage required to bias the reference to specification limits. $V_{IN(MIN)}$ (V)

Input Voltage Range – The range of voltage on an input terminal over which the device operates as specified. (V_{IN}) (V)

Intermodulation Products – Undesired output signals created by interaction of undesired input signals.

Killer Off Threshold – The voltage required at the color killer terminal to restore the chroma output.

Killer On Threshold – The voltage required at the color killer terminal to kill the chroma output.

Large Signal Voltage Gain – The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Limiting Sensitivity – The value of input voltage above which the output is 3.0 dB below its limited value.

Line Regulation – The change in output voltage for a specified change in input voltage. ($\Delta V_{OUT}/\Delta V_{IN}$) (mV or %)

Linearity – The deviation of the characteristic from a straight line.

Load Regulation – The change in output voltage for a specified change in load current. ($\Delta V_{OUT}/\Delta I_L$) (mV or %)

Noise Figure – The ratio of the input signal-to-noise ratio to the output signal-to-noise ratio. Usually expressed as common log. (NF) (dB)

1/F Noise – The noise measured at a specified low frequency below the frequency range where the device noise spectrum is essentially flat. (nV)

Open Loop Voltage Gain – The ratio of the output signal voltage to the differential input signal voltage, with no feedback applied. (A_{VOL}) (dB or V/mV)

Oscillator Control Sensitivity – The ratio of the change in oscillator frequency to the change in control voltage causing it.

Oscillator Pull-In Range – The range of free-running frequency over which the oscillator is locked to the incoming signal.

Oscillator Static Phase Error – The phase difference between the oscillator output and the incoming frequency to which it is locked.

Output Common Mode Voltage – The arithmetic mean of the two output voltages for devices with differential outputs.

Output Conductance – The resistive value of the output admittance.

Output Fall Time – See Fall Time.

Output HIGH Current – The current sourced by the output while maintaining a HIGH output logic level. (I_{OH})

Output HIGH Voltage – The output voltage that defines a logic HIGH output state. (V_{OH}) (V)

Output Impedance – The equivalent impedance seen looking into the output terminal. (Z_O) (Ω)

Output Leakage Current – The leakage current into the output transistor at the specified output voltage potential for uncommitted or open-collector outputs. (I_{CEX}) (μA)

Output Low Voltage – The voltage that defines the logic LOW output state. (V_{OL}) (V)

Output Noise Voltage – The rms value of the noise voltage measured at the output with constant load current and no input ripple. (e_{no}) (μV)

Output Offset Voltage – The voltage difference between the two outputs with both inputs grounded.

Output Resistance – The small signal ac resistance seen looking into the output with no feedback applied and the output dc voltage near zero. For comparators, it is the resistance seen looking into the output with the dc output level at the logic threshold. (R_O) (Ω)

Output Rise Time – See Rise Time

Output Saturation Voltage – The dc voltage between output and ground in the saturated condition.

Output Short Circuit Current – The output current obtainable with the output shorted to ground or to either supply. (I_{SC}) (mA)

Output Sink Current – The maximum current into the collector of an open-collector device. (I_{SINK}) (mA)

Output Voltage – The voltage present at the output terminal referred to ground. (V_{OUT}) (V)

Output Voltage Range – The range of output voltages over which the specifications apply. (ΔV_{OUT}) (V)

Output Voltage Swing – The peak output voltage swing, referred to zero, that can be obtained without clipping the output voltage waveform ($\pm V_{OUT}$) (V)

Overshoot – The difference between the peak amplitude of the output and the final value of the output divided by the output times 100%. (%)

Peak Output Current – The maximum current delivered by the device for a period too short for thermal protection to be activated. ($I_{OUT(Pk)}$) (A)

Phase Margin – The difference between 180° and the phase shift at the frequency where the open loop gain equals unity.

Play-Through Voltage – The signal voltage measured at the output with the volume control set for minimum output.

Power Bandwidth – The maximum frequency at which the maximum output can be maintained without significant distortion.

Power Consumption – The dc power required to operate the device under no load conditions.

Power Dissipation (Max) – The maximum power that can be dissipated in the device with a given heat sink beyond which the device may not perform to specification. ($P_{D(MAX)}$) (mW)

Power Supply Current – The current required from the power supply to operate the amplifier with no load and no signal applied. (I_{SS}) (mA)

Power Supply Rejection Ratio – The ratio of the change in input offset voltage to the change in power supply voltage. (PSRR) (μV/V)

Power Supply Sensitivity – The ratio of the change of a specified parameter to the change in supply voltage.

Propagation Delay – The time interval between appli-

cation of an input voltage step and its arrival at the output, measured at the 50% of final value points. (t_p) (ns)

Propagation Delay Time, HIGH to LOW Output – The propagation delay of a signal causing the output to change from a HIGH to a LOW logic state. (t_{PHL}) (ns)

Propagation Delay Time, LOW to HIGH Output – The propagation delay of a signal causing the output to change from a LOW to a HIGH logic state. (t_{PLH}) (ns)

Quiescent Current – That part of a regulator input current that is not delivered to the load. (I_Q) (mA)

Quiescent Output Current – The output current with no signal applied to the input.

Recovered Audio – The value of the audio voltage measured at the detector output under the specified circuit conditions.

Reference (Control) Current – The current drawn or supplied by the reference (control) terminal (I_{REF}) (μA)

Reference Voltage – The output of the reference amplifier measured with respect to the negative supply. (V_{REF}) (V)

Response Control Input Current – The current flowing out of the response control pin that is available to charge the response control capacitor. (I_{RIN})

Response Time – The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level. (t_{resp}) (ns)

Reverse Recovery Time – The time taken for the reverse recovery current to fall to a specified value after removal of the reverse bias under specified conditions. (t_{rr}) (ns)

RF Noise Voltage – The equivalent input noise voltage of the RF stage.

RF Transconductance – The ratio of the RF output current to the RF input voltage.

Ripple Rejection – The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage. (dB)

Rise Time – The time interval required for a signal to rise from 10% to 90% of its final amplitude. (t_r) (ns or μs)

Settling Time – The time from a step change of input to the time the corresponding output settles to within a specified percentage of the final value. (ns)

Short-Circuit Current Limit – The output current of a regulator with the output shorted to common (ground). (I_{SC}) (mA)

Short-Circuit Load Current – The maximum output current which the device will provide into a short-circuit.

67 kHz Storecast Rejection – The ratio of the 67 kHz SCA signal at the output to the desired output with the standard FCC signal input.

Slew Rate – The maximum rate of change of output under large signal conditions. (SR) (V/μs)

Standby Current Drain – The supply current drawn by a regulator with no output load and no reference voltage load (see Quiescent Current).

Static Forward Current Transfer Ratio – The ratio of dc collector current to base current in a transistor. (h_{FE})

Stereo Separation – The ratio of the right and left channel outputs for a standard input signal with specified audio frequency.

Storage Time – The propagation delay due to stored charge in the transistor. (t_s) (ns)

Strobe Activation Voltage – The voltage applied to the strobe terminal beyond which the device does not respond to the conditions at the input terminals. (V)

Strobe Current – The maximum current taken by the strobe terminal during activation. (I_{Strobe}) (μA)

Strobe Release Time – The time required for the outputs to rise to the logic threshold voltage after the strobe terminal has been activated.

Strobed Output Level – The dc output voltage, independent of input voltage, with the voltage on the strobe terminal in excess of the strobe activation voltage. (V)

Supply Regulation – The change in internal device supply voltage for a specified change in external power supply voltage.

Supply Voltage Rejection Ratio – See Power Supply Rejection Ratio.

Switching Speed – See Propagation Delay.

Temperature Coefficient – See Average Temperature Coefficient of specific parameter.

GLOSSARY (Cont'd)

Temperature Stability – The percentage change in output voltage over a specified ambient temperature range ($\Delta V_{OUT}/\Delta T_A$) (V/°C)

Terminating Resistance – The resistance normally used to provide a termination to a transmission line.

Threshold Voltage – The input voltage at which the output logic level changes state. (V_{TH}) (V)

Total Harmonic Distortion – The rms value of the harmonic content of a signal expressed as a percentage of the rms value of its fundamental. (THD)

Transient Response – The closed loop step function response of the circuit under small signal conditions.

Transition Time, HIGH to LOW Output – See Fall Time.

Transition Time, LOW to HIGH Output – See Rise Time.

Turn-off Delay – See Propagation Delay Time, LOW to HIGH Output (t_{PLH}) (ns)

Turn-off Propagation Delay – See Propagation Delay Time, LOW to HIGH Output. (t_{PLH}) (ns)

Turn-off Time – See Propagation Delay Time, LOW to HIGH Output (t_{PLH}) (ns)

Turn-on Delay – See Propagation Delay Time, HIGH to LOW Output (t_{PHL}) (ns)

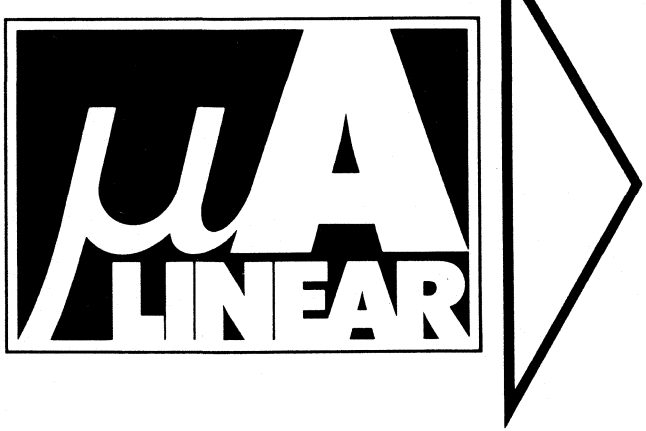
Turn-on Propagation Delay – See Propagation Delay Time, HIGH to LOW Output (t_{PHL}) (ns)

Turn-on Time – See Propagation Delay Time, HIGH to LOW Output (t_{PHL}) (ns)

Unity Gain Bandwidth – The frequency at which the open loop gain is reduced to unity. (f_t) (MHz)

Upper Threshold Voltage – The input voltage that causes the output to change logic state, when the input voltage is increasing in a device with hysteresis. (V_{TH+})

Voltage Gain – The ratio of the output voltage to the input voltage under small signal conditions. For comparators, it is the ratio of the change in output voltage to the change in voltage between the input terminals, with the dc output in the vicinity of the logic threshold. (A_V) (dB or V/mV)



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